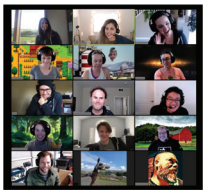
inst.eecs.berkeley.edu/~ee241b

EE241B : Advanced Digital Circuits

Lecture 22 – Reducing Leakage

Borivoje Nikolić



Sweetfarm.org/goat-2-meeting: Invite a goat or a llama to a zoom meeting

https://www.sweetfarm.org/goat-2-meeting

Announcements

- Assignment 4 due next Friday.
- Reading
  - Rabaey, LPDE, Chapter 8

Outline

- Module 5
  - Clock gating
  - Leakage reduction during design time and runtime

5.G Reducing Switching Activity Through Logic Design

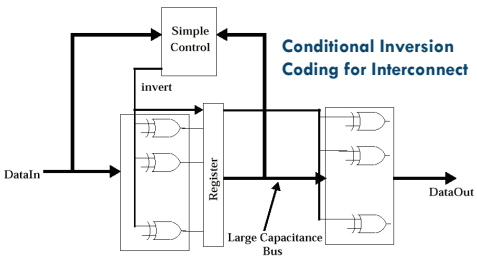
Power /Energy Optimization Space

	Constant Throughput/Latency		Variable Throughput/Latency
Energy	**Design Time**	**Sleep Mode**	**Run Time**
Active	Logic design Scaled V_{DD} Trans. sizing Multi-V_{DD}	Clock gating	DFS, DVS
Leakage	Stack effects Trans sizing Scaling V_{DD} + Multi-V_{Th}	Sleep T's Multi-V_{DD} Variable V_{Th} + Input control	+ Variable V_{Th}

Basic Idea

- $E \sim \alpha CV^2$
- Reduce switching activity, α, through logic and architectural transformations
- Many options
  - Switching activity lower with deeper logic
  - Pipelining has significant effect
  - Reduce the number of clocked devices in a flip-flop
    - e.g. group generation of clk_b
  - A few logic ideas follow

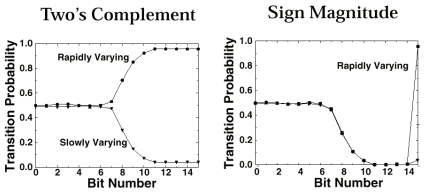
Circuit-Level Activity Encoding



from [Stan94]
(*1994 International Workshop on Low-power Design*)

Number Representation

- Input signals are noise most of the time



- Sign-extension activity significantly reduced using sign-magnitude representation

5.H Clock Gating

Power /Energy Optimization Space

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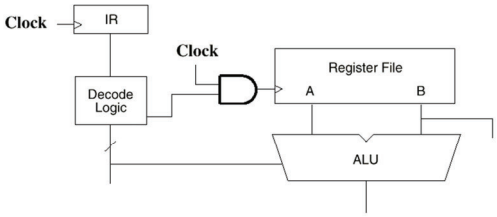
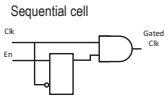
Clock Gating



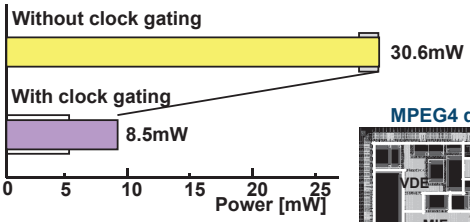
Requires a bit more complex gate ...
Well handled in today's EDA tools

Clock Gating

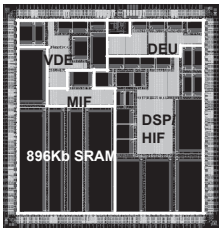
- Enabling clock needs to be synchronized



Clock Gating Efficiently Reduces Power



MPEG4 decoder



90% of F/F's were clock-gated.

70% power reduction by clock-gating alone.

Courtesy M. Ohashi, Matsushita, ISSCC 2002

Clock Gating

- ARM Cortex-A9 Technical Reference Manual:

Dynamic high level clock gating activity

When dynamic high level clock gating is enabled the clock of the integer core is cut in the following cases:

- the integer core is empty and there is an instruction miss causing a linefill
- the integer core is empty and there is an instruction TLB miss
- the integer core is full and there is a data miss causing a linefill
- the integer core is full and data stores are stalled because the linefill buffers are busy.

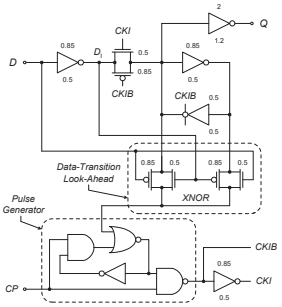
When dynamic clock gating is enabled, the clock of the system control block is cut in the following cases:

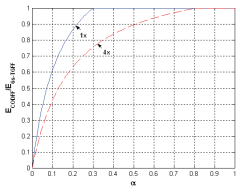
- there are no system control coprocessor instructions being executed
- there are no system control coprocessor instructions present in the pipeline
- performance events are not enabled
- debug is not enabled.

When dynamic clock gating is enabled, the clock of the data engine is cut when there is no data engine instruction in the data engine and no data engine instruction in the pipeline.

Local Clock Gating

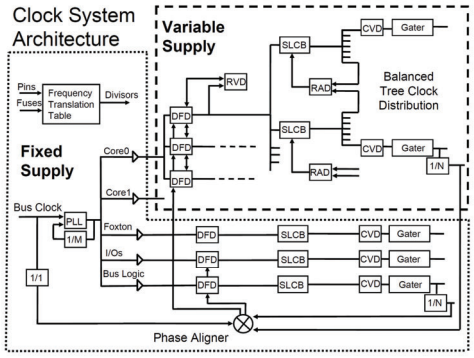
Local Clock Gating





'Clock on demand' Flip-flop

Complex Designs



Fischer, ISSCC'05

Power /Energy Optimization Space

	Constant Throughput/Latency		Variable Throughput/Latency
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Plan For the Rest of the Semester

- 4 more lectures:
  - Finish low power (2 lectures)
  - Supplies, clocks and their interaction
- Homework 4 due on April 24th
  - Quiz 4 on April 28th
- Final on April 30th
  - 80 minutes, open everything
- Final presentations, May 4
  - Final reports due on May 4

5.1 Lowering Leakage During Design: Multiple Thresholds

Power /Energy Optimization Space

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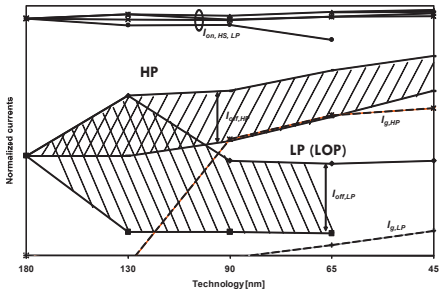
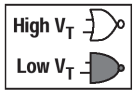
Technology Options

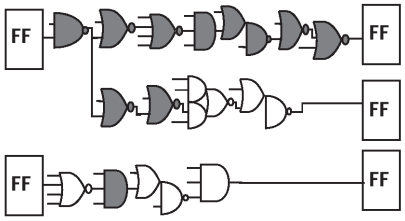
- Multiple thresholds, each spaced 50-100mV apart (5-10x less leakage)



Using Multiple Thresholds

- Cell-by-cell V_T assignment (not block level)
- Allows us to minimize leakage
- Achieves all-low-V performance





Yano, SSTCW'00

Typical Technologies

- 2-3 Thresholds
  - To choose from 4-6 in a node
  - In bulk and finfet, but not in FDSOI (unless doped)
- Threshold voltage diff ~5-10x in leakage

5.I Lowering Leakage During Design: Longer Channels

Power /Energy Optimization Space

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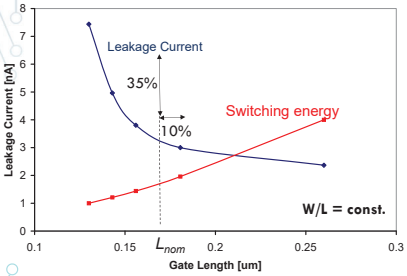
Longer Channels

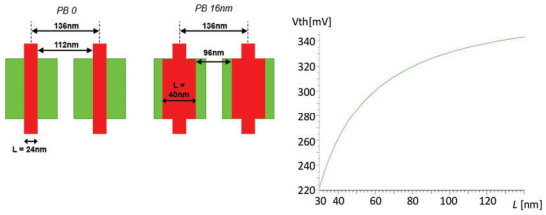


- 10% longer gates reduce leakage by 35% (in 130nm)
- Increases switching energy by 21% with W/L = const.

- Attractive when don't have to increase W (memory)
- Doubling *L* reduces leakage by 3x (in 0.13um)
- Much stronger effect in 28nm!
- Effect improves with shorter channel devices

Poly Bias

- 28FDSOI example



Longer Channels

5.J Lowering Leakage During Design: Transistor Stacking

Power /Energy Optimization Space

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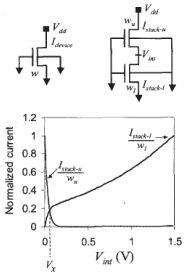
Stack Effect

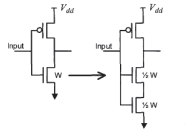


Reduction (in 0.13µ):

	High V_t	*Low* V_t
2 NMOS	10.7X	9.96X
3 NMOS	21.1X	18.8X
4 NMOS	31.5X	26.7X
2 PMOS	8.6X	7.9X
3 PMOS	16.1X	13.7X
4 PMOS	23.1X	18.7X

Narendra, ISLPED'01

Stack Forcing



Tradeoffs:
- W/2 – 1/3 of drive current, same loading
- 1.5W – 3x loading, same drive current

Narendra, ISLPED'01

Next Lecture

- Low-power design
  - Power gating
  - Dynamic thresholds
  - Optimal supplies and thresholds