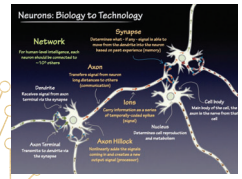
inst.eecs.berkeley.edu/~ee241b

EE241B : Advanced Digital Circuits

Lecture 24 – DTS, Clock

Borivoje Nikolić



The Promise and Pitfalls of Neuromorphic Computers, by Sunny Bains, EE Times, April 22, 2020.

https://www.eetimes.com

Announcements

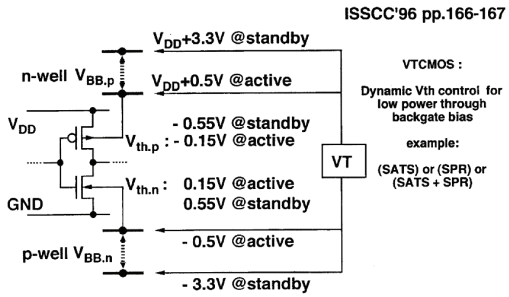
- Assignment 4 due on Friday.
  - Quiz on Tuesday
- Last lecture on Tuesday
- Final on Thursday, April 30
- Project presentations on Monday, May 4
- Reading: Wong, JSSC, 2006

Outline

- Module 5
  - Dynamic threshold scaling
  - Optimal thresholds and supplies
- Module 6
  - Clock generation

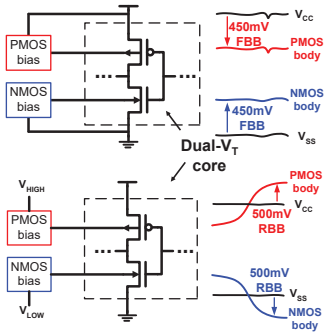
5.M Dynamic Threshold Scaling

Dynamic Body Bias (Bulk)



Switches between active and sleep

Dynamic Body Bias (Bulk)



Active mode

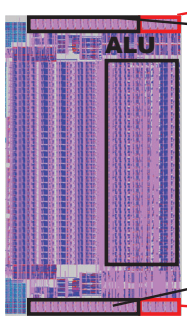
Forward body bias (FBB)
Local V_{CC} tracking

Idle mode

Reverse body bias (RBB)
Triple well needed

Tschanz, ISSCC'03

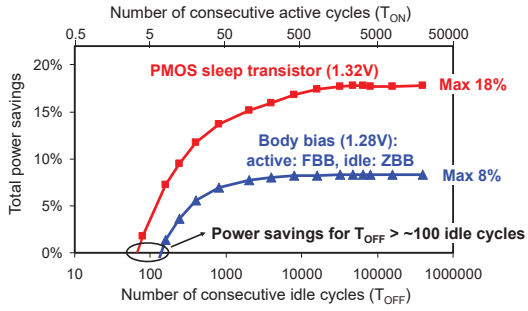
Body Bias Layout



Number of ALU core LBGs	30
Number of sleep transistor LBGs	10
PMOS device width	13mm
Area overhead	8%

Total Active Power Savings

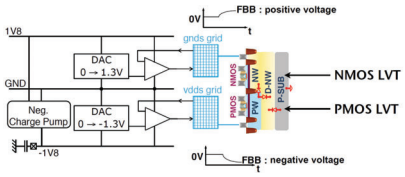
(Fixed activity: α = 0.05)



Reference: 450mV FBB to core with clock gating, 1.28V, 4.05GHz, 75°C

Generating Back-Bias

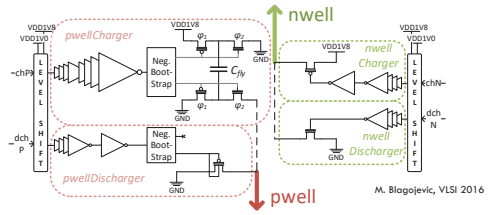
- Tradeoff – speed of charging and discharging well caps
- Often measure V_{BB} indirectly (leakage)
- Challenge: Generating $-V_{SS}$
- 28nm FDSOI implementation



D. Jacquet, VLSI 2013

Generating Back Bias

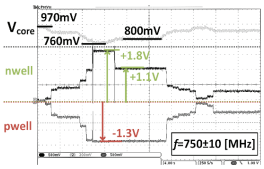
- Fast and wide voltage range back-bias in FDSOI



M. Blagojevic, VLSI 2016

Switched capacitors generate negative bias and pump substrate

Supply/Process Compensation



- Able to track ~200mV supply droops and maintain constant frequency (measured by a replica) by back-bias adjustments

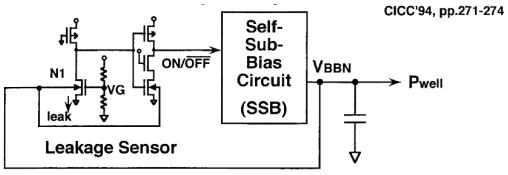
5.N Dynamic Threshold Scaling and Variations

Body Biasing and Variations

- Body biasing with a local control loop can be used to lower the impact of process variations
- Used to limit die-to-die and within-die variations

Self-Adjusting Threshold-Voltage Scheme (SATS)

- Older bulk technologies had stronger body effect

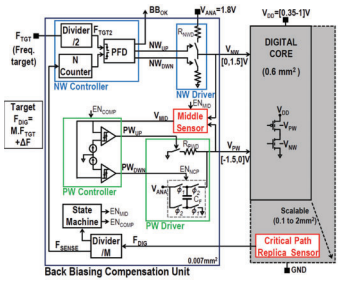


low V_{th}→ large leakage → SSB ON → deepV_{BB} → high V_{th}

high V_{th}→ little leakage → SSB OFF → shallow V_{BB} → low V_{th}

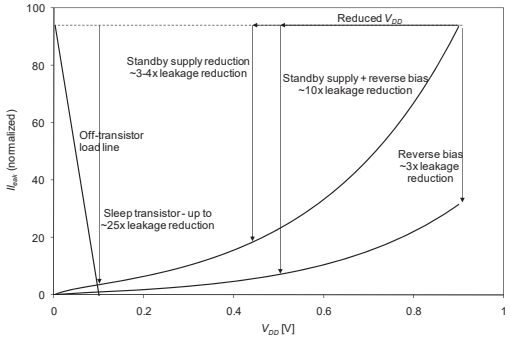
- control V_{th} to adjust leakage current
- compensate Vth fluctuation

Dynamic Frequency Loop in FDSOI



Quelen, ISSCC'18

Techniques Summary (around 130nm node)



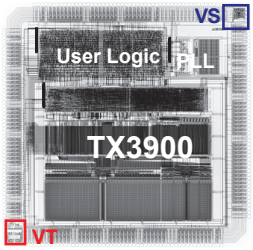
Power /Energy Optimization Space

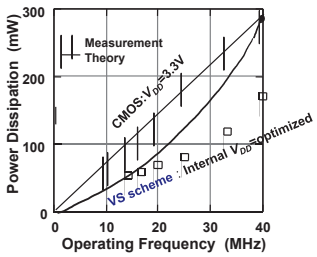
	Constant Throughput/Latency		Variable Throughput/Latency
Energy	**Design Time**	**Sleep Mode**	**Run Time**
Active	Logic design Scaled V_{DD} Trans. sizing Multi-V_{DD}	Clock gating	DFS, DVS
Leakage	Stack effects Trans sizing Scaling V_{DD} + Multi-V_{Th}	Sleep T's Multi-V_{DD} Variable V_{Th} + Input control	+ Variable V_{Th}

5.0 Optimal V_{DD}, V_{Th}

Dynamic Voltage Scaled Microprocessor

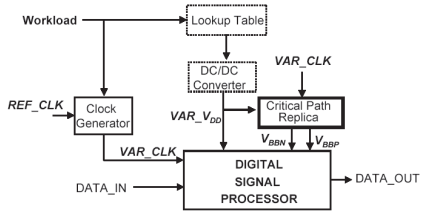
External V_{DD} 3.3V±10%
Internal V_{DDL} 0.8V~2.9V ±5%





Courtesy: Prof. Kuroda

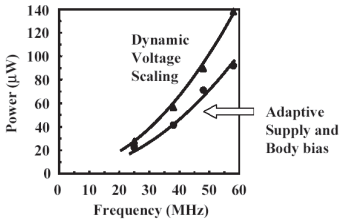
Adapting V_{DD} and V_{TH}



- Adapting both V_{DD} and V_{Th} during runtime
  - V_{Th} is much less sensitive

Miyazaki, ISSCC'02

Adapting V_{DD} and V_{TH}



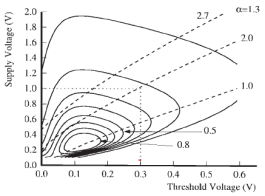
Miyazaki, ISSCC'02

Optimal V_{DD}, V_{Th}

- Adjusting V_{DD}, V_{Th} trades of energy and delay
- We studied energy-limited design
  - And alternate ways for optimizing energy and delay together
  - E.g. energy-delay product (EDP)
  - Or $E^n D^m$, $n,m > 1$

Optimal EDP Contours

- Plot of EDP curves in V_{DD}, V_{Th} plane



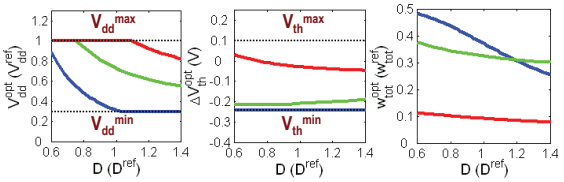
Gonzalez, JSSC 8/97

Sizing, Supply, Threshold Optimization

Reference Design:
D^{ref} (V_{dd}^{max},V_{th}^{ref})

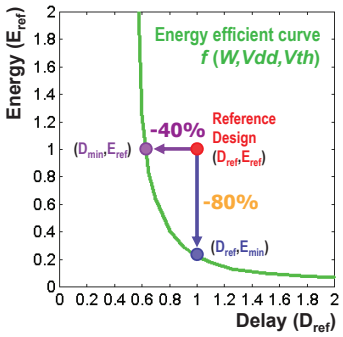
Topology	Inverter	Adder	Decoder
$(E_{Lk}/E_{Sw})^{ref}$	0.1%	1%	10%

Large variation in optimal circuit parameters V_{dd}^{opt}, V_{th}^{opt}, w^{opt}



Technology parameters (V_{dd}^{max}, V_{th}^{ref}) rarely optimal

Result: E-D Tradeoff in an Adder



Sensitivity	W	Vdd	Vth
(D_{ref},E_{ref})	∞	1.5	0.2
(D_{ref},E_{min})	1		
(D_{min},E_{ref})	22	16	22

80% of energy saved without delay penalty

40% delay improvement without energy penalty

Energy-constrained delay

- Active power

$$P_{act} = \alpha f C V_{DD}^2$$

$$f = 1/L_D t_p$$

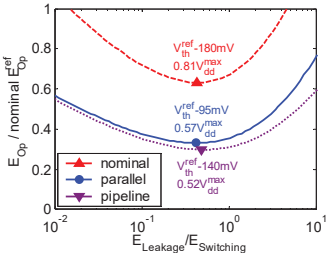
- Leakage power

$$P_{leak} = I_0 e^{\frac{-V_{Th}-\gamma V_{DD}}{S}} V_{DD}$$

- Eliminate one variable(V_{Th}) and find $P_{min}(V_{DD})$

Nose, ASP-DAC'00

Minimum energy: $E_{Sw} = 2_{ELk}$

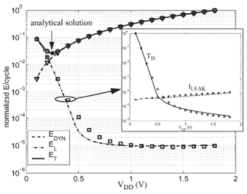


- Large $(E_{Lk}/E_{Sw})^{opt}$
- Flat E_{Op} minimum
- Topology dependent

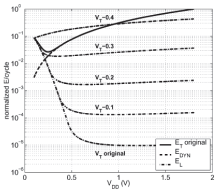
$$\left(E_{Lk}/E_{Sw}\right)_{opt} = \frac{2}{\ln\left(\frac{L_d}{\alpha_{avg}}\right) - K}$$

Optimal designs have high leakage ($E_{Lk}/E_{Sw} \approx 0.5$)

Subthreshold Optimum



f = 30kHz



Minimum is independent of V_T

Calhoun, JSSC 9/05

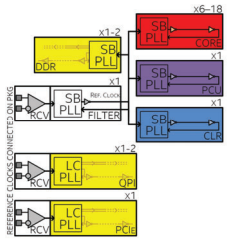
6. Clocks and Supplies

Clock Subsystem

- Clock Generation
- Clock Distribution
- Synchronization

Clock Subsystem

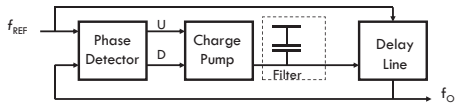
- Intel Xeon – Bowhill, ISSCC'15
  - Independent clocks for 4-18 cores
- Self-biased (SB) and LC PLLs



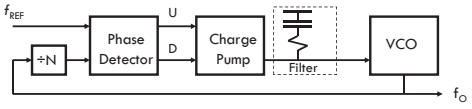
6.B Clock Generation

Clock Generation

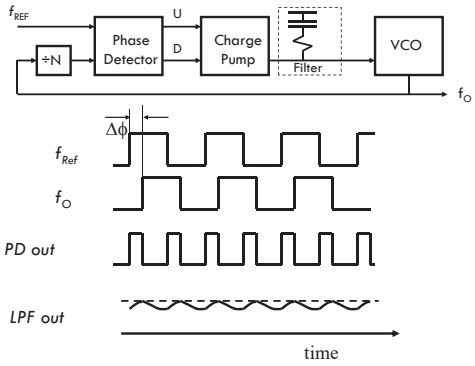
Delay-Locked Loop (Delay Line Based)



Phase-Locked Loop (VCO/DCO-Based)



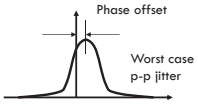
PLL Signals

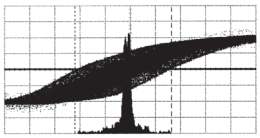


Loop Performance

- Ideal clock
  - Clock w/ jitter

  - Phase offset, peak-to-peak jitter, RMS jitter

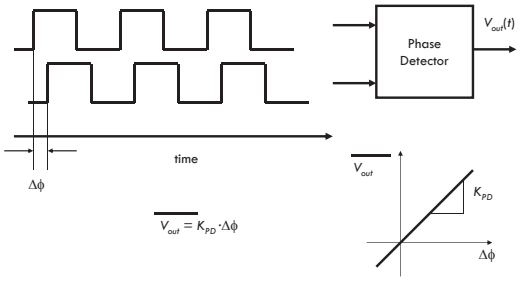




  - Bandwidth, locking time, frequency range

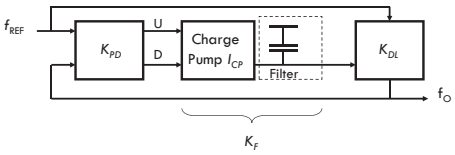
Phase Detector

- Detects the phase difference

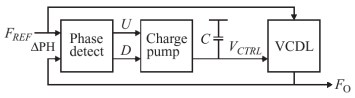


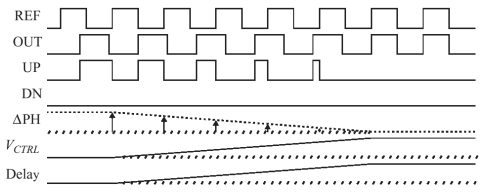
Delay-Locked Loop

- First order loop: inherently stable
- No filtering of input jitter
- Constant frequency (no synthesis)
- No phase error accumulation

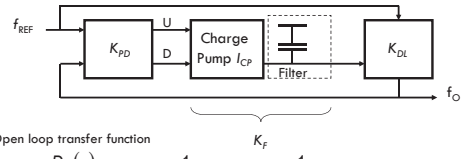


DLL Locking





Delay-Locked Loop



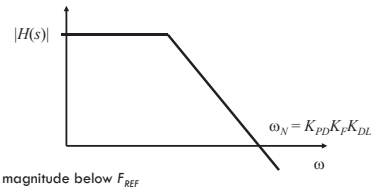
- Open loop transfer function

$$\frac{D_O(s)}{D_I(s)-D_O(s)} = K_{PD}\frac{1}{sC}I_{CP}K_{DL}F_{REF} = \frac{1}{s}K_{PD}K_FK_{DL}$$

- Closed loop transfer function

$$H(s) = \frac{D_O(s)}{D_I(s)} = \frac{K_{PD}K_FK_{DL}}{s + K_{PD}K_FK_{DL}}$$

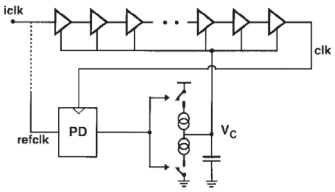
Delay-Locked Loop



- ω_N > an order of magnitude below F_{REF}
- Use of DLLs requires low-jitter input
- VCDL must span adequate delay range + reset to min delay
- Noise sources:
  - Delay line (Supply sensitivity)
  - Clock buffers that follow
  - Device noise (small)

Voltage-Controlled Delay Line

- Delay controlled by voltage with proportionality K_{DL}

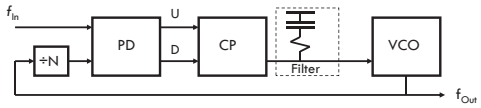


DLL Use

6.C Clock Generation: PLLs

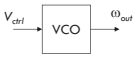
Phase-Locked Loop

- PLL is locked when the phase difference is zero
- Second/third order loop
- ÷N for frequency synthesis (and x M)
- Filters input jitter
- Accumulates phase error



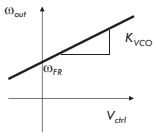
Voltage-Controlled Oscillator

- Oscillation frequency controlled by voltage



$$\omega_{out} = \omega_{FR} + K_{VCO}V_{ctrl}$$

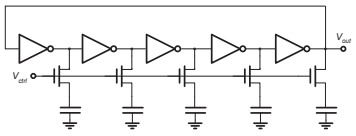
$$y_{out}(t) = A\cos\left(\omega_{FR}t + K_{VCO}\int_{-\infty}^{t} V_{ctrl}\,dt\right)$$



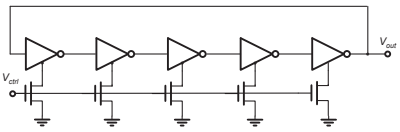
ω_{FR} – free-running frequency

Example VCO

- Ring-oscillator-based VCO: RC loaded



- Ring-oscillator-based VCO: Current-starved



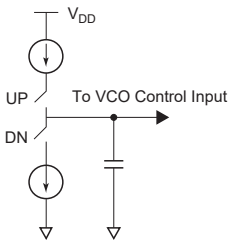
PLL vs. DLL Dynamics

- The key difference is in the VCDL vs. VCO transfer characteristics
- VCO integrates (accumulates) phase

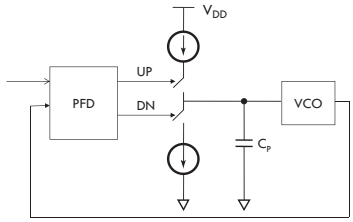
$H_{VCO}(s) = K_{VCO}/s$

Charge Pump

- Push/pull current source operation



Charge-Pump PLL

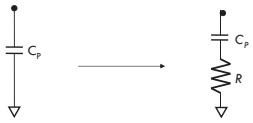


- Phase transfer function

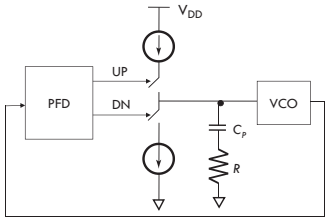
$$H(s) = \frac{\frac{K_{PFD}}{s} \cdot \frac{K_{VCO}}{s}}{1 + \frac{K_{PFD}}{s} \cdot \frac{K_{VCO}}{s}} = \frac{K_{PFD} K_{VCO}}{s^2 + K_{PFD} K_{VCO}}$$

Charge Pump PLL with a Zero

- Charge pump PLL has a stability problem
- Compensation by adding a zero



Charge Pump PLL with a Zero



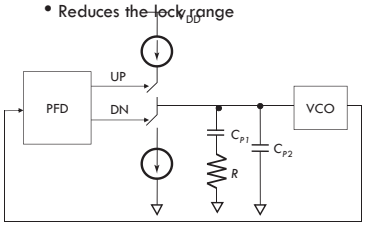
$$\omega_n = \sqrt{\frac{I}{2\pi C_P} K_{VCO}}$$

$$\zeta = \frac{R}{2} \sqrt{\frac{I C_P}{2\pi} K_{VCO}}$$

$$H(s) = \frac{\frac{K_{VCO} \cdot I}{2\pi C_P} \cdot (RC_P s + 1)}{s^2 + \frac{I}{2\pi} K_{VCO} R_S + \frac{I}{2\pi C_P} K_{VCO}}$$

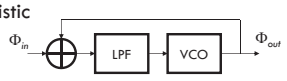
Higher Order Loops

- Another pole naturally exists
  - Filters the control voltage V_{CTRL}
  - Lowers phase margin
  - Reduces the lock range

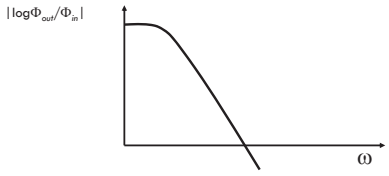


Phase Noise at the PLL Input

- Low-pass characteristic

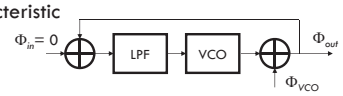


$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

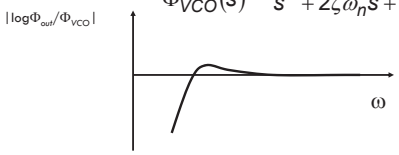


VCO Phase Noise

- High-pass characteristic



$$\frac{\Phi_{out}(s)}{\Phi_{VCO}(s)} = \frac{s(s + \omega_{LPF})}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$



Next Lecture

- Finish clocks and supplies
- Finale