

# EE241B : Advanced Digital Circuits

## Lecture 25 – Power Supply

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Time for course surveys!

Course Evaluations: Best Practices for Faculty	
<p><b>Reserve time in-class.</b> Give students time during class to complete the online course survey. Anecdotally, this is more effective when the time set aside is at the start of class.</p>	
<p><b>Inform students about the purpose of evaluations.</b> Give students examples of useful feedback you have received in the past and how the course has changed or benefited.</p>	
<p><b>Offer students incentives (e.g. extra credit).</b> To encourage broad, representative responses, instructors may choose to offer incentives to complete evaluations. An effective strategy has been to offer all students extra credit if a minimum percentage of students (e.g. 85%) respond.</p>	85%



### Announcements

- Quiz today!
- Final on Thursday, April 30, 9:30-11 am
- Project presentations on Monday, May 4
- Course surveys:
  - <https://drive.google.com/file/d/1saRVPwUtlRBApUzZ0Y9XAAG9vAhFkdV/view>

### Outline

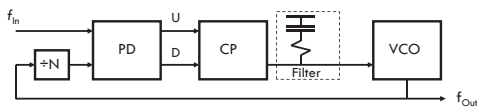
- Module 6
  - Supply distribution



### 6.C Clock Generation: PLLs

### Phase-Locked Loop

- PLL is locked when the phase difference is zero
- Second/third order loop
- $\pm N$  for frequency synthesis (and  $\times M$ )
- Filters input jitter
- Accumulates phase error



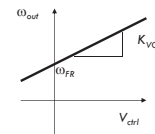
### Voltage-Controlled Oscillator

- Oscillation frequency controlled by voltage



$$\omega_{out} = \omega_{FR} + K_{VCO} V_{ctrl}$$

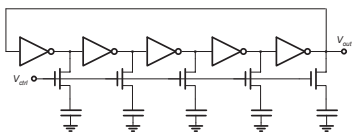
$$y_{out}(t) = A \cos(\omega_{FR} t + K_{VCO} \int_{-\infty}^t V_{ctrl} dt)$$



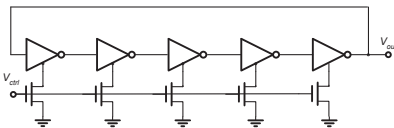
$\omega_{FR}$  – free-running frequency

### Example VCO

- Ring-oscillator-based VCO: RC loaded



> Ring-oscillator-based VCO: Current-starved



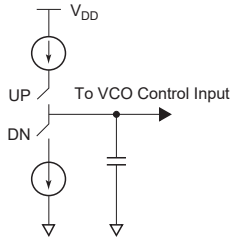
### PLL vs. DLL Dynamics

- The key difference is in the VCDL vs. VCO transfer characteristics
- VCO integrates (accumulates) phase

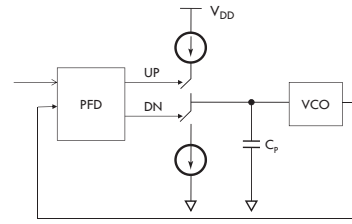
$$H_{VCO}(s) = K_{VCO}/s$$

### Charge Pump

- Push/pull current source operation



### Charge-Pump PLL

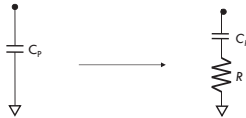


> Phase transfer function

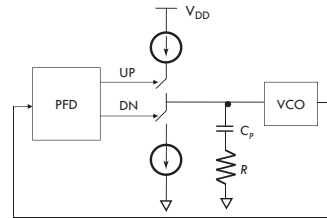
$$H(s) = \frac{\frac{K_{PFD} \cdot K_{VCO}}{s} \cdot \frac{K_{PFD} \cdot K_{VCO}}{s}}{1 + \frac{K_{PFD} \cdot K_{VCO}}{s} \cdot \frac{K_{PFD} \cdot K_{VCO}}{s}} = \frac{K_{PFD} K_{VCO}}{s^2 + K_{PFD} K_{VCO}}$$

### Charge Pump PLL with a Zero

- Charge pump PLL has a stability problem
- Compensation by adding a zero



### Charge Pump PLL with a Zero



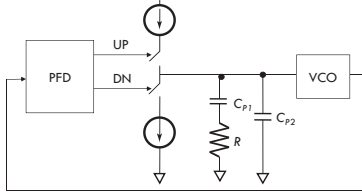
$$\omega_n = \sqrt{\frac{I}{2\pi C_P} K_{VCO}}$$

$$\zeta = \frac{R}{2} \sqrt{\frac{I C_P}{2\pi} K_{VCO}}$$

$$H(s) = \frac{\frac{K_{VCO} \cdot I}{2\pi C_P} \cdot (RC_P s + 1)}{s^2 + \frac{I}{2\pi} K_{VCO} R s + \frac{I}{2\pi C_P} K_{VCO}}$$

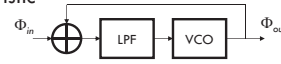
### Higher Order Loops

- Another pole naturally exists
  - Filters the control voltage  $V_{CTRL}$
  - Lowers phase margin
  - Reduces the lock range

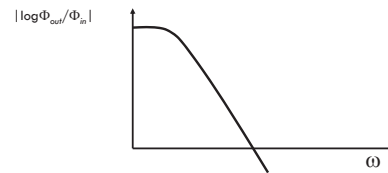


### Phase Noise at the PLL Input

- Low-pass characteristic

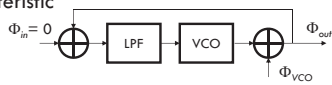


$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

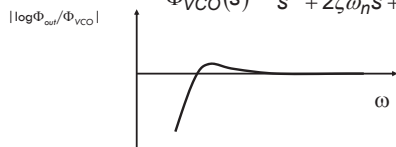


### VCO Phase Noise

- High-pass characteristic



$$\frac{\Phi_{out}(s)}{\Phi_{VCO}(s)} = \frac{s(s + \omega_{LPF})}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

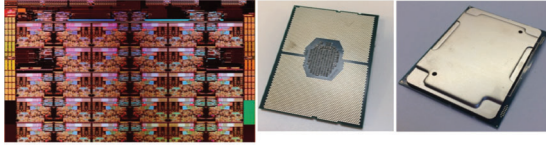
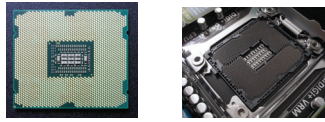


6.D Interaction with Supply

## Power Delivery

- Decoupling in Core i7

Andreas Hopf/Flickr



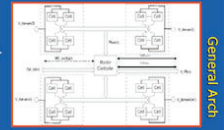
Skylake-SP, ISSCC'18

Decoupling in Skylake-SP

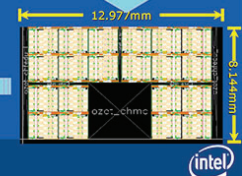
## Inside Haswell

### Integrated VR Technology

- 'Common Cell' Architecture - 20 cells
- Architecture supports flat efficiency curve
- Fine grain power management
  - Allows for multiple voltage rails
- Telemetry and Margining features
- Active Voltage Positioning for current sharing and balance
- Control features, including: JTAG, FPGA, Test/BIST



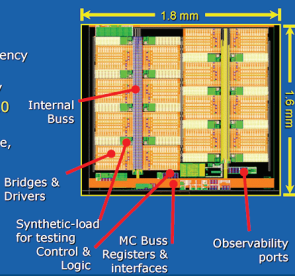
Power cell  
- 2.8 mm<sup>2</sup>



## Inside Haswell

### Review: Power Cell Architecture

- Each Power cell = Mini VR
  - Up to 25A rating\* - tested
  - Programmable switching frequency 30MHz to 140MHz
  - Ring coupled inductor topology
- 16 phases per power cell, 320 phases per chip
  - High phase count reduces noise, ripple
  - High granularity
  - Cell shedding
  - Bridge shedding
- BIST
  - Self-load and characterization system.

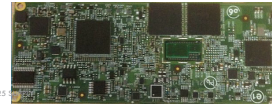
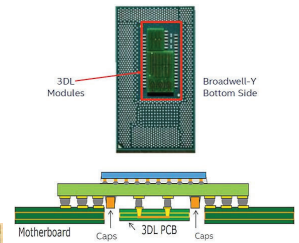
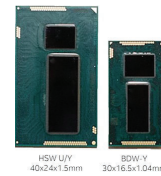


\* Thermally constrained



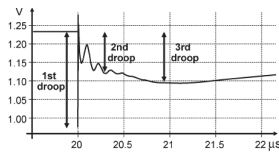
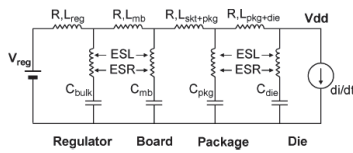
## Intel Broadwell

- Inductors moved to a small PCB



## Power Delivery

- Typical model



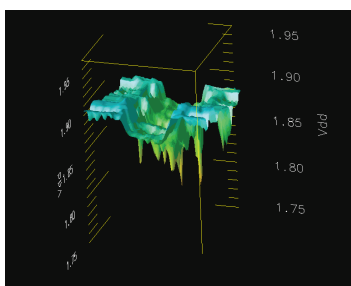
Wong, JSSC'06

## Supply Resonances

- First droop
  - Package L + on-die C
- Second droop
  - Motherboard + package decoupling
- Third droop
  - Board capacitors

## What happens with supply?

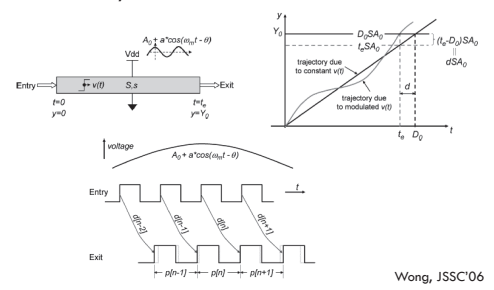
<http://www.research.ibm.com/people/r/restle/Animations/DAC01top.html>



Phillip Restle, IBM

## How to model

- Abstracted delay line

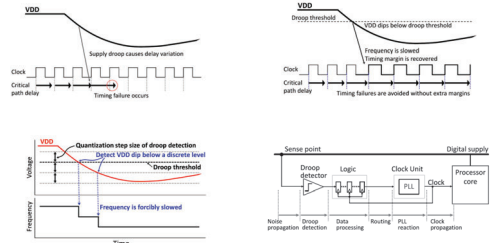


Period modulation from successive modulated delays

Wong, JSSC'06

## Droop Detection

- Hashimoto, JSSC 4/18



## This Class

- Put design choices in technology perspective
- The design constraints have changed and will be changing
  - Cost, energy, (power, leakage, ...), performance
- Focused on variability, power-performance tradeoffs, power management
- Did not cover arithmetic, domino, I/O, supply generation, packaging, ...

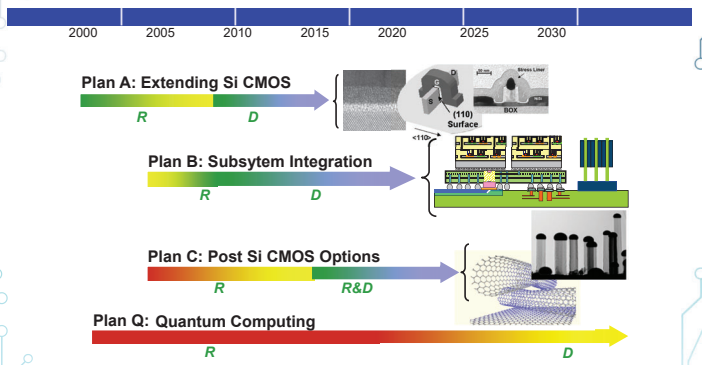
## This Field

- Moore's law will end sometime during your (my?) career
  - 5nm in 2020 scales to 0.1nm by 2050 with 2-yr cycles (or to 1nm with 4-yr cycles)
- Physics will stop CMOS somewhere ~3nm (?)
  - Will we see a different CMOS device in the meantime
- Economics will likely stop it somewhere while still in single digits
  - And the nodes will be stretched out
- We will see multi-chip/packaging solutions
- Don't worry: Creativity is unlimited!
  - What can you build with 10B/100B/1 trillion transistors?
  - Even filling 10B-transistor chips with SRAM is not trivial!

## This Field

- Focus on principles
- Watch out for opportunities
- Stay current!

## Technology Strategy / Roadmap



T.C. Chen, Where Si-CMOS is going: Trendy Hype vs. Real Technology, ISSCC'06