# EE241B : Advanced Digital Circuits

## Lecture 3 – Modern Technologies

Borivoje Nikolić

**ASML Ramps up EUV Scanners Production: 35 in 2020, up to 50 in 2021.** ASML shipped 26 extreme ultraviolet lithography (EUVL) step-and-scan systems to its customers last year, and the company plans to increase shipments to around 35 in 2020. And the ramp-up won't stop there: as semiconductor fabs ramp up their own usage of EUV process technologies, they are going to need more leading-edge equipment, with ASML expecting to sell up to 50 EUVL scanners in 2021.

**AnandTech, January 23, 2020.**

ASML's EUV Shipments

| | 2018 | 2019 | 2020 | 2021 |
|---|---|---|---|---|
| Actual | 18 | 26 | 35 | 45 - 50 |
| Target | 20 | 30 | ? | ? |

## Announcements

- Sign up for Piazza if you haven't already



## Assigned Reading

- R.H. Dennard et al, "Design of ion-implanted MOSFET's with very small physical dimensions" IEEE Journal of Solid-State Circuits, April 1974.
  - Just the scaling principles
- C.G. Sodini, P.-K. Ko, J.L. Moll, "The effect of high fields on MOS device and circuit performance," IEEE Trans. on Electron Devices, vol. 31, no. 10, pp. 1386 - 1393, Oct. 1984.
- K.-Y. Toh, P.-K. Ko, R.G. Meyer, "An engineering model for short-channel MOS devices" IEEE Journal of Solid-State Circuits, vol. 23, no. 4, pp. 950-958, Aug. 1988.
- T. Sakurai, A.R. Newton, "Alpha-power law MOSFET model and its applications to CMOS inverter delay and other formulas," IEEE Journal of Solid-State Circuits, vol. 25, no. 2, pp. 584 - 594, April 1990.



## Outline

- Scaling issues
- Technology scaling trends
- Features of modern technologies
  - Lithography
  - Process technologies

## 1.C Features of Modern Technologies



## Technology Features

- Lithography implications (this lecture)
  - Restrictions on design
  - Implications on design variability
- FEOL features (next lecture)
- Models

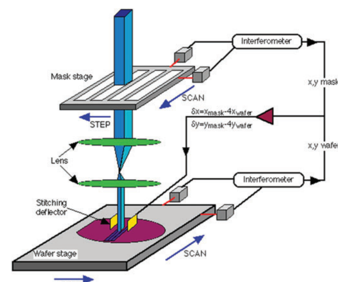


## Lithography – Key Points

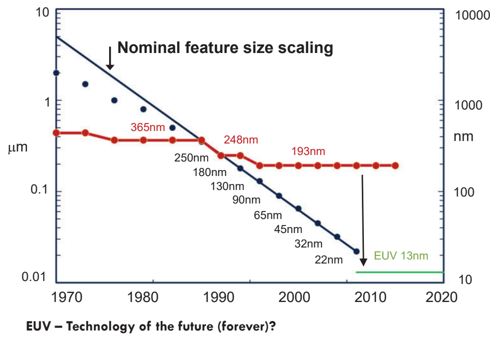
- Current lithography restricts features in design, affects variability
- This is change with EUV (expected next year in volume)
  - But that 'next year' has been taking a while to arrive



## Step-and-Scan Lithography



## Lithography Scaling

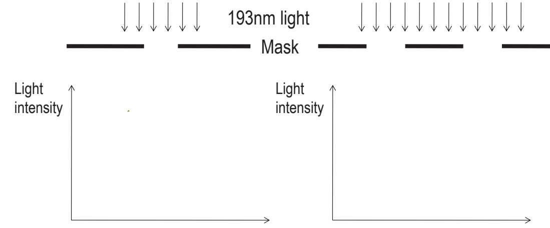



**EUV – Technology of the future (forever)?**



## Sub-Wavelength Lithography

- Light projected through a gap






## Sub-Wavelength Lithography

- CD ~ half pitch
- Decrease λ
  - Presently: 193 nm (ArF excimer laser)
  - (Distant?) future: EUV
- Increase $NA = n\sin\alpha$
  - Maximum $n$ is 1 in air
  - Presently: ~0.92-1.35
  - Immersion
- Result: Shrinking k1
  - Presently: 0.35 – 0.4
  - Theoretical limit: 0.25

$$CD = k_1 \frac{\lambda}{NA}$$

$$CD_{min} = k_1 \frac{\lambda}{NA} = 0.25 \frac{193nm}{0.92} = 50nm$$

22nm pitches beyond resolution limit



## Litho: How to Enhance Resolution?

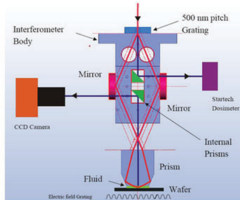
- Immersion
- Off-axis illumination
- Optical proximity correction
- Phase-shifting masks
- Double patterning



## Litho (1): Immersion

- Project through a drop of liquid
- $n_{water} = 1.47$

$$CD_{min} = k_1 \frac{\lambda}{NA} = 0.25 \frac{193nm}{1.35} = 35nm$$

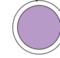



IBM

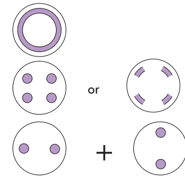


## Litho (2): Illumination

- Amplifies certain pitches/rotations at expense of others
  - **Regular Illumination**



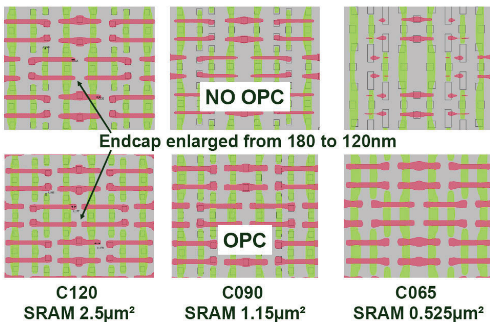
  - **Many off-axis designs (OAI)**
    - Annular
    - Quadrupole / Quasar
    - Dipole




A.Kahng, ICCAD'03



## Litho (3): Resolution Enhancement



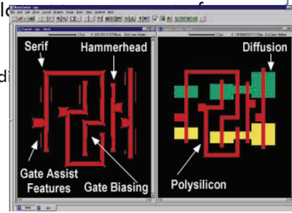

J.Hartmann, ISSCC'07

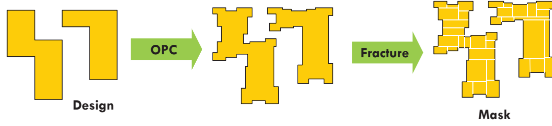


## Litho (3): OPC

## Litho (3): OPC

- Optical Proximity Correction (OPC) modifies l
  process distortions
  - Add non-electrical structures to layout to control d
  - Rule-based (past) or model-based




A.Kahng, ICCAD'03



## Inverse Lithograpphy Techniques

- OPC vs. ILT

**Optical Proximity Correction** | **Inverse Lithography Technology**

| 45nm node | 28nm node | 14nm node | 7nm node |
|---|---|---|---|
| without OPC | normal OPC | normal ILT | ideal ILT |

https://semiengineering.com/what-happened-to-inverse-lithography/

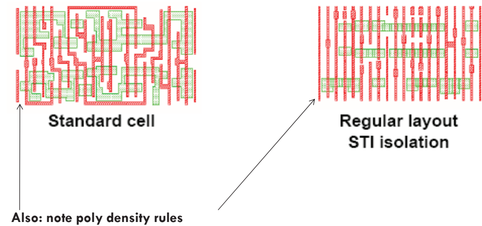


## Extreme Ultraviolet Lithography

- Wavelength $\lambda$ = 13.5nm
- Lower wafer throughput
- Simpler design rules (single patterning)
- Used on critical layers
- First deployed by Samsung in 7nm node (Exynos 9825 SoC)
  - Also used by Intel in 7nm, TSMC in 5nm



## Litho (4): Restricted Design Rules

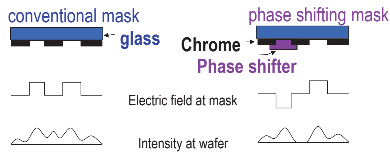



Also: note poly density rules

J.Hartmann, ISSCC'07

## Litho (5): Phase-Shift Masks

- Phase Shifting Masks (PSM)
  - Creates interference fringes on the wafer →Interference effects boost contrast →Phase Masks can make extremely small lines

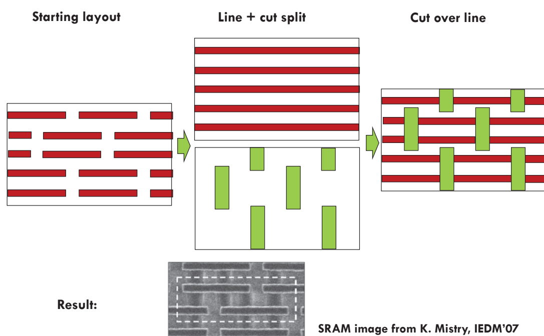



A.Kahng, ICCAD'03

## Litho (6): Double Patterning

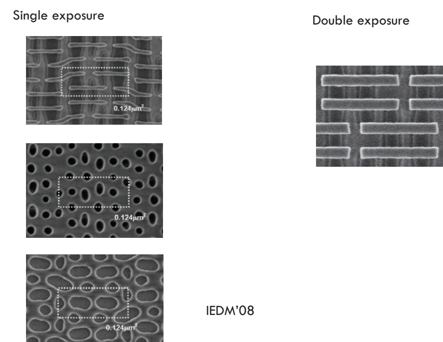
- Double exposure double etch
  - Double exposure double etch
  - Pitch split, litho-etch-litho-etch (LELE)
- Self-aligned methods
  - Self-aligned double patterning
  - Self-aligned quadruple patterning

## Double-Exposure Double-Etch



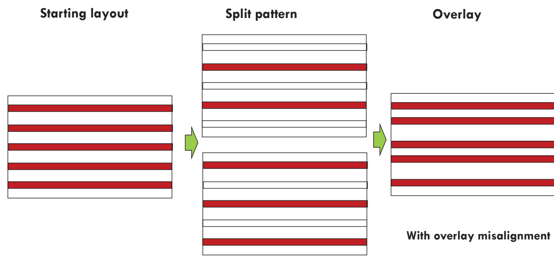

SRAM image from K. Mistry, IEDM'07

## 32nm Examples



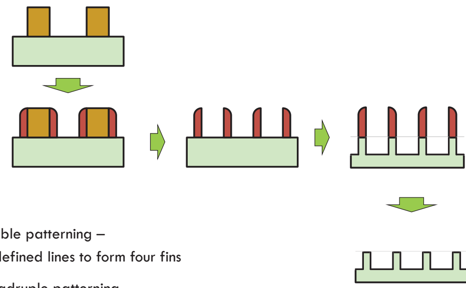

IEDM'08

## Pitch-Split Double Exposure




Also called litho-etch-litho-etch (LELE)

## Self-Aligned Double Patterning (SADP)



- SADP: Double patterning – Two litho-defined lines to form four fins
- SAQP: Quadruple patterning

## Litho: Design Implications

- Forbidden directions
  - Depends on illumination type
  - Poly lines in other directions can exist but need to be thicker
- Forbidden pitches
  - Nulls in the interference pattern
  - Multiple patterning
- Forbidden shapes in PSM, multiple-patterning
- Assist features
  - If a transistor doesn't have a neighbor, let's add a dummy

## Litho: Current Options (Beyond 10nm)

- Multiple patterning
  - NA ~ 1.2-1.35
- EUV lithography
  - $\lambda$ = 13.5nm

| Normalized wafer cost adder* | |
|---|---|
| SE | 1 |
| LELE | 2.5 |
| LELELE | 3.5 |
| SADP | 2 |
| SAQP | 3 |
| EUV SE | 4 |
| EUV SADP | 6 |

*TEL™ Internal calculation

Cost adder reduced with increased power/throughput of EUV (EUV SE, EUV SADP)

A. Raley, SPIE'16

## 1.D Modern Bulk/finFET/FDSOI processes

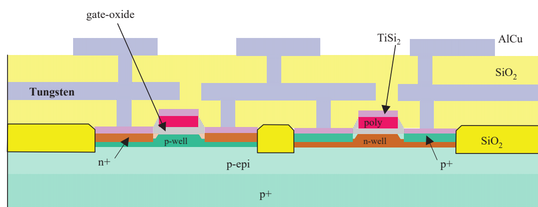


## Some of the Process Features

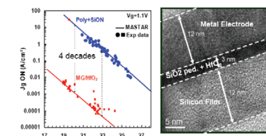
1. Shallow-trench isolation
2. High-k/Metal-gate technology
3. Strained silicon
4. Thin-body devices (28nm, and beyond)
5. Copper interconnects with low-k dielectrics

## 1. Shallow Trench Isolation

- Less space needed for isolation
- Some impact on stress

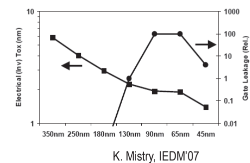



## 2. Hi-k/Metal gate



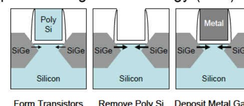

Gate leakage can be improved by 4 decades by using High-K/Metal Gate Stack

TEM X-section of HighK /Metal Gate Stack on FDSOI



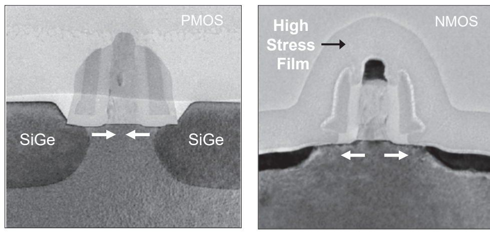

K. Mistry, IEDM'07

Replacement gate technology (Intel)




S. Natarajan, IEDM'08

## 3. Strained Silicon




Compressive channel strain
30% drive current increase
in 90nm CMOS

Tensile channel strain
10% drive current increase
in 90nm CMOS

Intel

## Intel's Strained Si Numbers

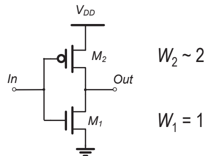
Performance gains:

| | 90 nm | | 65 nm | |
|---|---|---|---|---|
| | NMOS | PMOS | NMOS | PMOS |
| μ | 20% | 55% | 35% | 90% |
| IDSAT | 10% | 30% | 18% | 50% |
| IDLIN | 10% | 55% | 18% | 80% |

S. Thompson, VLSI'06 Tutorial

## Strained Silicon

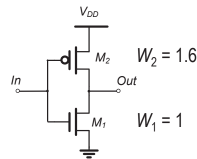
- No strain




$W_2 \sim 2$

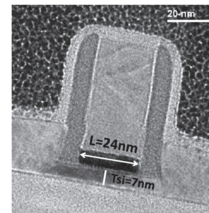
$W_1 = 1$

- Strained Si



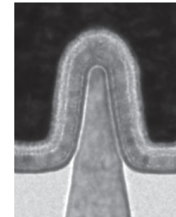

## 5. Thin-Body Devices

- 28nm FDSOI




N. Planes, VLSI'2012

- 22/14nm finFET

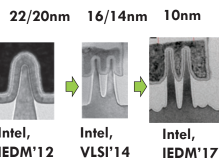


C. Auth, VLSI'2012

## 5. FinFETs

- FinFET scaling

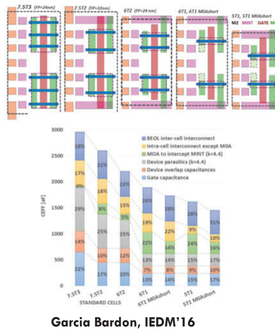
22/20nm 16/14nm 10nm



Intel, IEDM'12 | Intel, VLSI'14 | Intel, IEDM'17

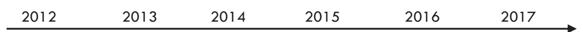
- N-P spacing

- Track scaling



Garcia Bardon, IEDM'16

## 5. FDSOI



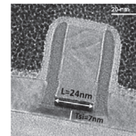

28FDSOI (STMicroelectronics)

28FD-SOI (Samsung)

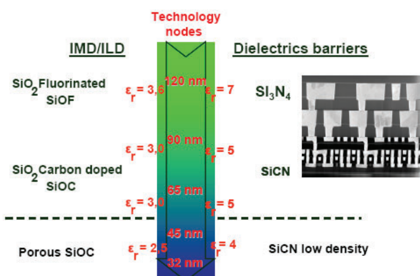
22FDX (GLOBALFOUNDRIES)

12FDX (GLOBALFOUNDRIES)

18FDS (Samsung)



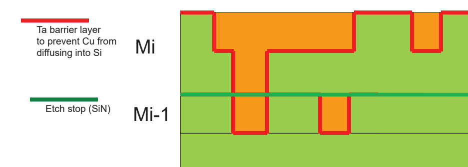
## 5. Interconnect



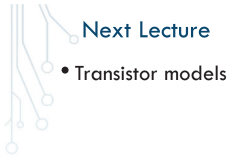

J. Hartmann, ISSCC'07

## Interconnect: CMP

Cu interconnect: Dual damascene process




- Metal density rules (20%-80%)
- Slotting rules
- Also: Antenna rules



## Next Lecture

- Transistor models