inst.eecs.berkeley.edu/~ee241b

EE241B : Advanced Digital Circuits

Lecture 4 – Transistor Models

Borivoje Nikolić

EECS kicks off Berkeley 150W with ten "first" women. In celebration of the anniversary of 150 Years of Women at Berkeley (150W) in 2020, the EECS department will profile a number of remarkable women who have studied or worked here. This month, Berkeley EECS is highlighting ten trailblazing women who were the first to reach important milestones over the past 50 years. Learn how professors Susan Graham, Avideh Zakhor, Shafi Goldwasser and Tsu-Jae King Liu, and alumnae Kawthar Zaki, Carol Shaw, Paula Hawthorn, Barbara Simons, Deborah Estrin, and Susan Eggers, broke through glass ceilings on campus, in their fields, in industry, and in the world..

EECS Website, January 16, 2020.

Announcements

- Homework 1 will be assigned this week

Outline

- Module 2
  - MOS transistor I-V and C-V models

Module 2: Transistor and Gate Models

Module 2 Goals

- Models that traverse design hierarchy
- Start with transistor models
- Gate delay models
- Use models to time the design
- Modeling variability
- Based on 251A, approach
  - Increase accuracy, when needed

2.A MOS Modeling Goals

Device Models

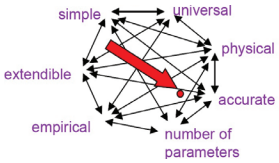
- Transistor models
  - I-V characteristics
  - C-V characteristics
- Interconnect models
  - R, C, L
  - Covered in EE240A

Transistor Modeling

- Different levels:
  - Hand analysis
  - Computer-aided analysis (e.g. Matlab)
  - Switch-level simulation (some flavors of 'fast Spice')
  - Circuit simulation (Hspice)
- These levels have different requirements in complexity, accuracy and speed of computation
- We are primarily interested in delay and energy modeling, rather than current modeling
- But we have to start from the currents…

Transistor Modeling

- DC
  - Accurate I-V equations
  - Well behaved conductance for convergence (not necessarily accurate)
- Transient
  - Accurate I-V and Q-V equations
  - Accurate first derivatives for convergence
  - Conductance, as in DC
- Physical vs. empirical



from BSIM group

Goal for Today

- Develop velocity-saturated model for I_{on} and apply it to sizing and delay calculation
  - Similar approach as in 251A, just use an analytical model

Transistor I-V Modeling

- BSIM
  - Superthreshold and subthreshold models
  - Need smoothening between two regions
- EKV/PSP
  - One continuous model based on channel surface potential

2.B Long-Channel MOS On-Current

MOS I-V (BSIM)

Start with the basics:

$I_{DS} = WC_{ox}(V_{GS} - V_{Th} - V_C(x))\,\mu E$

MOS I-V (BSIM)

Start with the basics:

$I_{DS} = WC_{ox}(V_{GS} - V_{Th} - V_C(x))\,\mu E$

$I_{DS} = WC_{ox}(V_{GS} - V_{Th} - V_C(x))\,\mu(dV_C(x)/dx)$

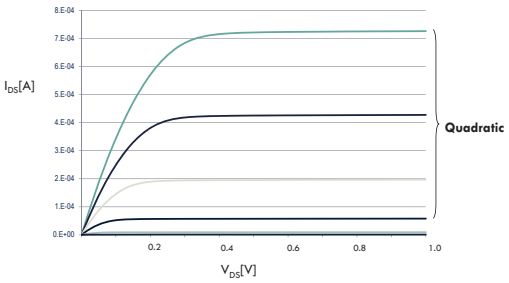
- When integrated over the channel:

$$I_{DS} = \frac{W}{L}\mu C_{ox}\left(V_{GS} - V_{Th} - \frac{V_{DS}}{2}\right)V_{DS}$$

Transistor saturates when $V_{GD} = V_{Th}$, - the channel pinches off at drain's side.

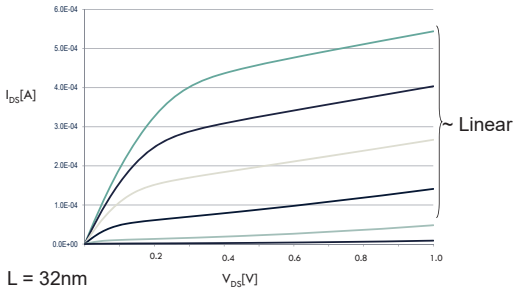
$$I_{DS} = \frac{W}{2L}\mu C_{ox}(V_{GS} - V_{Th})^2$$

MOS Currents (32nm CMOS with L>>1µm)



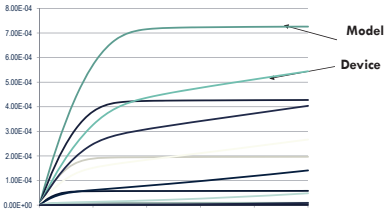
Currents according to the quadratic model
Correct for long channel devices (L ~ µm)

Simulated 32nm Transistor



L = 32nm

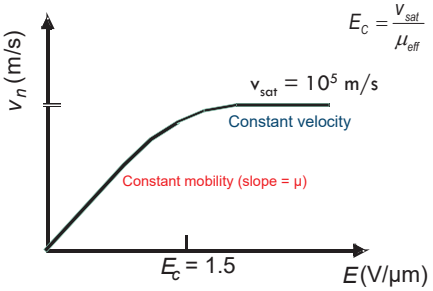
Simulation vs. Model



Major discrepancies:
- shape
- saturation points
- output resistances

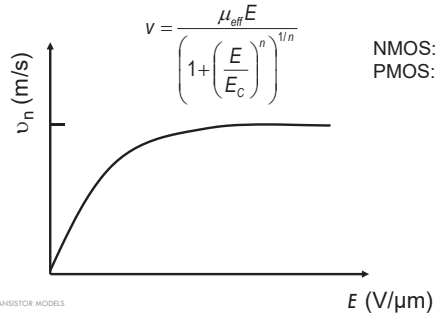
2.C Velocity Saturation

Velocity Saturation



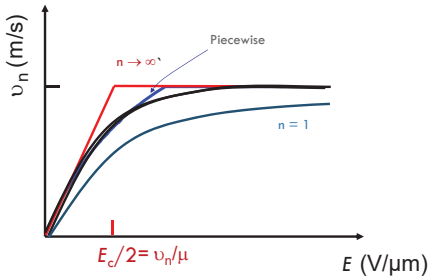
Modeling Velocity Saturation

- Fit the velocity-dependence curve



Modeling Velocity Saturation

- A few approximations: (a) n → ∞, (b) n = 1, (c) piecewise



2.D Short-Channel MOS On-Current

Approximation $n \to \infty$

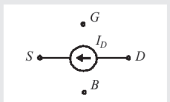
1) $v = \mu_{eff} E$, $E < E_C$ $\quad I_{DS} = \mu C_{ox} \frac{W}{L}\left((V_{GS} - V_{Th})V_{DS} - \frac{V_{DS}^2}{2}\right)$

2) $v = v_{sat}$, $\quad E > E_c$ $\quad I_{Dsat} = \mu C_{ox} \frac{W}{L}\left((V_{GS} - V_{Th})V_{Dsat} - \frac{V_{Dsat}^2}{2}\right)$

$V_{Dsat} = ?$

Can be reduced to Rabaey DIC model by V_{Dsat} = const

MOS Models



$I_D = 0$ for $V_{GT} \le 0$

$I_D = k'\frac{W}{L}\left(V_{GT}V_{min} - \frac{V_{min}^2}{2}\right)(1 + \lambda V_{DS})$ for $V_{GT} \ge 0$

with $V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT})$,

$V_{GT} = V_{GS} - V_T$,

and $V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$

γ - body effect parameter

From Rabaey, 2nd ed.

Unified MOS Model

- Model presented is compact and suitable for hand analysis.
- Still have to keep in mind the main approximation: that V_{DSat} is constant . When is it going to cause largest errors?
  - When does *E* scale? – Transistor stacks.
- But the model still works fairly well.
  - Except for stacks

Approximation $n = 1$, piecewise

- $n = 1$ is solvable, piecewise closely approximates

$$v = \begin{cases} \dfrac{\mu_{eff} E}{1 + E/E_0}, & E < E_0 = \dfrac{2v_{sat}}{\mu_{eff}} \\ v_{sat}, & E > E_0 \end{cases}$$

Sodini, Ko, Moll, TED'84
Toh, Ko, Meyer, JSSC'88
BSIM model

Drain Current

- We can find the drain current by integrating $I_{DS} = WC_{ox}(V_{GS} - V_{Th} - V_C(x))\, v$

$$I_{DS} = \frac{\mu C_{ox}}{1 + (V_{DS}/E_C L)} \frac{W}{L} \left((V_{GS} - V_{Th}) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

- In saturation:

$$I_{DSat} = C_{ox} W v_{sat} (V_{GS} - V_{Th} - V_{Dsat})$$

$$I_{Dsat} = \frac{\mu C_{ox}}{1 + (V_{Dsat}/E_C L)} \frac{W}{L} \left((V_{GS} - V_{Th}) V_{Dsat} - \frac{V_{Dsat}^2}{2} \right)$$

Drain Current in Velocity Saturation

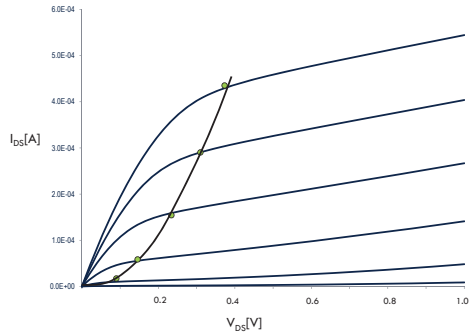
- Solving for V_{Dsat}

$$V_{DSat} = \frac{(V_{GS} - V_{Th}) E_C L}{(V_{GS} - V_{Th}) + E_C L}$$

- And saturation current

$$I_{DSat} = \frac{W}{L} \frac{\mu_{eff} C_{ox} E_C L}{2} \frac{(V_{GS} - V_{Th})^2}{(V_{GS} - V_{Th}) + E_C L}$$

Velocity Saturation



Velocity Saturation

- $E_C L$ is V_{GS} dependent
- Can calculate V_{DSat} (V_{Th} ~ 0.4V in 32nm)

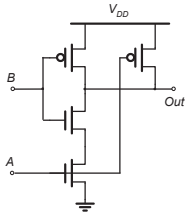
V_{GS} [V]	0.5	0.6	0.7	0.8	0.9	1.0
V_{DSat} [V]	0	0.05	0.11	0.18	0.25	0.33

- For $V_{GS} - V_{Th} << E_C L$, V_{DSat} is close to V_{GS}-V_{Th}
- For large V_{GS}, V_{DSat} bends upwards toward $E_C L$
- Therefore $E_C L$ can be sometimes approximated with a constant term

2.E Application of Models

Application of Models: NAND Gate

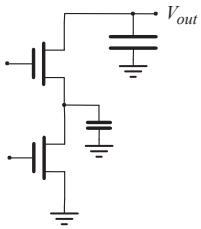
- 2-input NAND gate



Sizing for equal transistions:
- P/N ratio (β-ratio) of 1 in < 22nm, 1.6 >22nm
- Upsizing stacks by a factor proportional to the stack height

Transistor Stacks

- With transistor stacks, V_{DS}, V_{GS} reduce.
- Unified model assumes V_{DSat} = const.
- For a stack of two, appears that both have exactly double R_{ekv} of an inverter with the same width
- Therefore, doubling the size of each, should make the pull down *R* equivalent to an inverter



Velocity Saturation

- As $(V_{GS}-V_{Th})/E_CL$ changes, the depth of saturation changes

$$I_{DSat} = \frac{W}{L}\frac{\mu_{eff}C_{ox}E_CL}{2}\frac{(V_{GS}-V_{Th})^2}{(V_{GS}-V_{Th})+E_CL}$$

- For V_{GS}, V_{DS} = 1.0V, E_CL is ~0.75V
- With double length, E_CL is 1.5V (in this model)
- Stacked transistors are less saturated
- $V_{GS}-V_{Th}$ = 0.6V, I_{DSat} ~ 2/3 of inverter I_{DSat} (64%)
- Therefore NAND2 should have pull-down sized 1.5X
- Check any library NAND2's

Examples

Note about FinFETs

- Widths are quantized