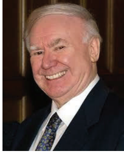
EE241B : Advanced Digital Circuits

Lecture 5 – Leakage, Delay Models

Borivoje Nikolić



The passing of Barrie Gilbert (1937-2020). He was well known for his invention of numerous analog circuit concepts, holding over 100 patents worldwide, and for the discovery of the Translinear Principle. His name is attributed to a class of related topologies loosely referred to as the Gilbert cell, one of which is a mixer - a key frequency translation device - used in every modern wireless communication device.

Announcements

- Homework 1 posted today, due in 2 weeks

Outline

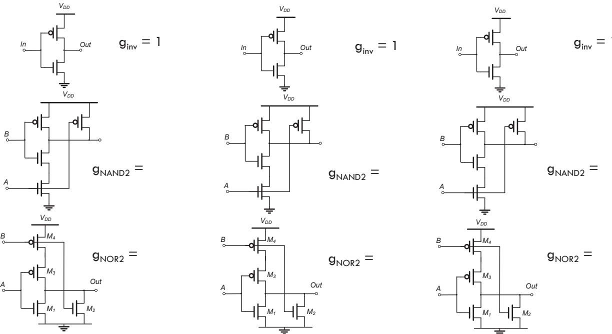
- Module 2
  - MOS transistor leakage
  - C-V models
  - Delay revisited

Recap last lecture

- Scaled transistors are different that the ones in textbooks
- But the same principles still apply
- Sizing:
  - P/N ratio is set by mobilities
    - Mobility enhancements are more effective on PMOS devices
    - ~1:1 in sub 16nm
  - Stack sizing set by velocity saturation
  - Stack of 2 reduces NMOS current by ~2/3
    - PMOS depends on the degree of saturation, also ~2/3 in sub 16nm

Recap last lecture: Logical Effort

- Older CMOS (>1μm)
- Planar CMOS (~28nm, bulk, FDSOI)
- FinFET (16nm-7nm)



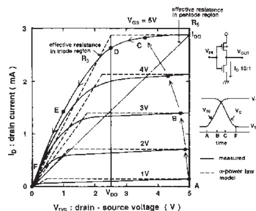
2.E Other Velocity Saturation Models

Other Models: Alpha Power Law Model

- Simple model, sometimes useful for hand analysis

$$I_{DS} = \frac{W}{2L}\mu C_{ox}(V_{GS} - V_{Th})^{\alpha}$$

Parameter α is between 1 and 2.



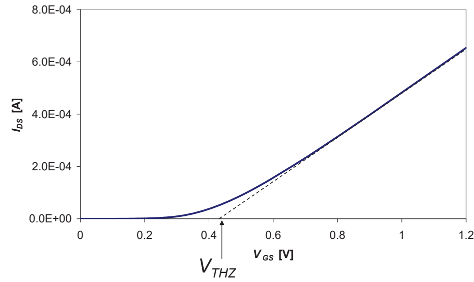
Sakurai, Newton, JSSC 4/90

Alpha Power Law Model

- This is not a physical model
- Simply empirical:
  - Can fit (in minimum mean squares sense) to variety of α's, V_{Th}
  - Need to find one with minimum square error – fitted V_{Th} can be different from physical
  - Can also fit to α = 1
    - What is V_{Th}?

$K(V_{GS} - V_{THZ})$ Model ($\alpha = 1$)

Drain current vs. gate-source voltage



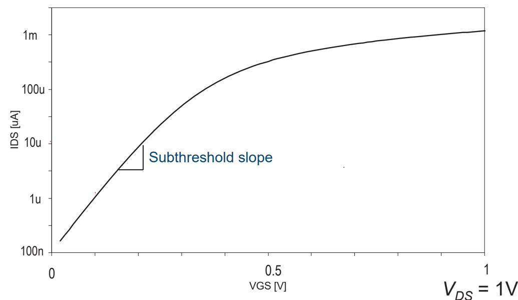
Saturation Currents

Model	Usage
$I_{DS} = K\frac{W}{L}(V_{GS} - V_{THZ})$	Delay estimates with $V_{DD} >> V_{TH}$
$I_{DS} = \frac{W}{L}\frac{\mu C_{ox}}{2}(V_{GS} - V_{TH})^2$	Long channel devices (rare in digital)
$I_{DS} = \frac{W}{L}\frac{\mu C_{ox}}{2}(V_{GS} - V_{TH})^\alpha$	Delay estimates in a wider range of V_{DD}'s
$I_{DS} = \frac{W}{L}\mu C_{ox}\left((V_{GS} - V_{TH})V_{Dsat} - \frac{V_{Dsat}^2}{2}\right)$	Easy to remember, does not handle stacks correctly
$I_{DS} = \frac{W}{L}\frac{\mu C_{ox}}{2}\frac{E_C L (V_{GS} - V_{TH})^2}{(V_{GS} - V_{TH}) + E_C L}$	Handles stacks correctly, sizing

2.F Transistor Leakage

Transistor Leakage

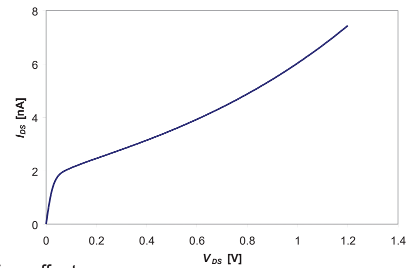
Transistor Leakage



V_{DS} = 1V

Leakage current is exponential with V_{GS}

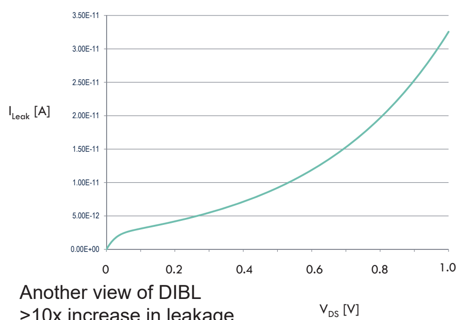
Transistor Leakage (130nm)



Two effects:

- diffusion current (like a bipolar transistor)
- exponential increase with V_{DS} (DIBL)

Transistor Leakage (32nm LP PTM)



Another view of DIBL
>10x increase in leakage

V_{DS} [V]

Subthreshold Current

- Subthreshold behavior can be modeled physically

$$I_{ds,subth} = \mu_{eff} C_{ox} \frac{W}{L}(m-1)\left(\frac{kT}{q}\right)^2 e^{\frac{V_{GS}-V_{Th}}{mkT/q}}\left(1 - e^{-\frac{Vds}{kT/q}}\right)$$

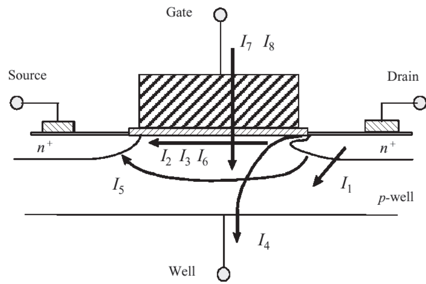
$$m = 1 + \frac{C_{dm}}{C_{ox}} \quad \text{(m ~ 1.1-1.4)}$$

Taur, Ning, Modern VLSI Devices

Or (approx):

$$I_{ds,subth} = I_0 \frac{W}{W_0} 10^{\frac{(V_{gs}-V_{Th})+\gamma V_{ds}}{S}} \qquad S = 2.3m\frac{kT}{q}$$

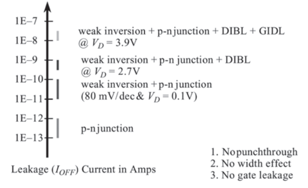
Leakage Components



Courtesy of IEEE Press, New York. © 2000

Leakage Components (250nm)

1. pn junction reverse bias current
2. Weak inversion
3. Drain-induced barrier lowering (DIBL)
4. Gate-induced drain leakage (GIDL)
5. Punchthrough
6. Narrow width effect
7. Gate oxide tunneling
8. Hot carrier injection



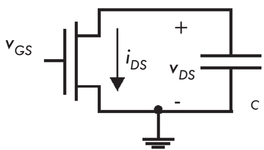
Leakage Components

- Drain-induced barrier lowering (DIBL)
  - Voltage at the drain lowers the source potential barrier
  - Lowers V_{Th}, no change on S
- Gate-induced drain leakage (GIDL)
  - High field between gate and drain increases injection of carriers into substrate -> leakage
    (band-to-band leakage)

2.H Transistor C-V

MOS Transistor as a Switch

Discharging a capacitor



- Can solve:

$$i_{DS} = i_{DS}(v_{DS})$$

$$i_{DS} = C(v_{DS})\frac{dv_{DS}}{dt}$$

- Prefer using equivalent resistances
- Find t_{pHL}
- Find equivalent C, R

$$t_{pHL} = \int \frac{C(v_{DS})dv_{DS}}{i_{DS}(v_{GS}, v_{DS})}$$

MOS Capacitances

- Gate capacitance
  - Non-linear channel capacitance
  - Linear overlap, fringing capacitances
  - Miller effect on overlap, fringing capacitance
- Non-linear drain diffusion capacitance
  - PN junction
- Wiring capacitances
  - Linear

Gate and Drain Capacitances

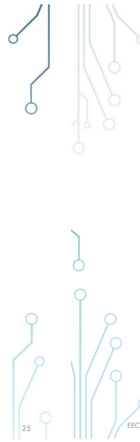
Gate capacitance

Drain capacitance

Gate Capacitances

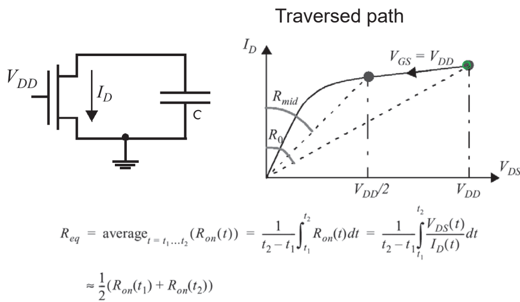
Gate Capacitances

- Gate capacitance is non-linear
  - First order approximation with $C_{ox}WL$ ($C_{ox}L$ = 2fF/μm)
- Need to find the actual equivalent capacitance by simulating it
- Since this is a linear approximation of non-linear function, it is valid only over the certain range
  - Different capacitances for HL, LH transitions and power computation
- Drain capacitance non-linearity compensates
  - But this changes with fanout



2.I Delay Revisited

MOS Transistor as a Switch (EECS251A)



$$R_{eq} = \text{average}_{t=t_1...t_2}(R_{on}(t)) = \frac{1}{t_2-t_1}\int_{t_1}^{t_2} R_{on}(t)dt = \frac{1}{t_2-t_1}\int_{t_1}^{t_2} \frac{V_{DS}(t)}{I_D(t)}dt$$

$$\approx \frac{1}{2}(R_{on}(t_1) + R_{on}(t_2))$$

MOS Transistor as a Switch (EE241A)

Solving the integral:

$$R_{eq} = \frac{1}{-V_{DD}/2}\int_{V_{DD}}^{V_{DD}/2} \frac{V}{I_{DSAT}(1+\lambda V)}dV \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1-\frac{7}{9}\lambda V_{DD}\right)$$

with appropriately calculated I_{dsat}

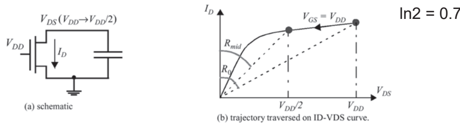
Averaging resistances:

$$R_{eq} = \frac{1}{2}\left(\frac{V_{DD}}{I_{DSAT}(1+\lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT}(1+\lambda V_{DD}/2)}\right) \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1-\frac{5}{6}\lambda V_{DD}\right)$$

CMOS Performance

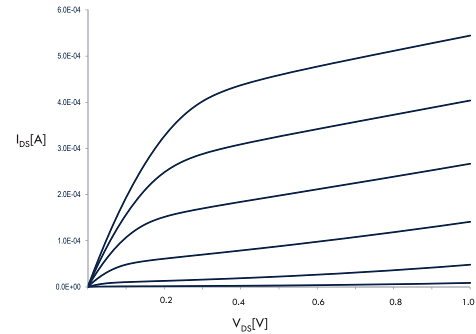
Propagation delay: $t_{pHL} = (\ln 2)R_{eqn}C_L$ $\quad t_{pLH} = (\ln 2)R_{eqp}C_L$

ln2 = 0.7



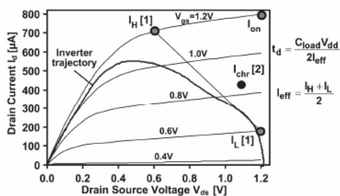
(a) schematic (b) trajectory traversed on ID-VDS curve.

Switching Trajectory



Effective Current

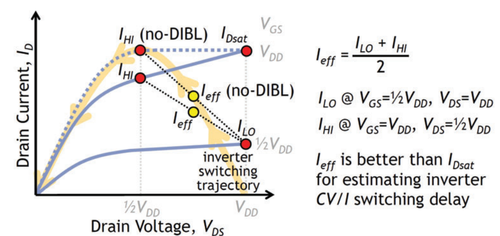
- $I_{on}(V_{DD})$ is never reached
- Define $I_{eff} = (I_H + I_L)/2$
- $I_L = I_{DS}(V_{GS}=V_{DD}/2, V_{DS}=V_{DD})$; $I_H=I_{DS}(V_{GS}=V_{DD}, V_{DS}=V_{DD}/2)$,



Na, IEDM'2002
Von Arnim, IEDM'2007

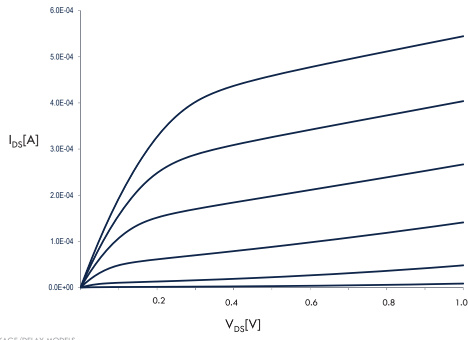
DIBL Matters

- A. Loke, VLSI'16
  - FinFET, FDSOI – less DIBL



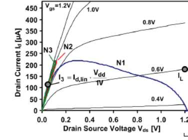
Less DIBL → higher I_{eff} & r_{out} for same I_{Dsat}

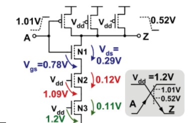
Transistor Stacks



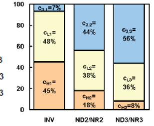
Effective Current in Stacks

- Add linear current, I_3





V_{gs}	V
V_{dd}	$V_{dd}/2$
$V_{dd}/2$	V_{dd}
V_{dd}	$0.05 \cdot V_{dd}$



Model: $I_{stack,i} = c_{H,i} I_H + c_{L,i} I_L + c_{3,i} I_3 \Rightarrow$

Inverter: $I_{stack1} = 0.45 \cdot I_H + 0.48 \cdot I_L + 0.07 \cdot I_3$

NAND2/NOR2: $I_{stack2} = 0.18 \cdot I_H + 0.38 \cdot I_L + 0.44 \cdot I_3$

NAND3/NOR3: $I_{stack3} = 0.08 \cdot I_H + 0.36 \cdot I_L + 0.56 \cdot I_3$

Von Arnim, IEDM'2007

Next Lecture

- Standard Cells