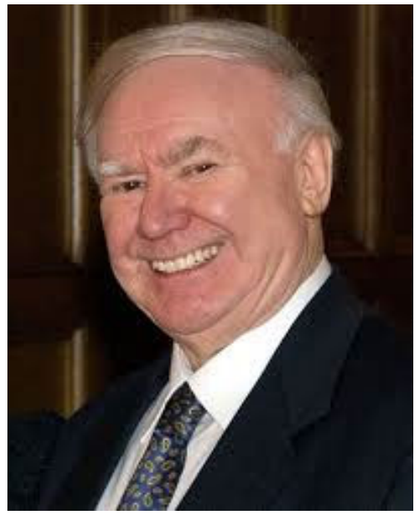
EE241B : Advanced Digital Circuits

Lecture 5 – Leakage, Delay Models

Borivoje Nikolić



The passing of Barrie Gilbert (1937-2020). He was well known for his invention of numerous analog circuit concepts, holding over 100 patents worldwide, and for the discovery of the Translinear Principle. His name is attributed to a class of related topologies loosely referred to as the Gilbert cell, one of which is a mixer - a key frequency translation device - used in every modern wireless communication device.

Announcements

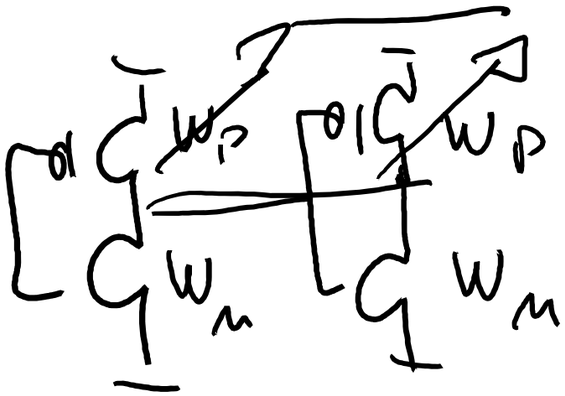
- Homework 1 posted today, due in 2 weeks

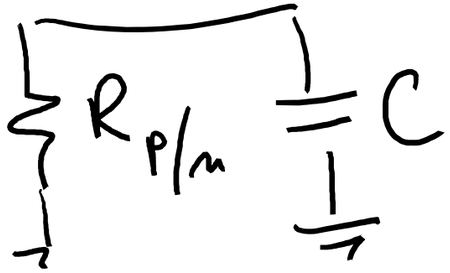
Outline

- Module 2
  - MOS transistor leakage
  - C-V models
  - Delay revisited

Recap last lecture

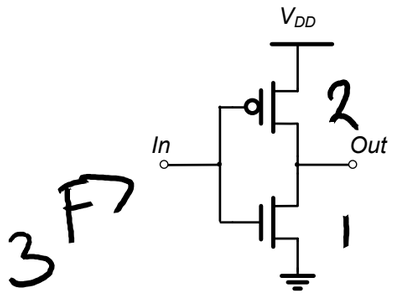
- Scaled transistors are different that the ones in textbooks
- But the same principles still apply
- Sizing:
  - P/N ratio is set by mobilities
    - Mobility enhancements are more effective on PMOS devices
    - ~1:1 in sub 16nm 1 : 0.9
  - Stack sizing set by velocity saturation
  - Stack of 2 reduces NMOS current by ~2/3
    - PMOS depends on the degree of saturation, also ~2/3 in sub 16nm



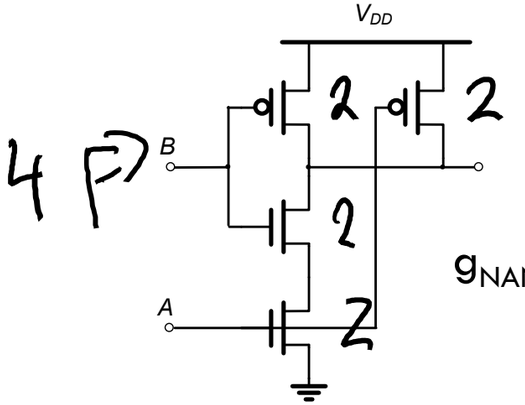


Recap last lecture: Logical Effort

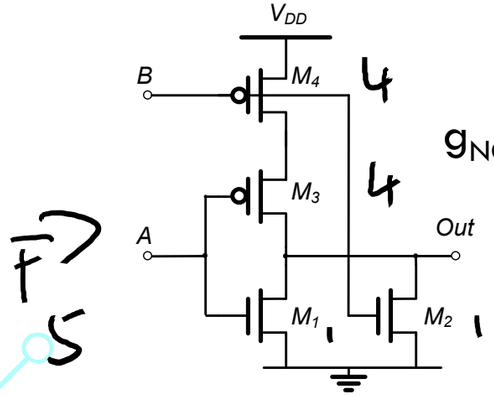
- Older CMOS (>1µm)
- Planar CMOS (~28nm, bulk, FDSOI)
- FinFET (16nm-7nm)



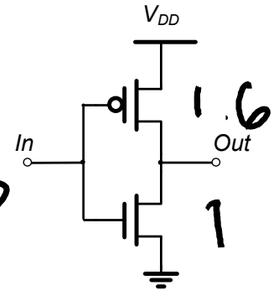
$g_{inv} = 1$



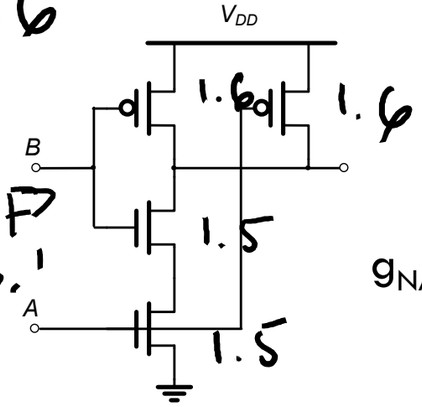
$g_{NAND2} = \frac{4}{3} = 1.33$



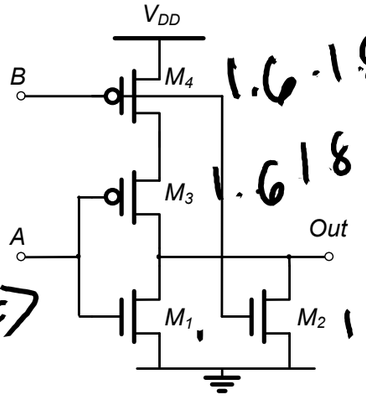
$g_{NOR2} = \frac{5}{3} = 1.67$



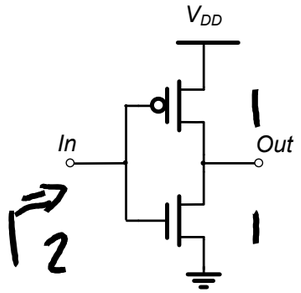
$g_{inv} = 1$



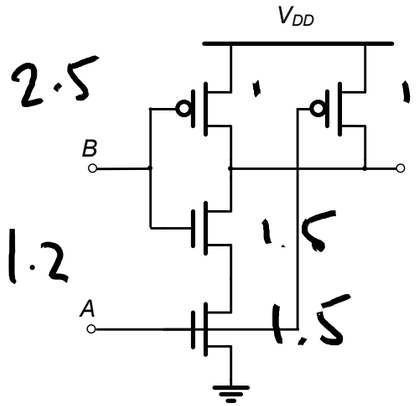
$g_{NAND2} = \frac{3.1}{2.6} = 1.2$



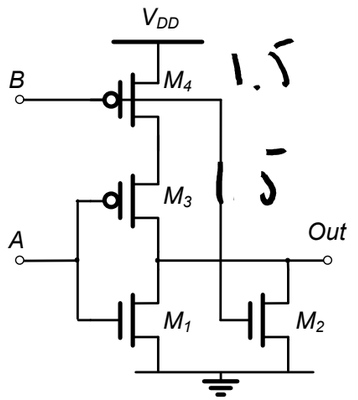
$g_{NOR2} = \frac{3.9}{2.6} = 1.5$



$g_{inv} = 1$



$g_{NAND2} = \frac{2.5}{2} = 1.25$



$g_{NOR2} = \frac{2.5}{2} = 1.25$

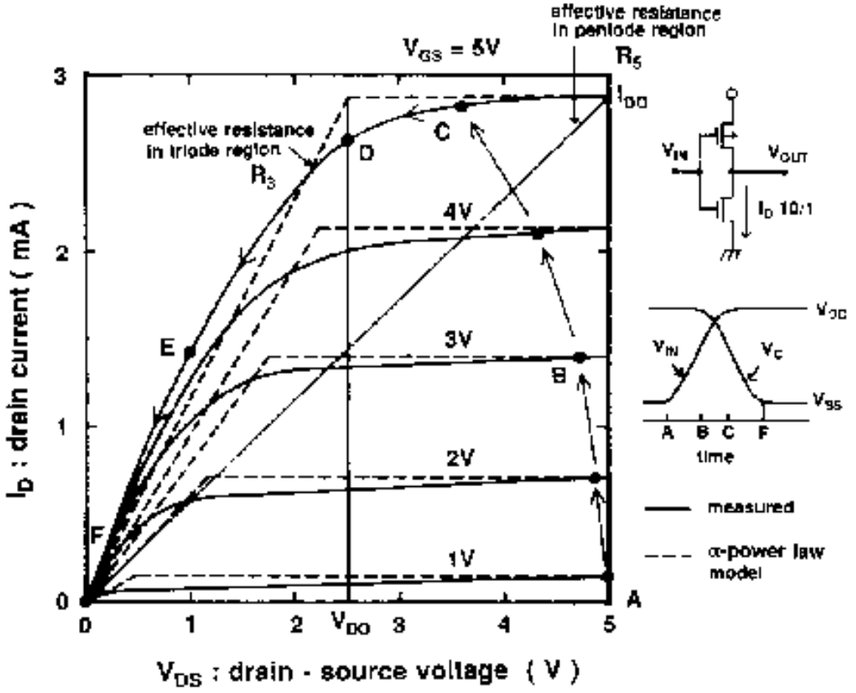
2.E Other Velocity Saturation Models

Other Models: Alpha Power Law Model

- Simple model, sometimes useful for hand analysis

$$I_{DS} = \frac{W}{2L}\mu C_{ox}\left(V_{GS} - V_{Th}\right)^{\alpha}$$

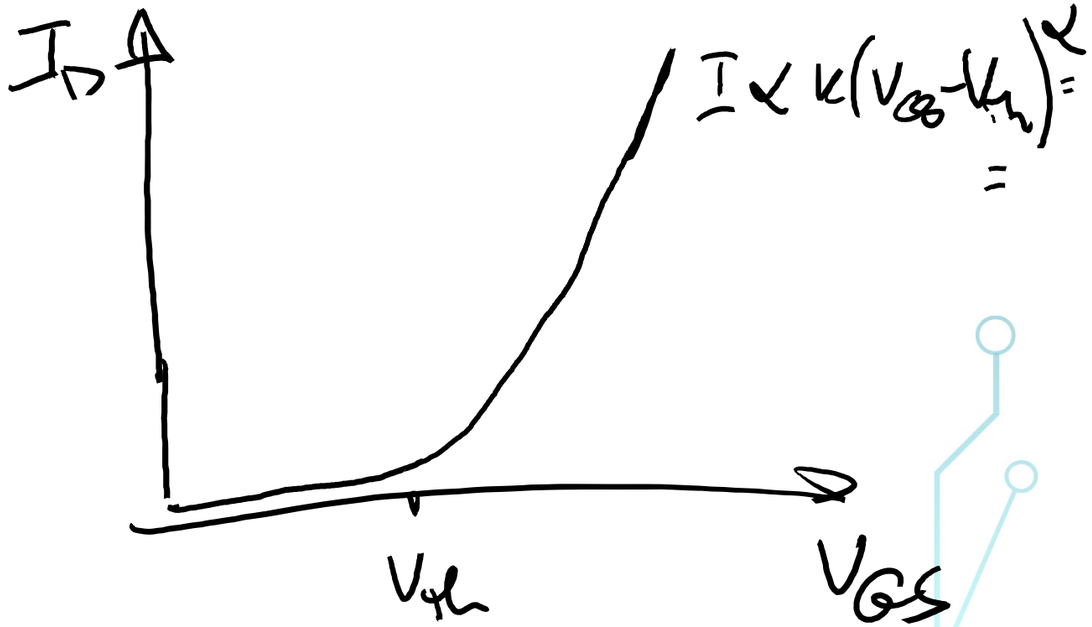
Parameter a is between 1 and 2.



Sakurai, Newton, JSSC 4/90

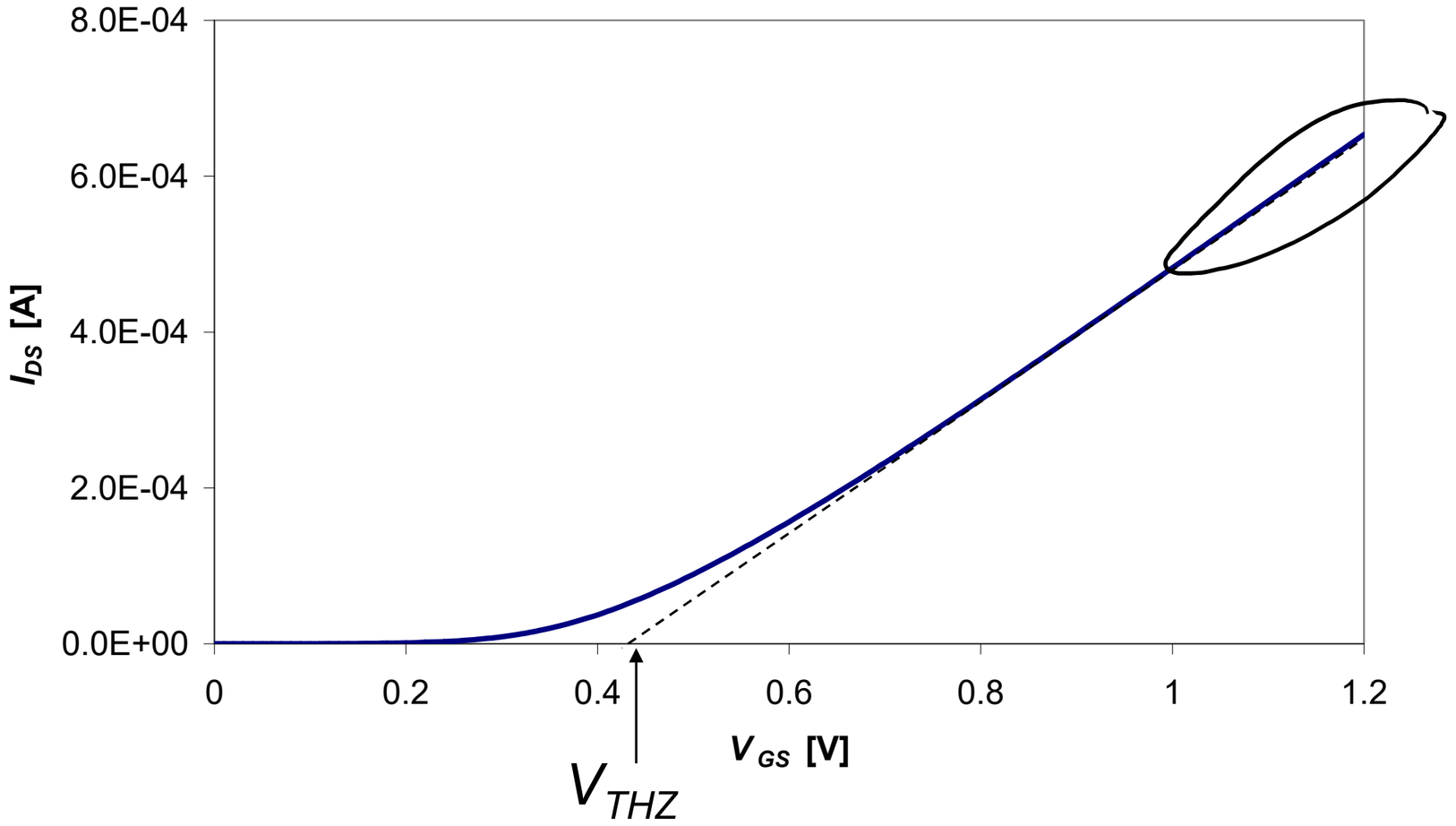
Alpha Power Law Model

- This is not a physical model
- Simply empirical:
  - Can fit (in minimum mean squares sense) to variety of α's, V_{Th}
  - Need to find one with minimum square error – fitted V_{Th} can be different from physical
  - Can also fit to $\alpha = 1$
    - What is V_{Th}?



1: $K(V_{GS} - V_{THZ})$ Model ($\alpha = 1$)

Drain current vs. gate-source voltage (28nm)

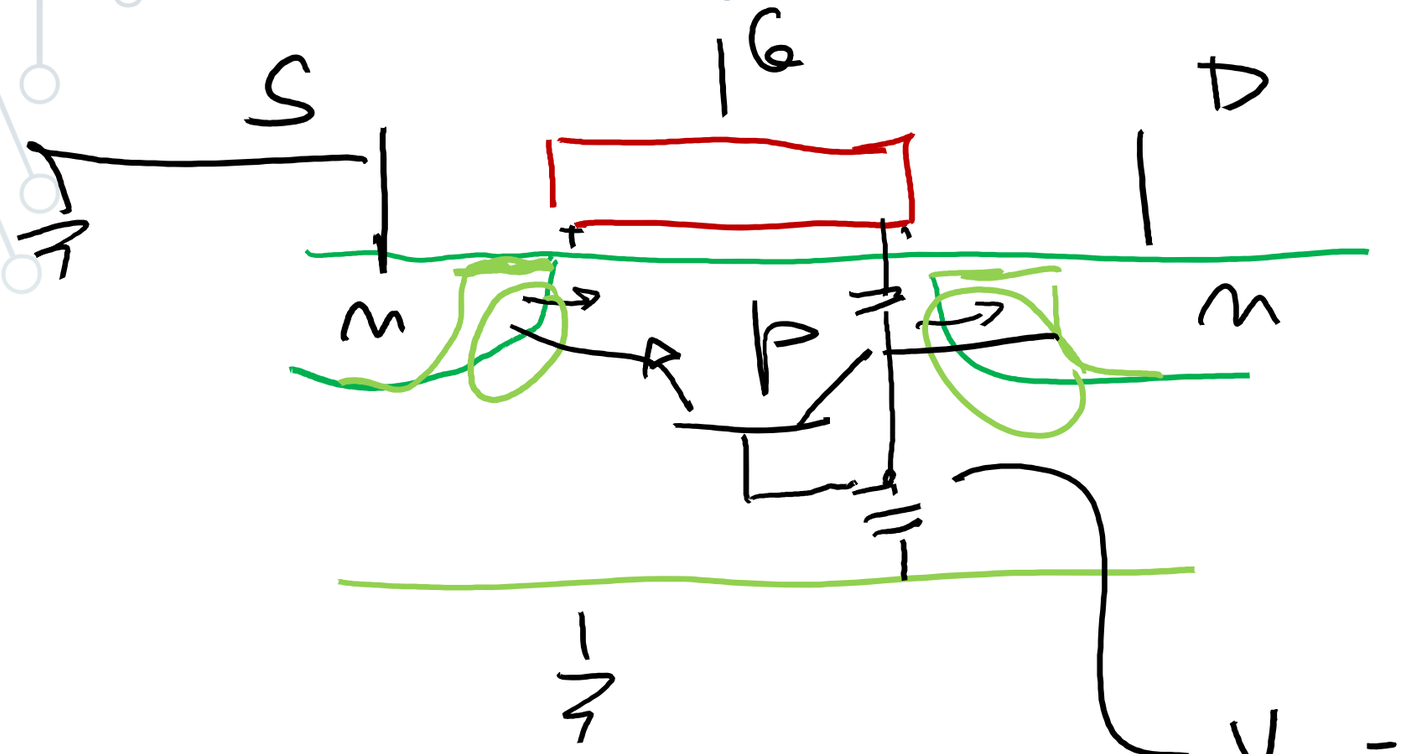


Saturation Currents

Model	Usage
$I_{DS} = K\frac{W}{L}(V_{GS} - V_{THZ})$	Delay estimates with $V_{DD} >> V_{TH}$
$I_{DS} = \frac{W}{L}\frac{\mu C_{ox}}{2}(V_{GS} - V_{TH})^2$	Long channel devices (rare in digital)
$I_{DS} = \frac{W}{L}\frac{\mu C_{ox}}{2}(V_{GS} - V_{TH})^{\alpha}$	Delay estimates in a wider range of V_{DD}'s
$I_{DS} = \frac{W}{L}\mu C_{ox}\left((V_{GS} - V_{TH})V_{Dsat} - \frac{V_{Dsat}^2}{2}\right)$	Easy to remember, does not handle stacks correctly
$I_{DS} = \frac{W}{L}\frac{\mu C_{ox}}{2}\frac{E_C L(V_{GS} - V_{TH})^2}{(V_{GS} - V_{TH}) + E_C L}$	Handles stacks correctly, sizing

2.F Transistor Leakage

Transistor Leakage



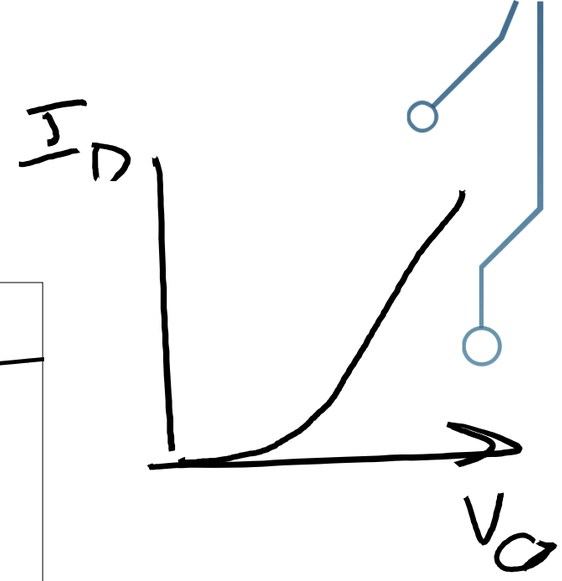
ideal $S = 60\,mV/dec$

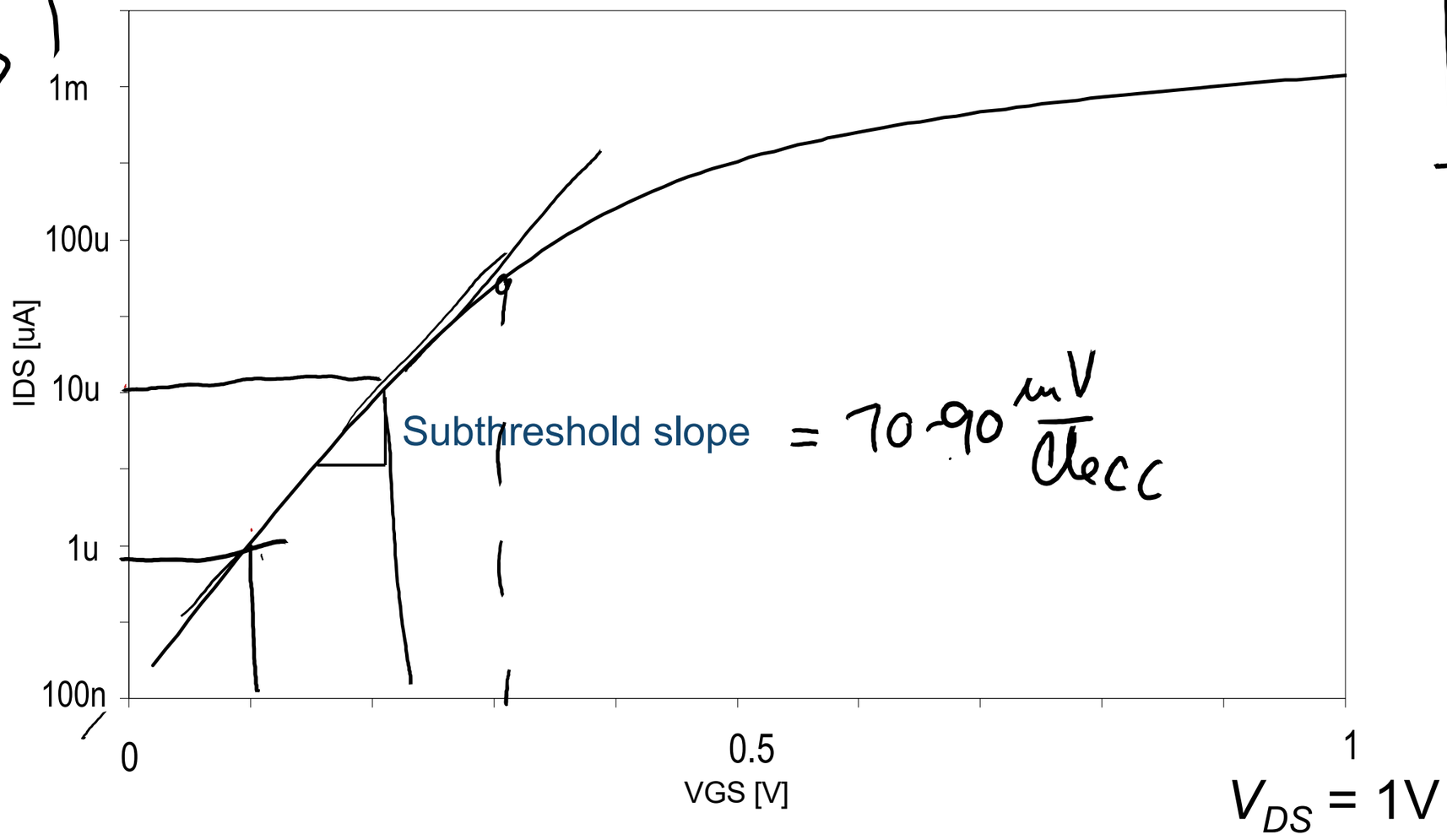
bulk
practical $S = 90\text{-}95\ \frac{mV}{dec}$

Fin FDSOI $S = 70\,mV/dec$

$$V_B = \frac{C_{ox}}{C_{ox} + C_{dm}} V_{GS}$$

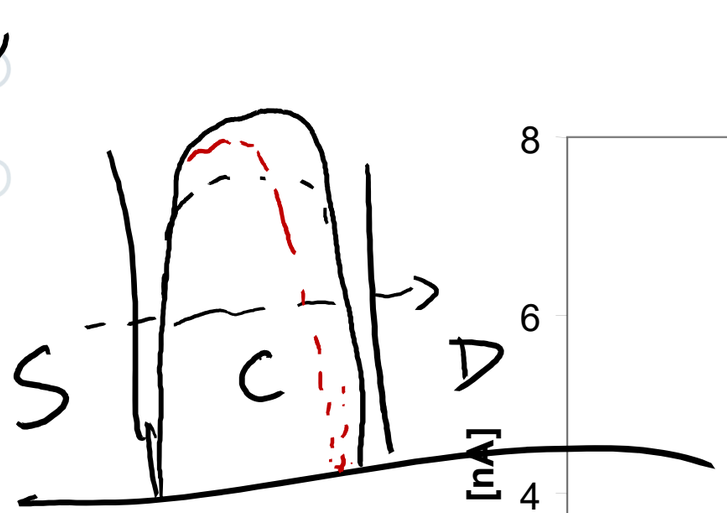
Transistor Leakage

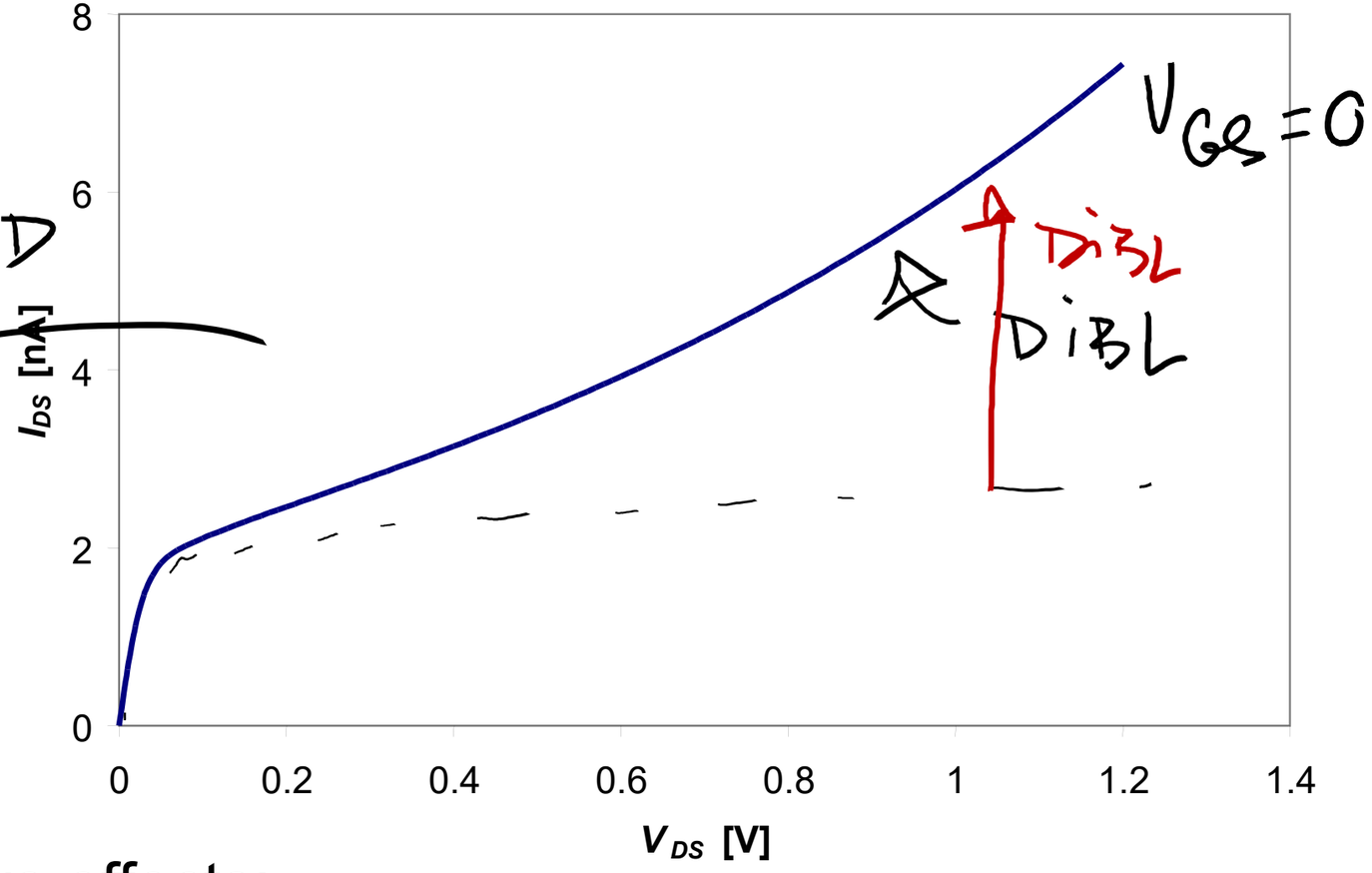


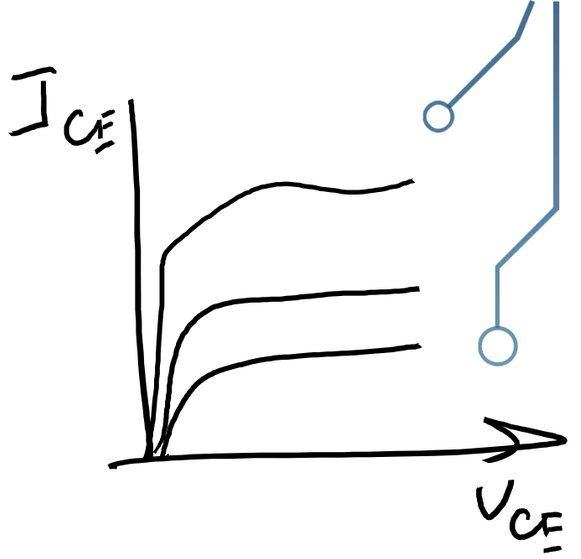


Leakage current is exponential with V_{GS}

Transistor Leakage (130nm)



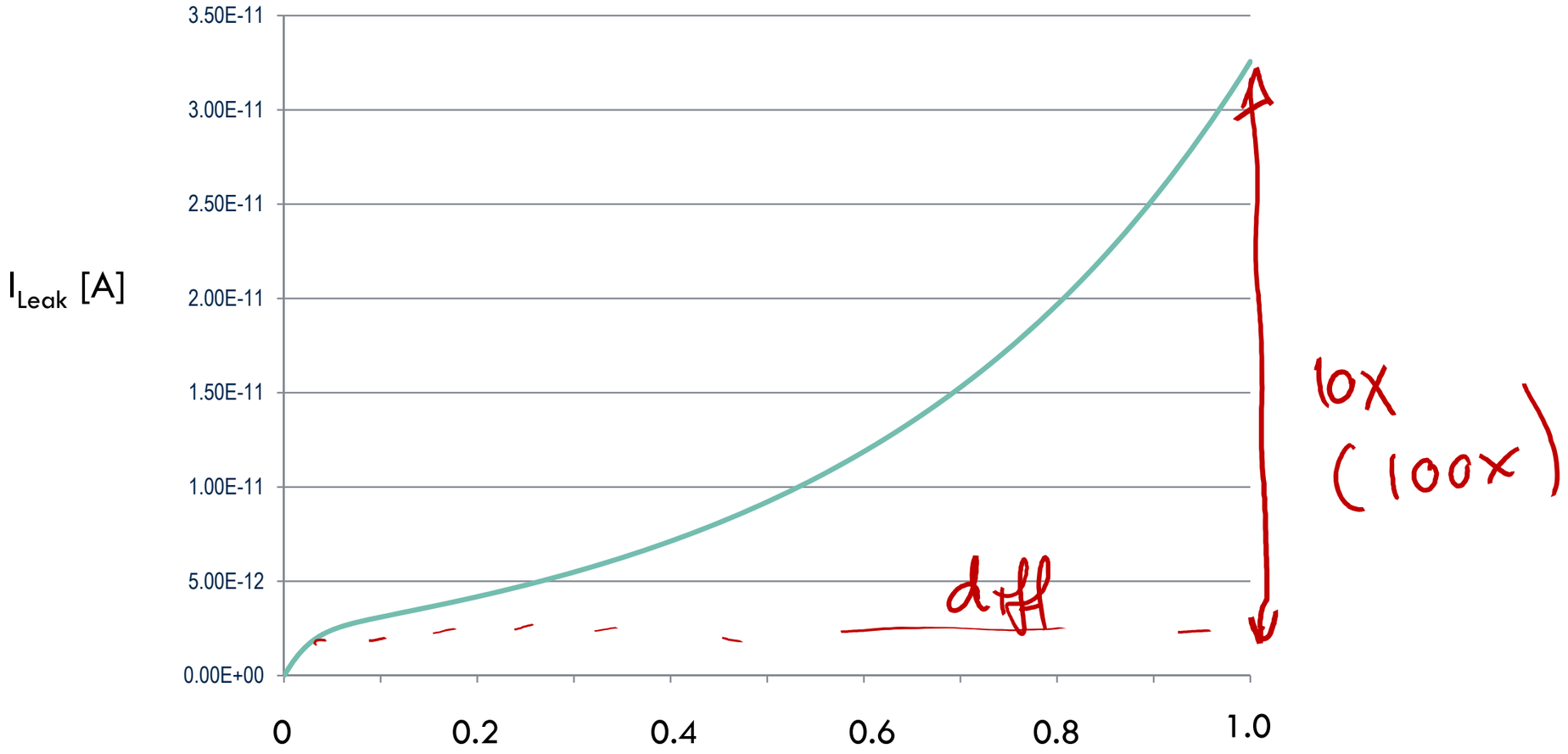




Two effects:

- diffusion current (like a bipolar transistor)
- exponential increase with V_{DS} (DIBL)

Transistor Leakage (32nm LP PTM)



Another view of DIBL
>10x increase in leakage

Subthreshold Current

- Subthreshold behavior can be modeled physically

$$I_{ds,subth} = \mu_{eff} C_{ox} \frac{W}{L}(m-1)\left(\frac{kT}{q}\right)^2 e^{\frac{V_{GS}-V_{Th}}{mkT/q}}\left(1-e^{-\frac{Vds}{kT/q}}\right)$$

$$m = 1+\frac{C_{dm}}{C_{ox}} \quad (\text{m} \sim 1.1\text{-}1.4)$$

BJT

DiBL

DiBL ($\delta < 0.1$)

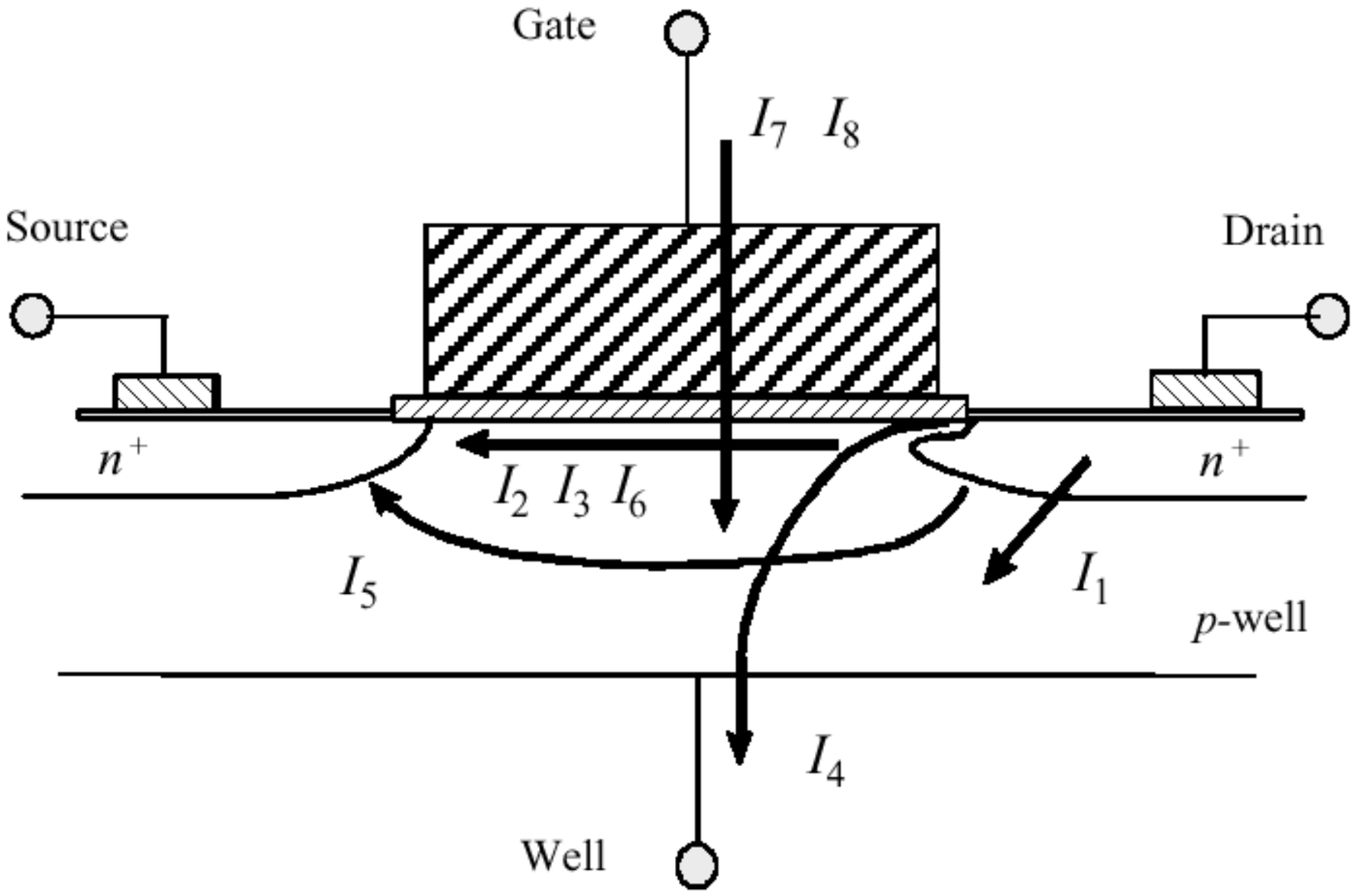
Taur, Ning, Modern VLSI Devices

Or (approx):

$$I_{ds,subth} = I_0 \frac{W}{W_0} 10^{\frac{(V_{gs}-V_{Th})+\gamma V_{ds}}{S}}$$

$$S = 2.3m\frac{kT}{q}$$

Leakage Components



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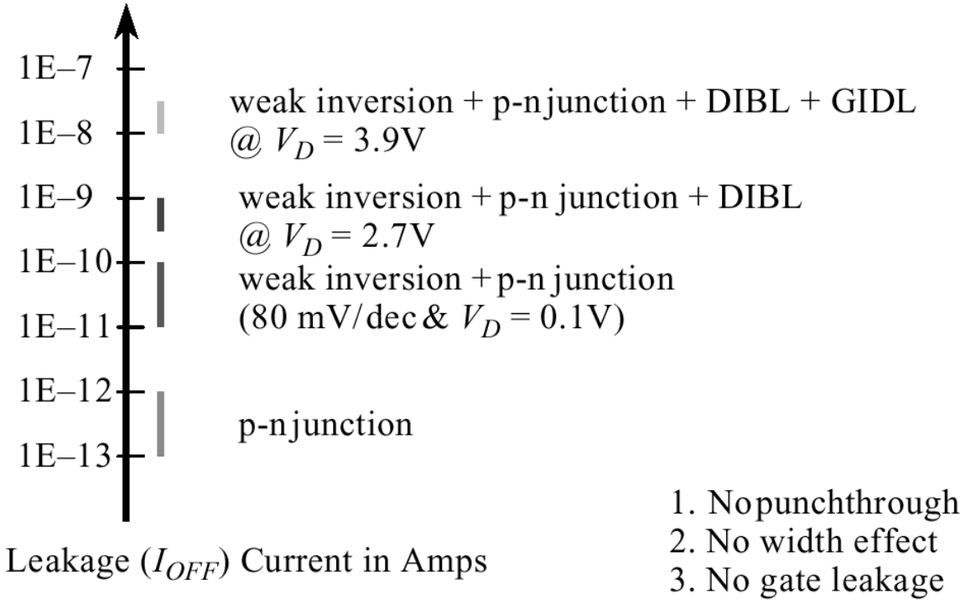
Leakage Components (250nm)

1. pn junction reverse bias current
2. Weak inversion
3. Drain-induced barrier lowering (DIBL)
4. Gate-induced drain leakage (GIDL)
5. Punchthrough
6. Narrow width effect
7. Gate oxide tunneling
8. Hot carrier injection



Leakage Components

- Drain-induced barrier lowering (DIBL)
  - Voltage at the drain lowers the source potential barrier
  - Lowers V_{Th}, no change on S
- Gate-induced drain leakage (GIDL)
  - High field between gate and drain increases injection of carriers into substrate -> leakage
    (band-to-band leakage)

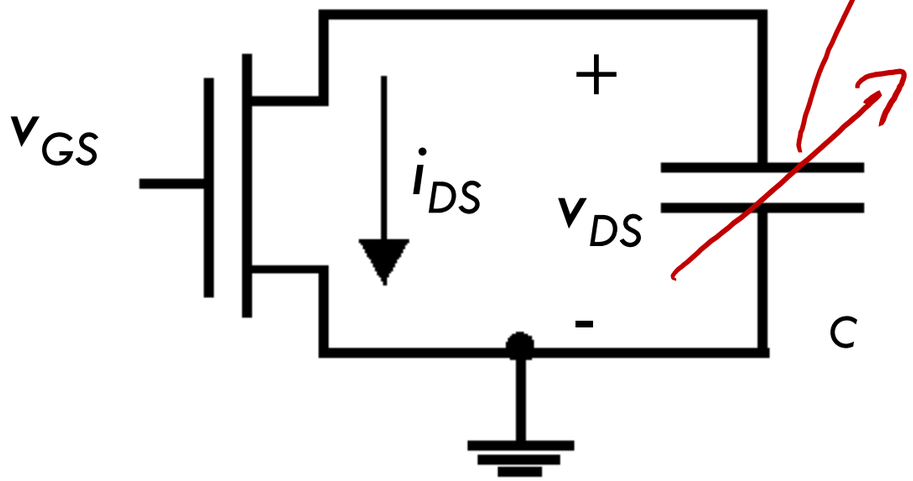
limits substrate bias $V_{BS} < 0$

2.H Transistor C-V

MOS Transistor as a Switch

gdes + wires

Discharging a capacitor



- Can solve:

$$i_{DS} = i_{DS}\left(v_{DS}\right)$$

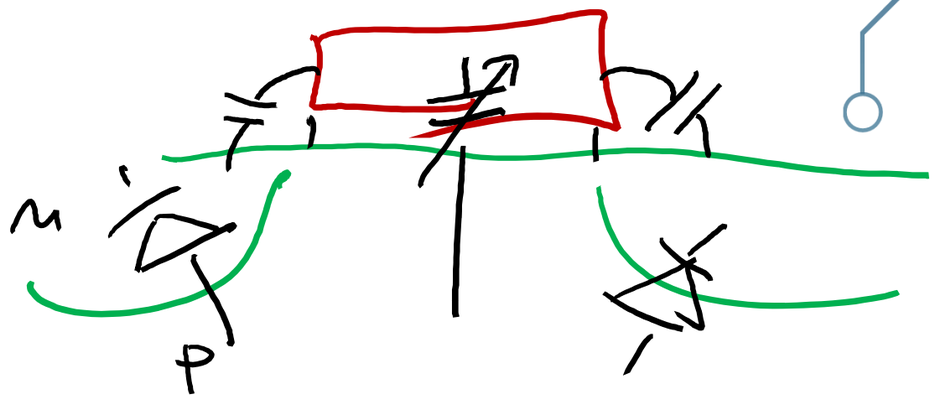
$$i_{DS} = C\left(v_{DS}\right)\frac{dv_{DS}}{dt}$$

- Prefer using equivalent resistances
- Find t_{pHL}
- Find equivalent C, R

$$t_{pHL} = \int \frac{C(v_{DS})\,\mathrm{d}v_{DS}}{i_{DS}\left(v_{GS},v_{DS}\right)}$$

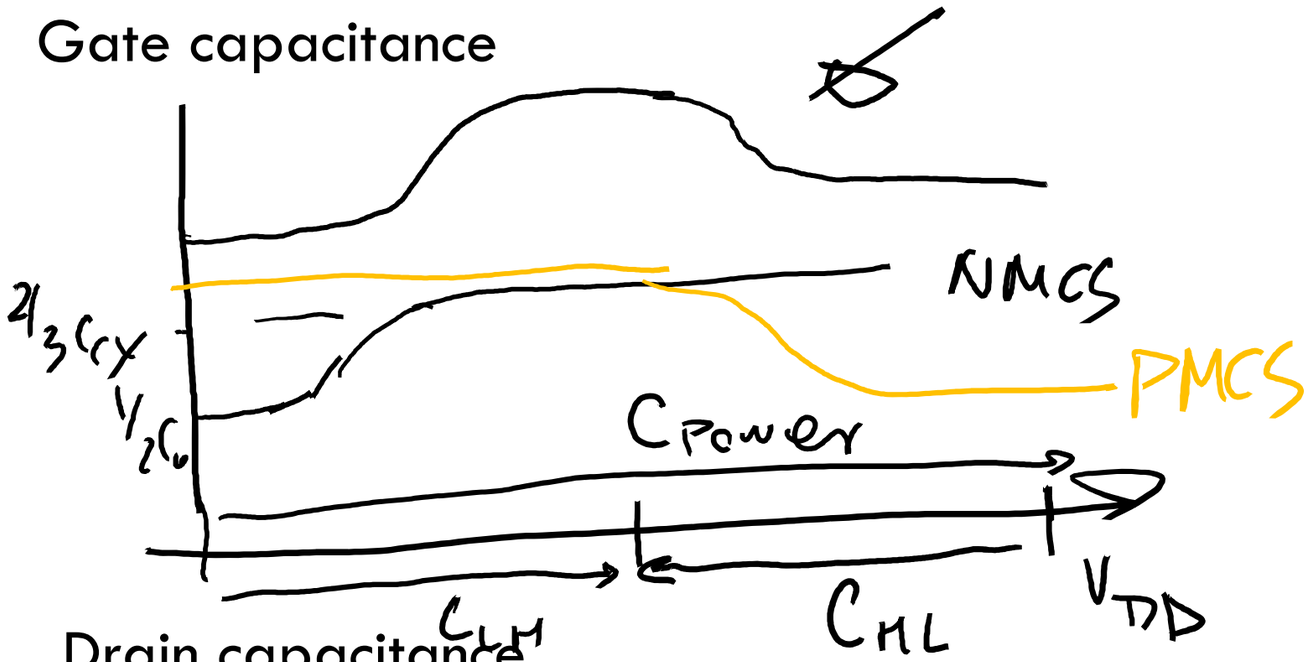
MOS Capacitances

- Gate capacitance
  - Non-linear channel capacitance
  - Linear overlap, fringing capacitances
  - Miller effect on overlap, fringing capacitance
- Non-linear drain diffusion capacitance
  - PN junction
- Wiring capacitances
  - Linear

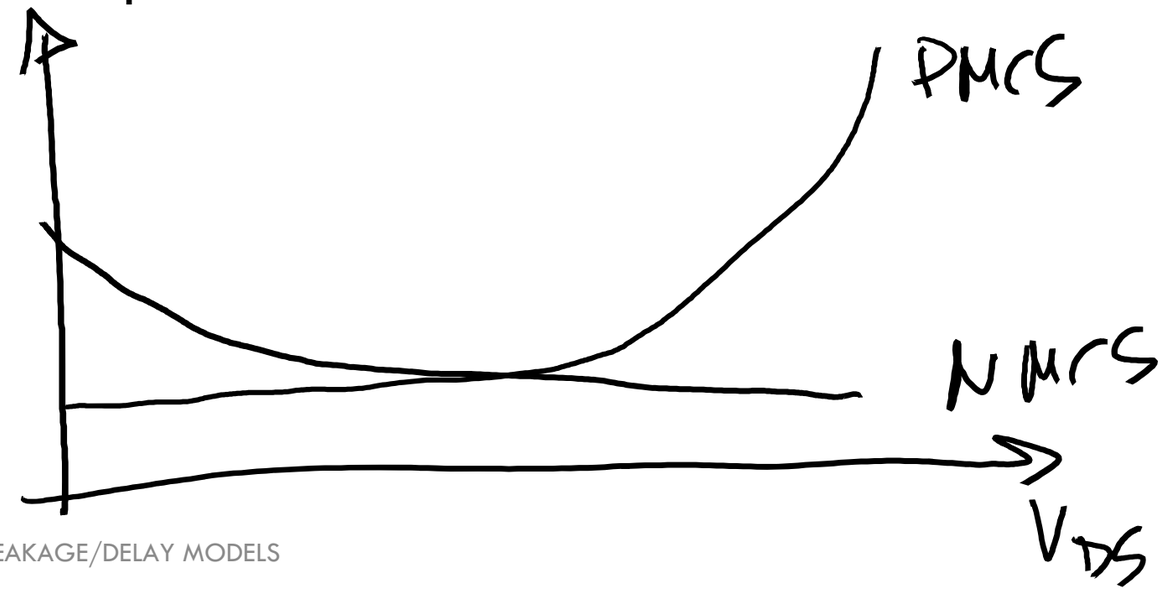


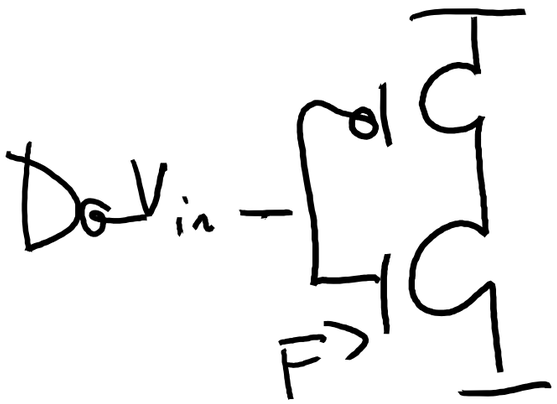
Gate and Drain Capacitances

Gate capacitance



Drain capacitance





$t_{pHL}: V_{DD} - V_{TD2}$

$C_{HL} \neq C_{LH} \neq C_{power}$

$\neq C V_{DD}^2$

P_{av}