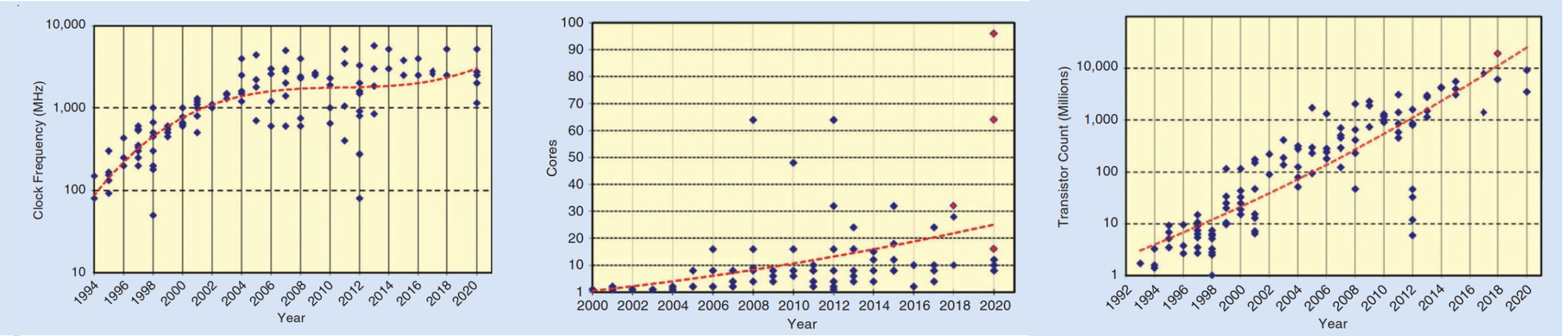
EE241B : Advanced Digital Circuits

Lecture 6 – Standard Cells

Borivoje Nikolić

IEEE International Solid-State Circuits Conference. San Francisco, February 16-21, 2020. Preview in the IEEE Solid-State Circuits Magazine, Winter 2020.



Announcements

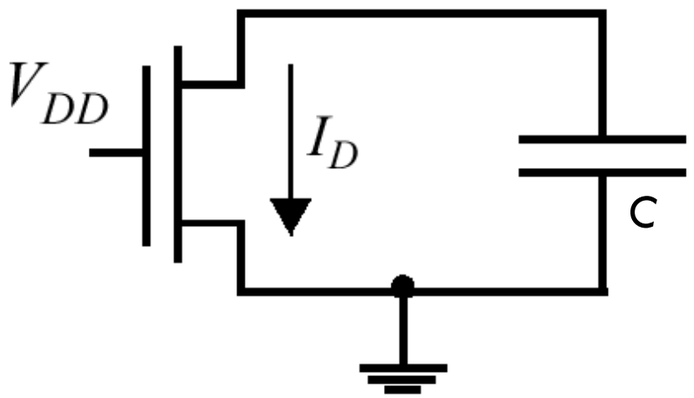
- Homework 1 posted, due on February 17
- No class on February 18 (ISSCC)

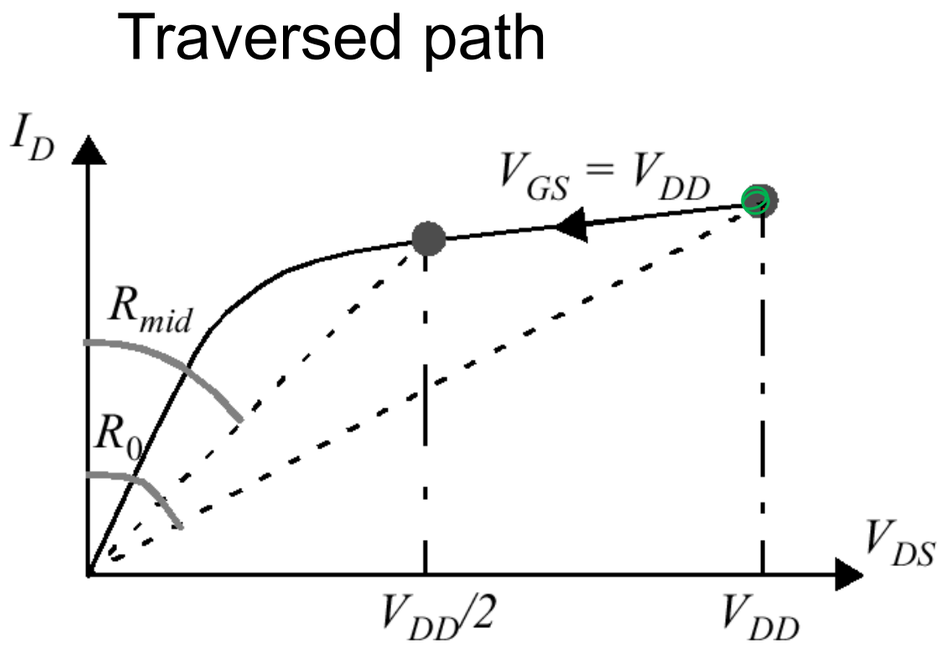
Outline

- Module 2
  - Standard cells
  - Gate delay
  - Design flows

2.1 Delay Revisited

MOS Transistor as a Switch (EECS251A)





$$R_{eq} = \text{average}_{t=t_1 \ldots t_2}(R_{on}(t)) = \frac{1}{t_2 - t_1}\int_{t_1}^{t_2} R_{on}(t)dt = \frac{1}{t_2 - t_1}\int_{t_1}^{t_2} \frac{V_{DS}(t)}{I_D(t)}dt$$

$$\approx \frac{1}{2}(R_{on}(t_1) + R_{on}(t_2))$$

MOS Transistor as a Switch (EE241A)

Solving the integral:

$$R_{eq} = \frac{1}{-V_{DD}/2} \int_{V_{DD}}^{V_{DD}/2} \frac{V}{I_{DSAT}(1+\lambda V)} dV \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1 - \frac{7}{9}\lambda V_{DD}\right)$$

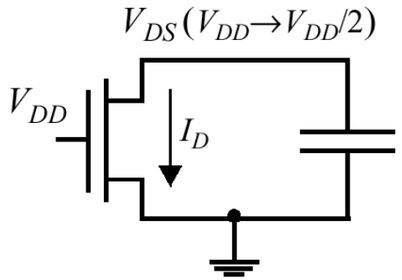
with appropriately calculated I_{dsat}

Averaging resistances:

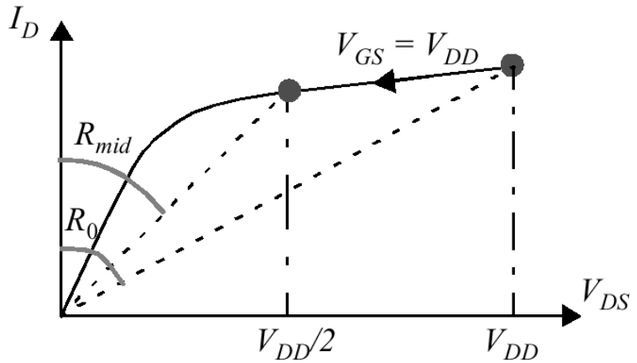
$$R_{eq} = \frac{1}{2}\left(\frac{V_{DD}}{I_{DSAT}(1+\lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT}(1+\lambda V_{DD}/2)}\right) \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1 - \frac{5}{6}\lambda V_{DD}\right)$$

CMOS Performance

Propagation delay: $t_{pHL} = (\ln 2) R_{eqn} C_L \quad t_{pLH} = (\ln 2) R_{eqp} C_L$



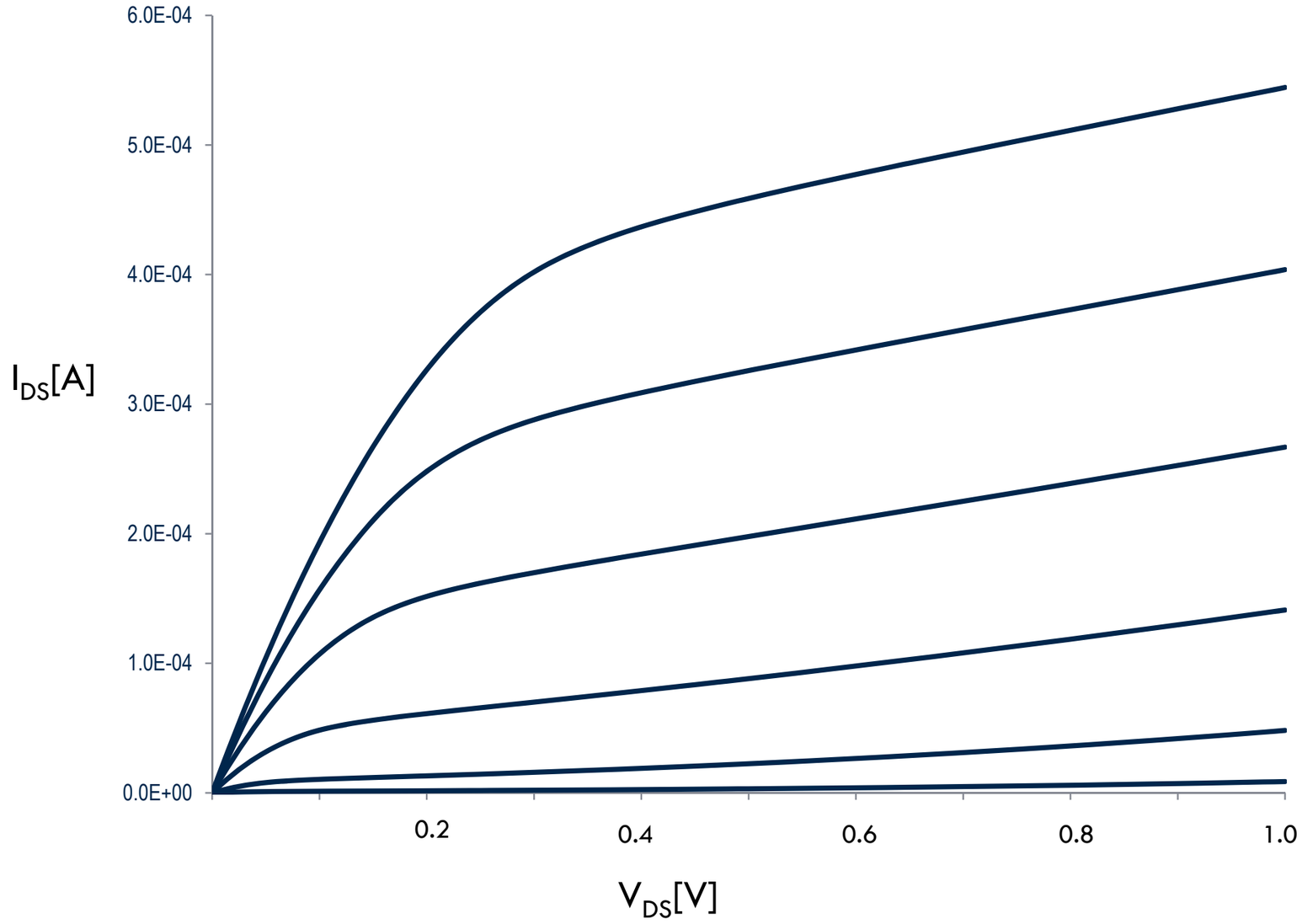
(a) schematic



(b) trajectory traversed on ID-VDS curve.

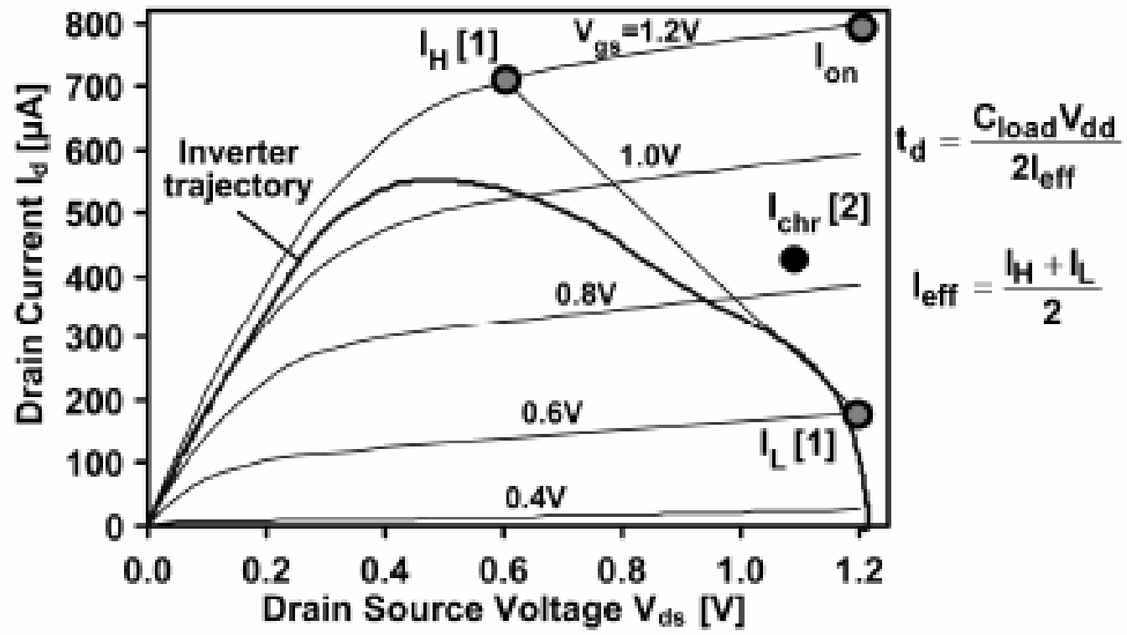
ln2 = 0.7

Switching Trajectory



Effective Current

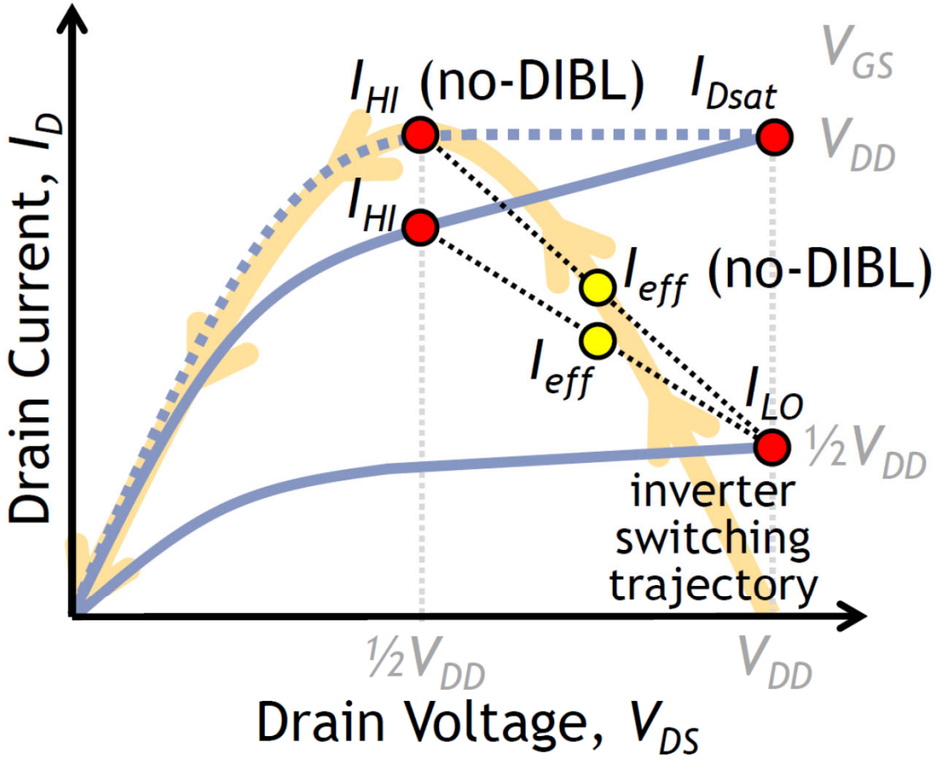
- $I_{on}(V_{DD})$ is never reached
- Define $I_{eff} = (I_H + I_L)/2$
- $I_L = I_{DS}(V_{GS}=V_{DD}/2, V_{DS}=V_{DD})$; $I_H=I_{DS}(V_{GS}=V_{DD}, V_{DS}=V_{DD}/2)$,



Na, IEDM'2002
Von Arnim, IEDM'2007

DIBL Matters

- A. Loke, VLSI'16
  - FinFET, FDSOI – less DIBL



$$I_{eff} = \frac{I_{LO} + I_{HI}}{2}$$

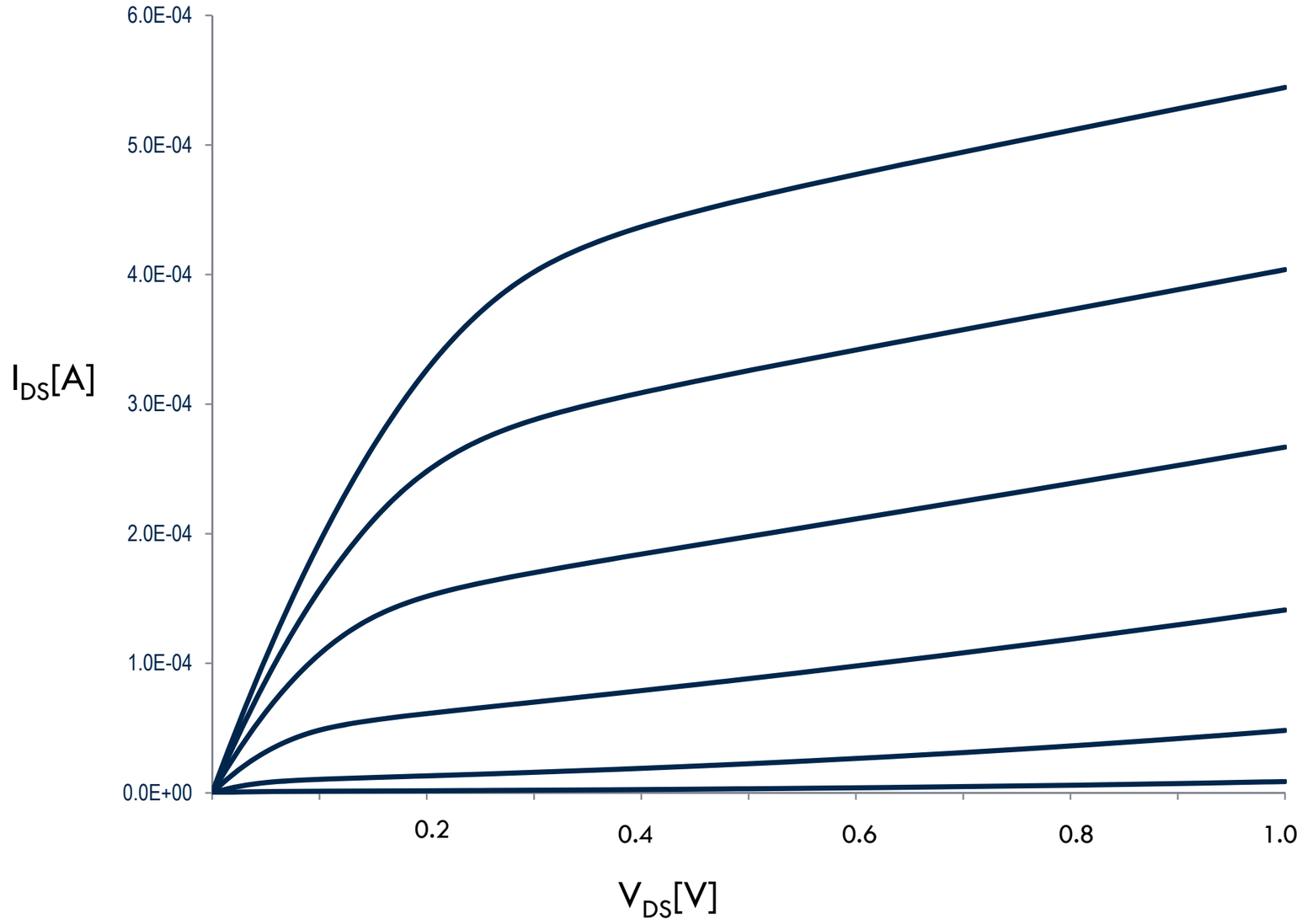
I_{LO} @ V_{GS}=½V_{DD}, V_{DS}=V_{DD}

I_{HI} @ V_{GS}=V_{DD}, V_{DS}=½V_{DD}

I_{eff} is better than I_{Dsat} for estimating inverter CV/I switching delay

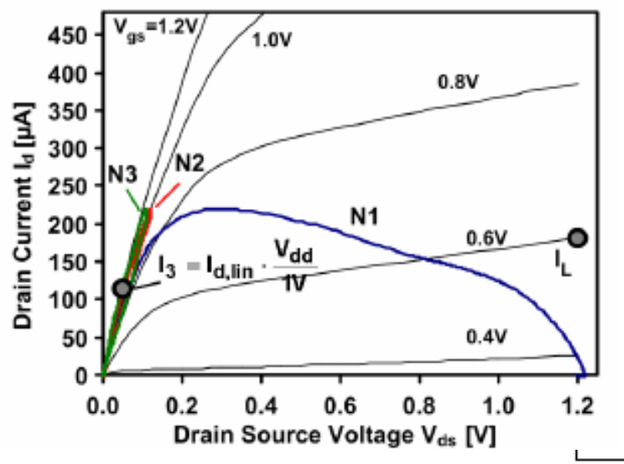
Less DIBL → higher I_{eff} & r_{out} for same I_{Dsat}

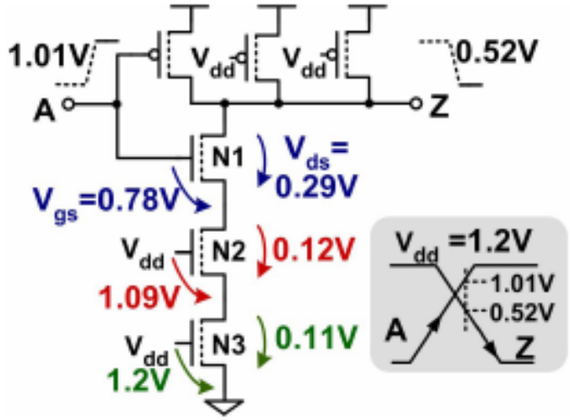
Transistor Stacks



Effective Current in Stacks

- Add linear current, I_3





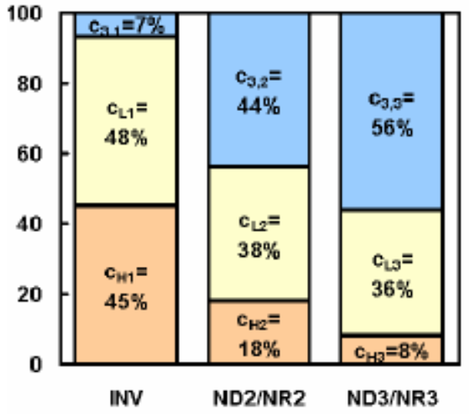
V_{gs}	V_{ds}
V_{dd}	$V_{dd}/2$
$V_{dd}/2$	V_{dd}
V_{dd}	$0.05 \cdot V_{dd}$

Model: $I_{stack,i} = c_{H,i} I_H + c_{L,i} I_L + c_{3,i} I_3 \Rightarrow$

Inverter: $I_{stack1} = 0.45 \cdot I_H + 0.48 \cdot I_L + 0.07 \cdot I_3$

NAND2/NOR2: $I_{stack2} = 0.18 \cdot I_H + 0.38 \cdot I_L + 0.44 \cdot I_3$

NAND3/NOR3: $I_{stack3} = 0.08 \cdot I_H + 0.36 \cdot I_L + 0.56 \cdot I_3$



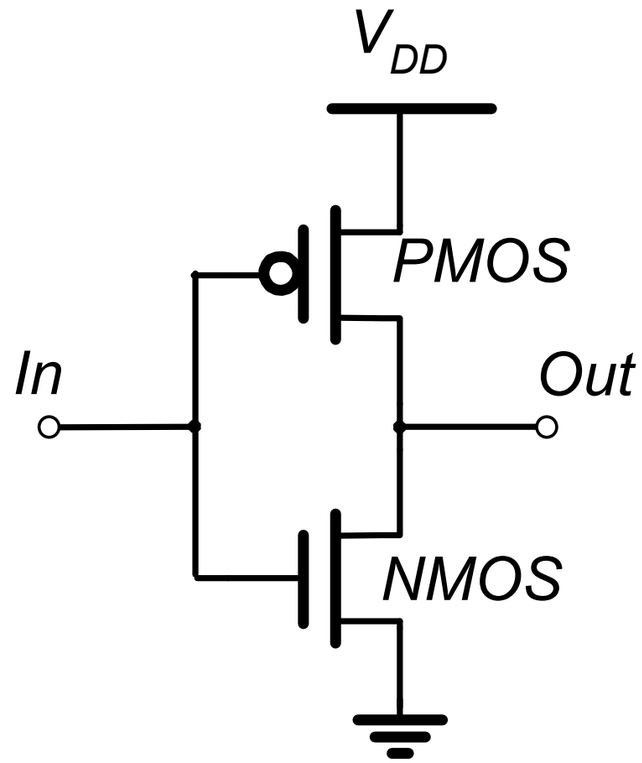
Von Arnim, IEDM'2007

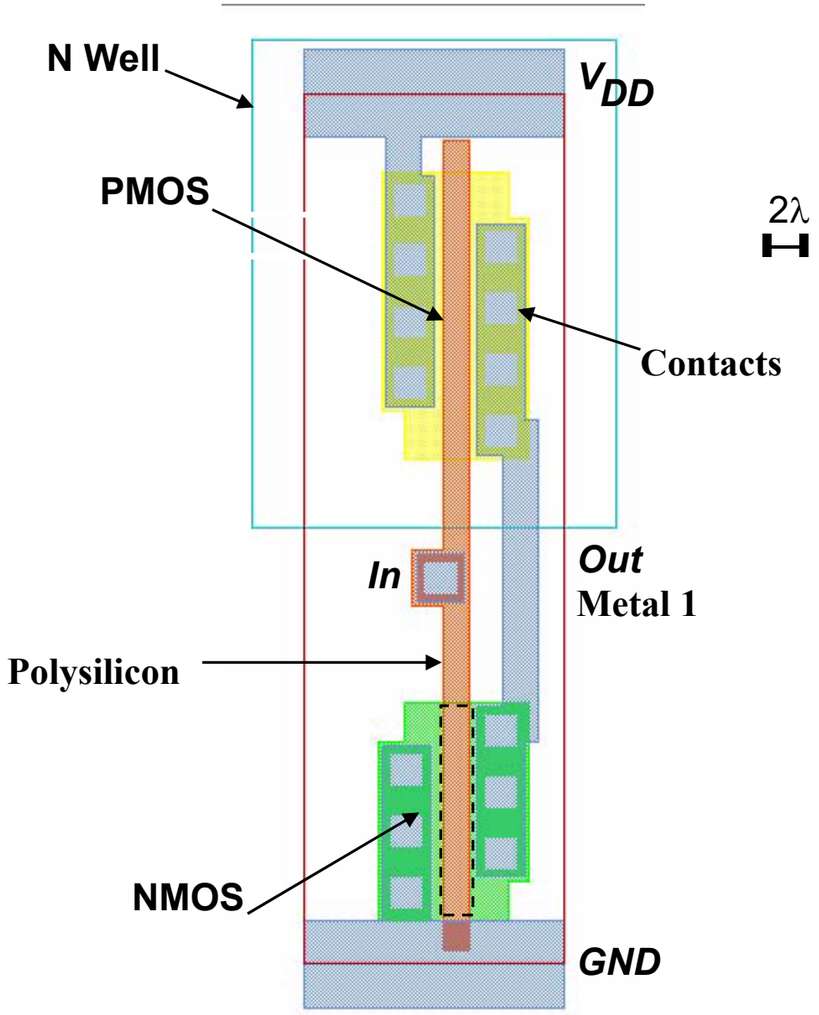
2.J Standard Cells

Standard Cell Inverter

- Schematic and layout

  (in a planar bulk process)



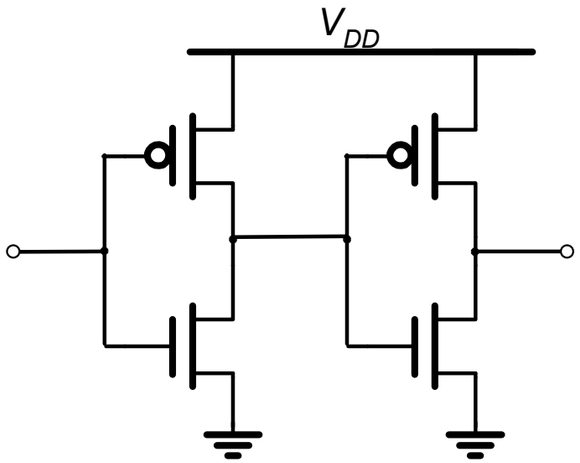


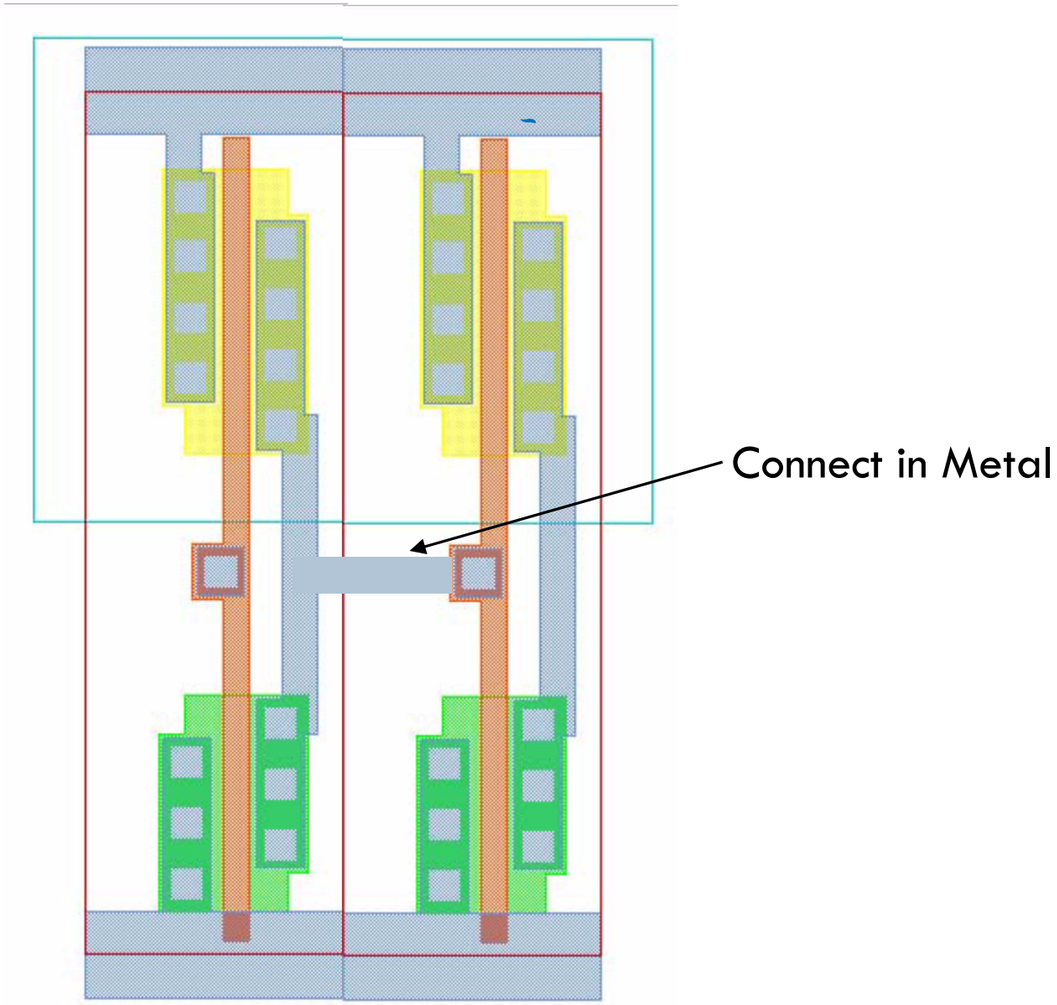
- Pitches are integer multiples of λ

Two Inverters

Share power and ground

Abut cells



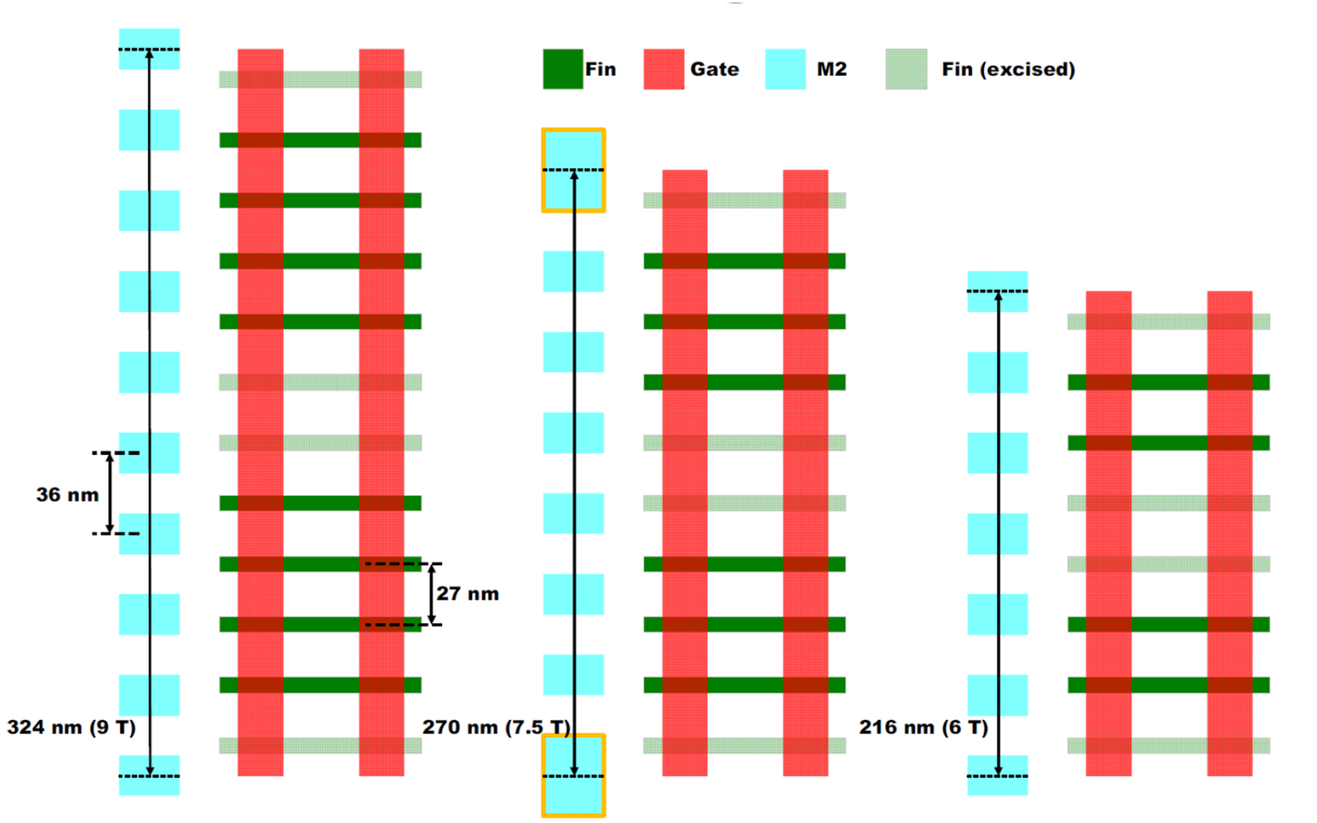


- Delay is additive

FinFET Standard Cells

ASAP7

- **Standard cell height selection is application specific**
  - **Related to fins/gate, i.e. drive strength**
- **Gear ratio: fin-to-metal pitch ratio**
  - **Cell height needs to be integer # of fins and (mostly) an integer # of metals accessing the cell pins (e.g. M2)**



- **12 fin pitches, 9 M2 tracks**
  - **Easy intra-cell routing, rich library**
  - **Wasteful for density**
- **10 fin pitches, 7.5 M2 tracks**
  - **Rich library without overly difficult routing or poor density**
  - **Allows wide M2 power rails**
- **8 fin pitches, 6 M2 tracks**
  - **Difficult intra-cell routing, diminished library richness**
  - **Limited pin access**

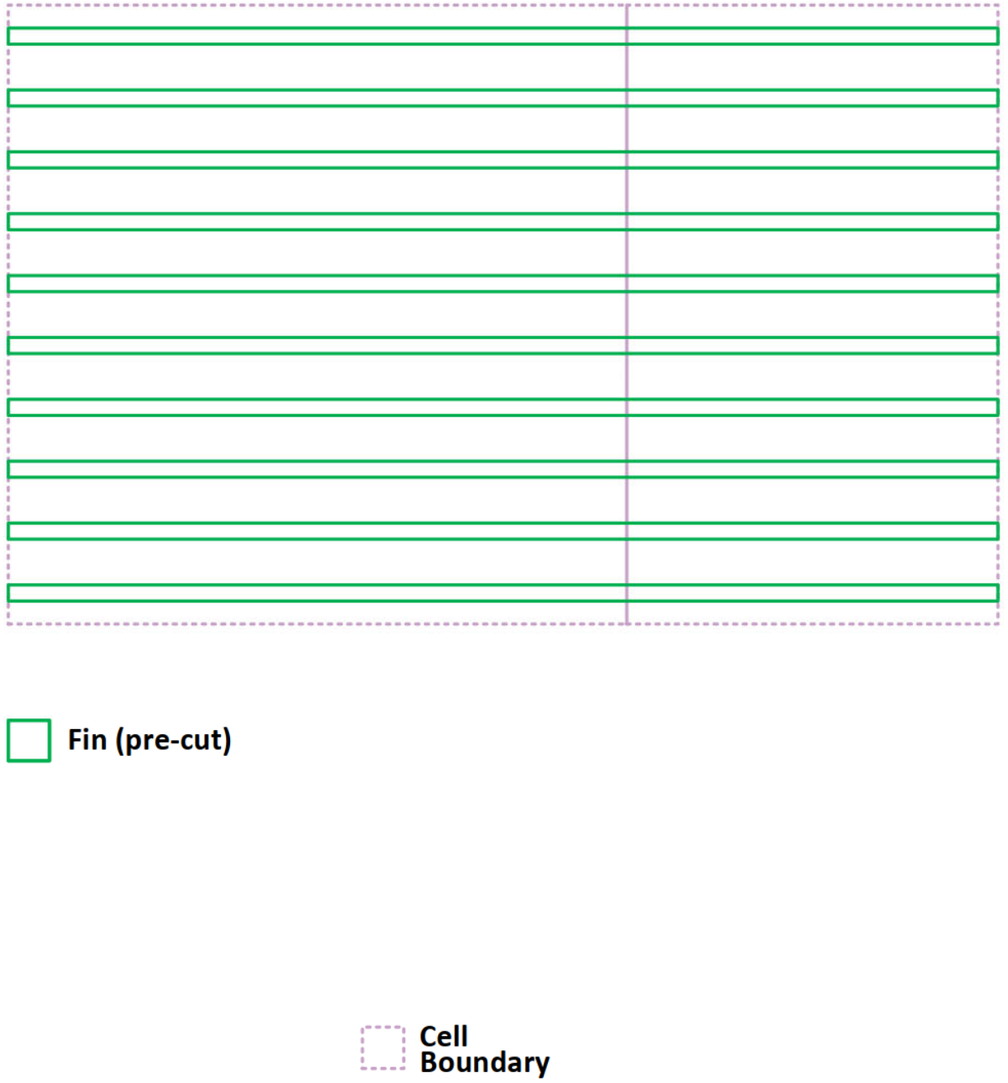
ICCAD 2017 Embedded Tutorial ASAP7

16

V. Vashishtha, ICCAD'17

ASAP7 Standard Cells

- **Cell architecture**
  - **7.5 M2 track height**
    - **Provides good gear ratio with fin, poly, and M2 pitch**



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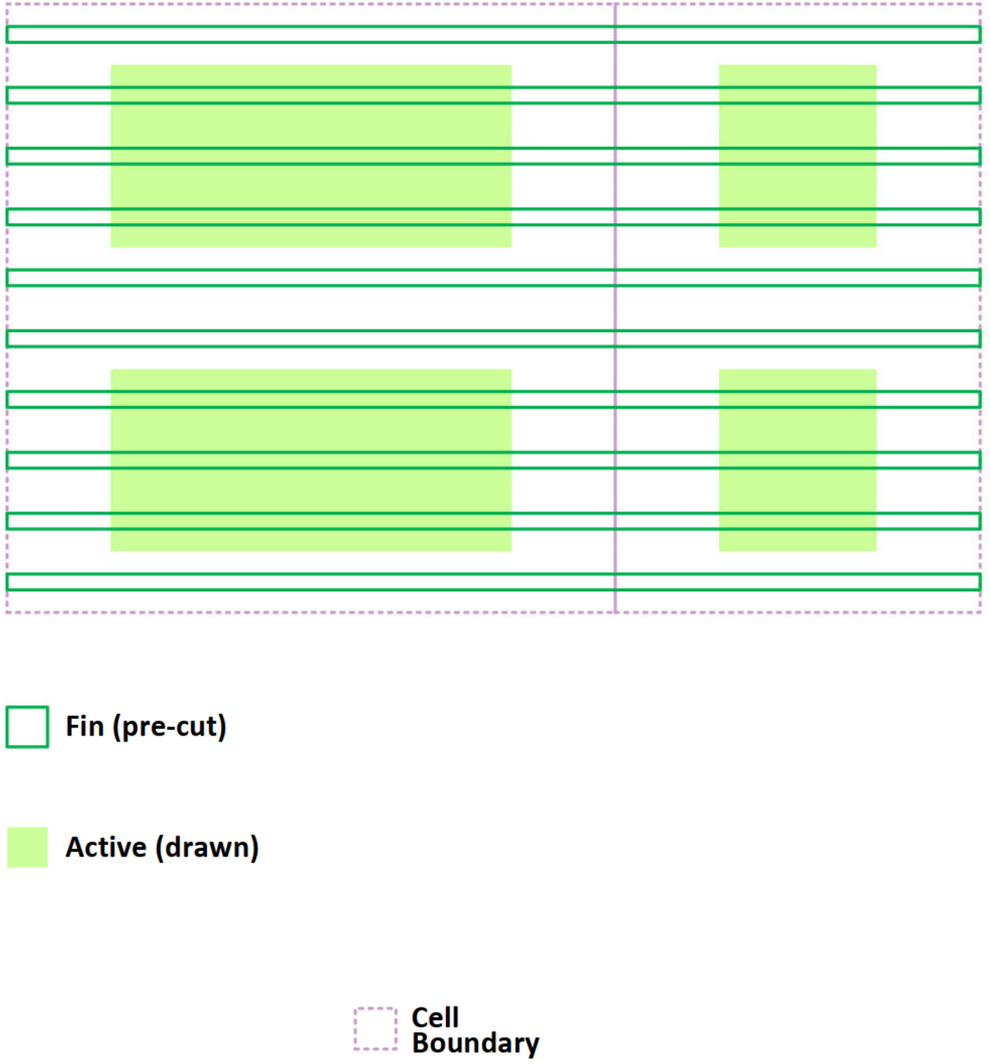

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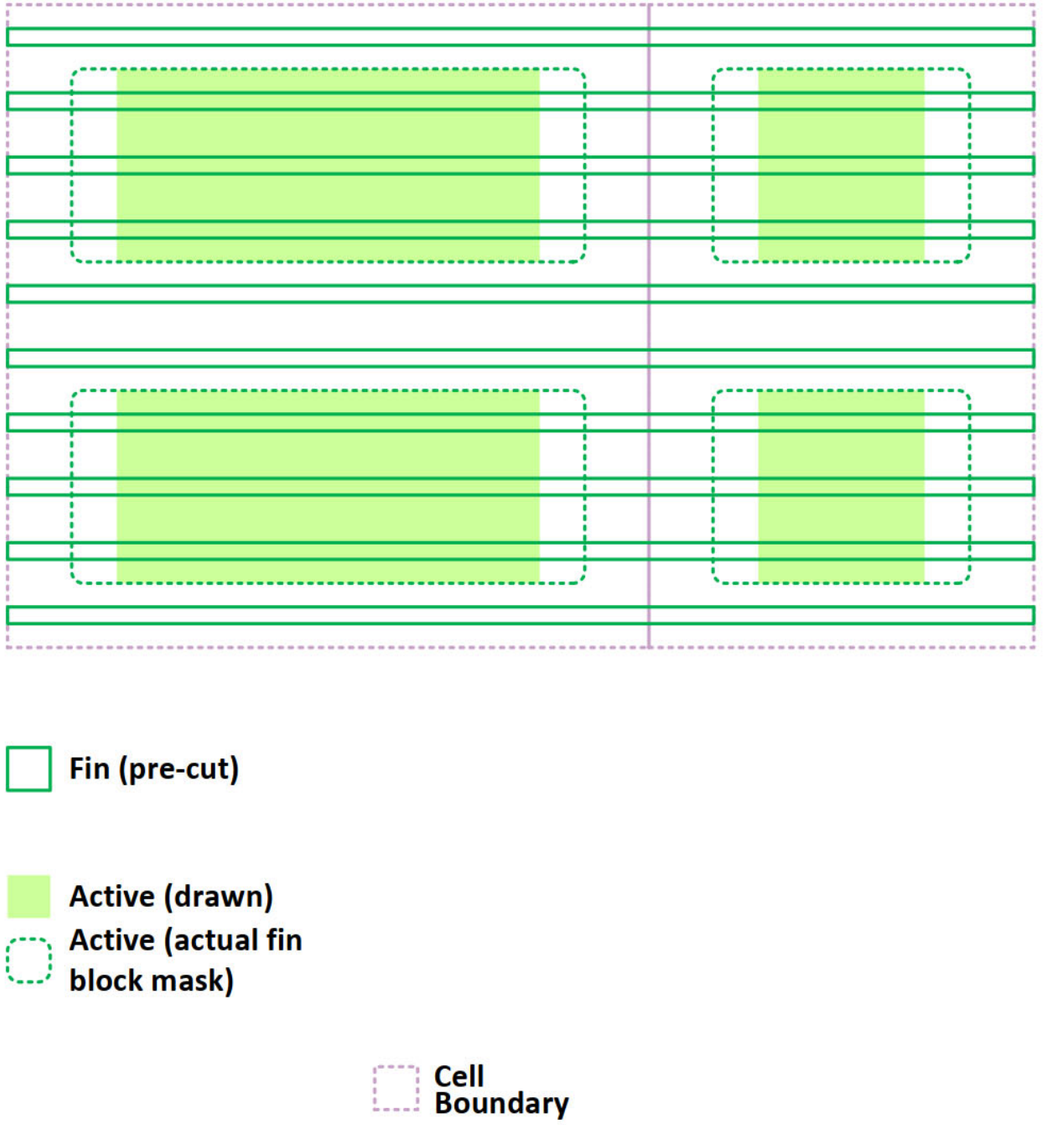

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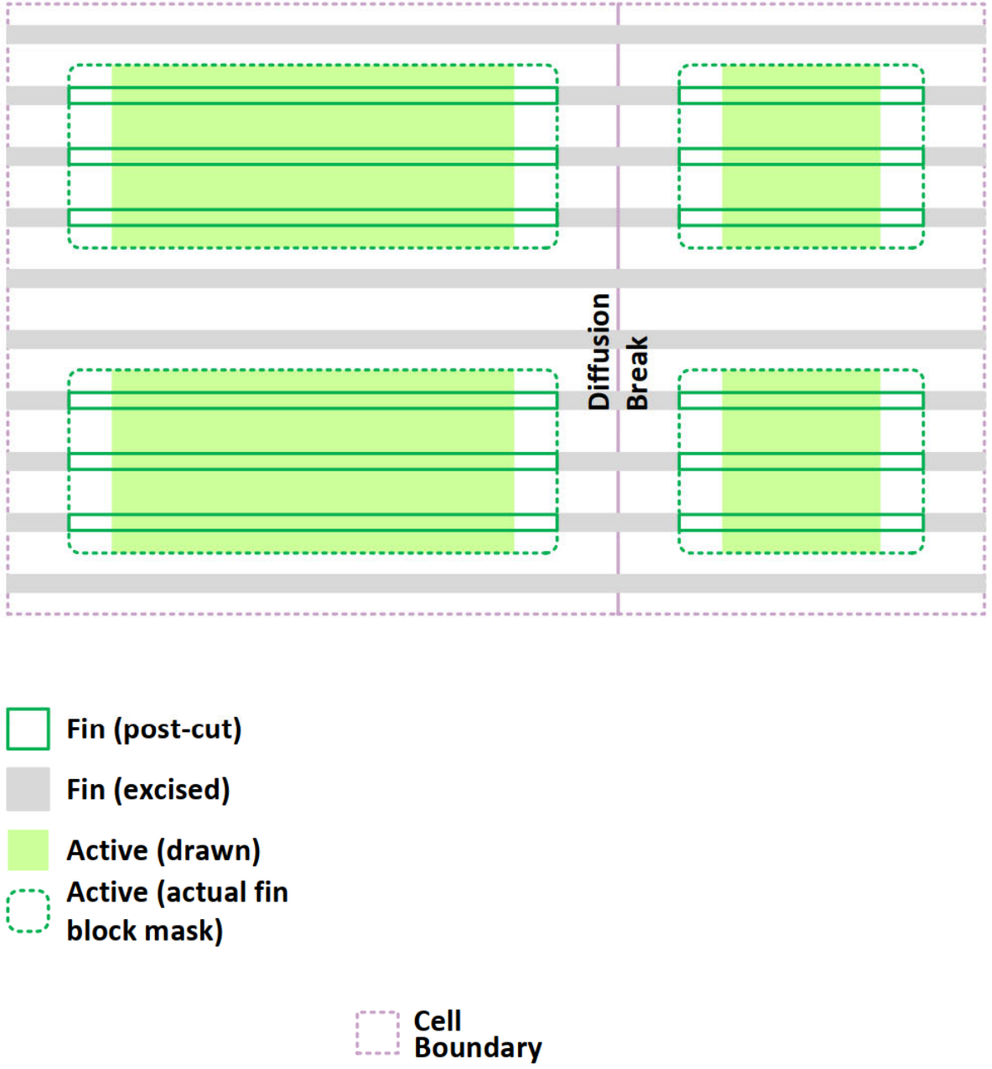
  - **Design rules check for connectivity**



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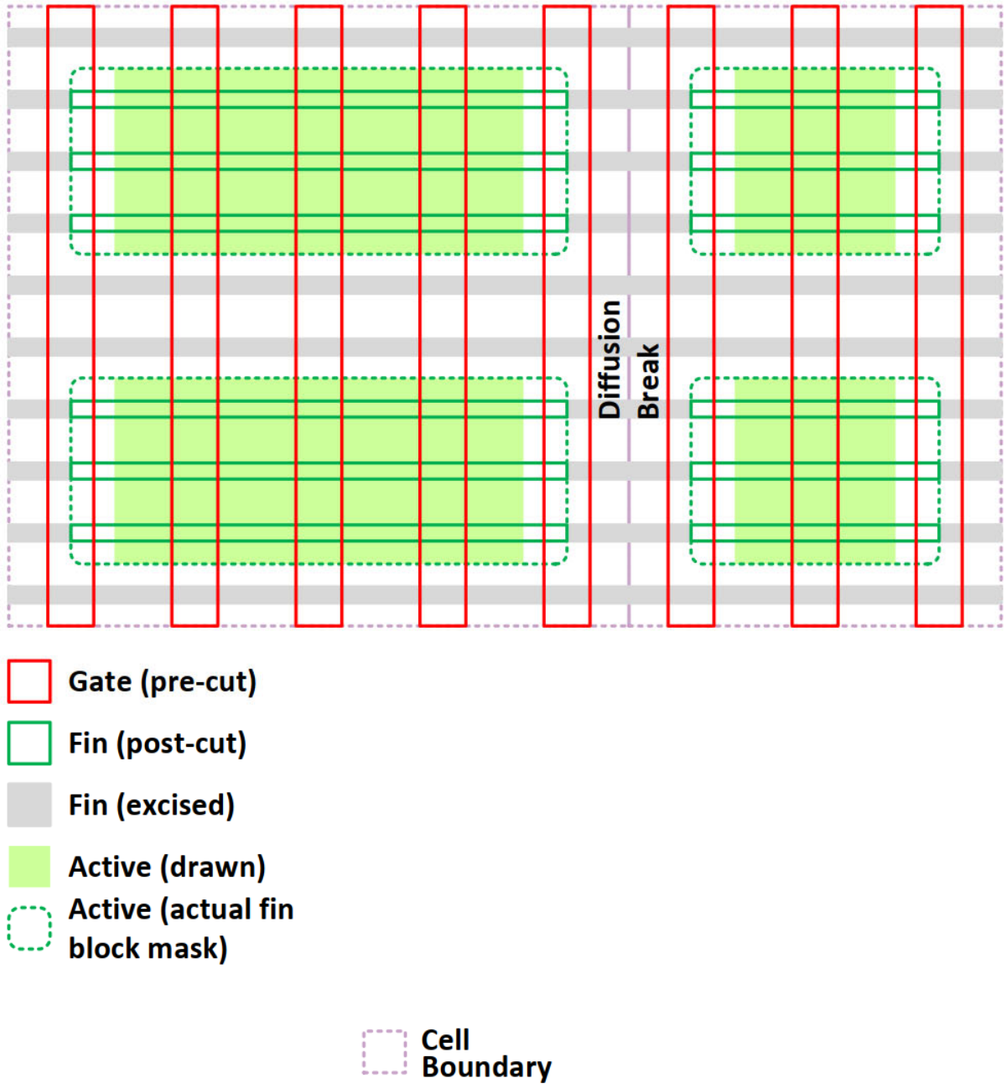

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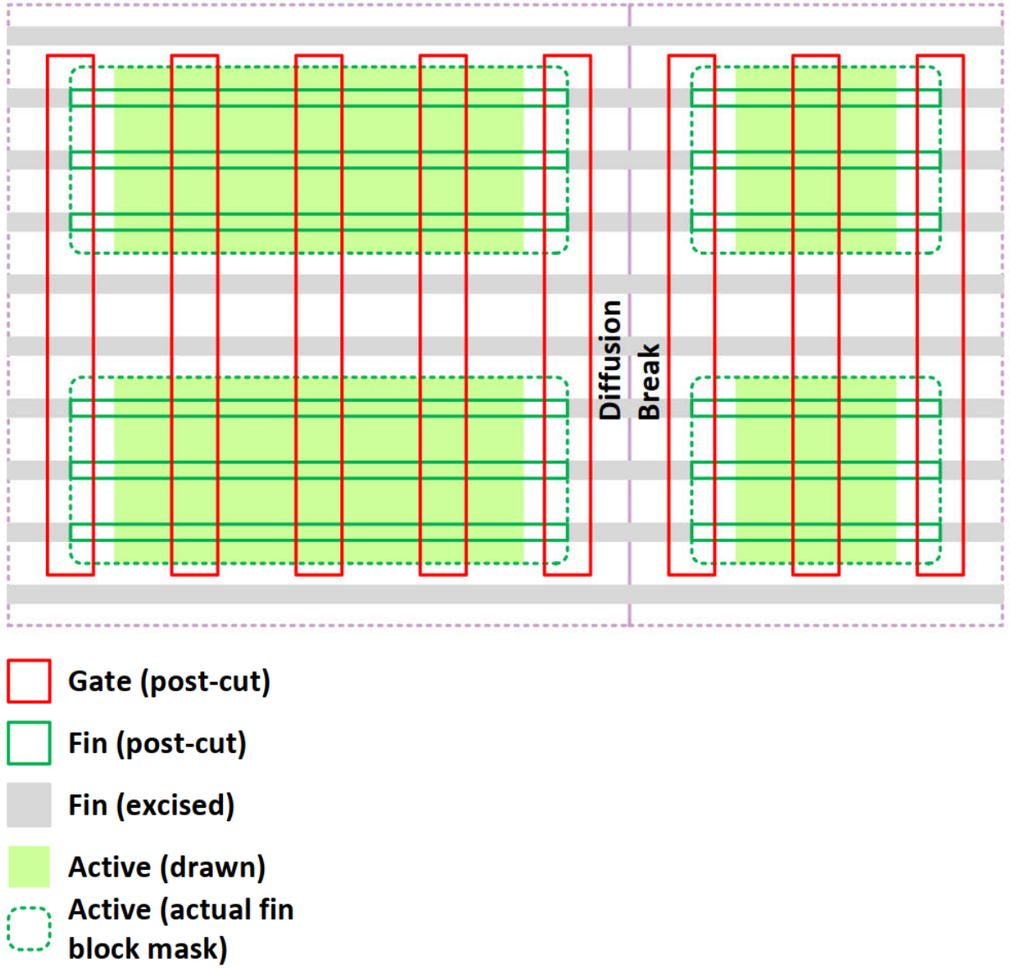

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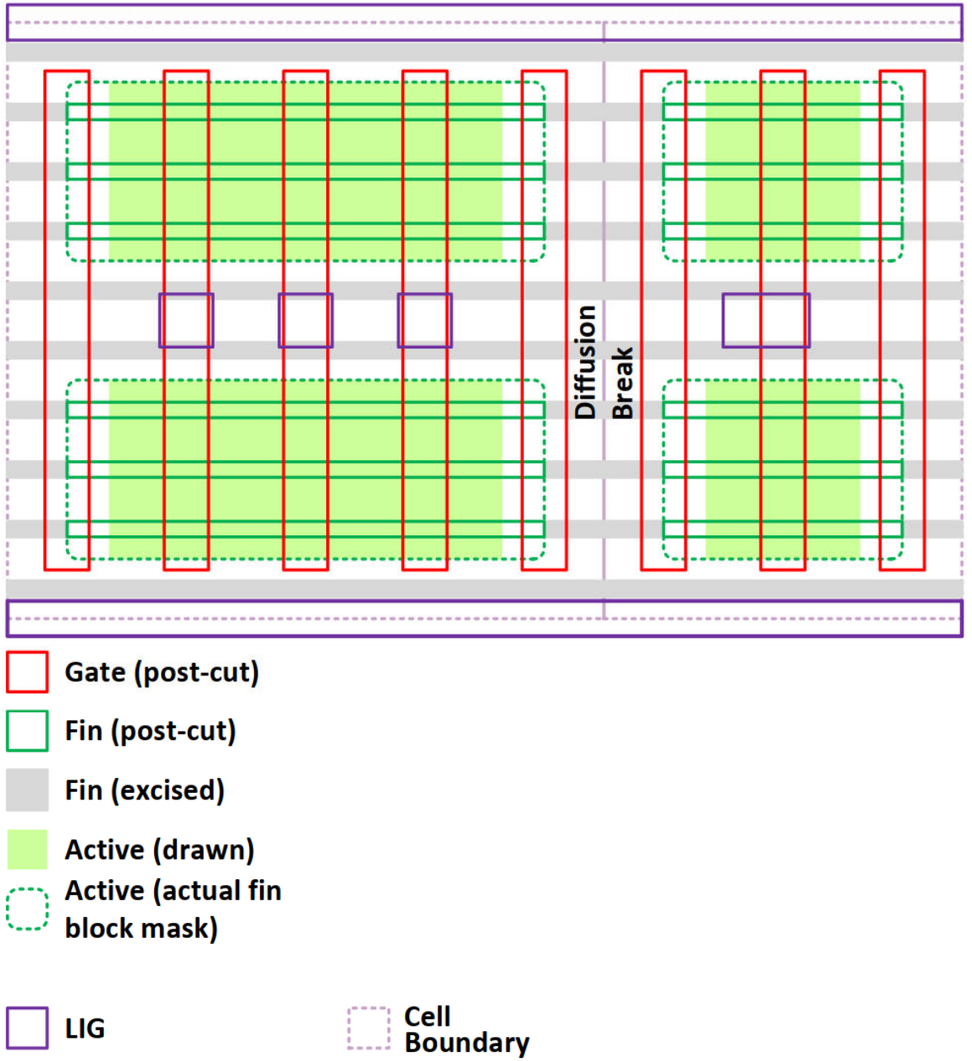

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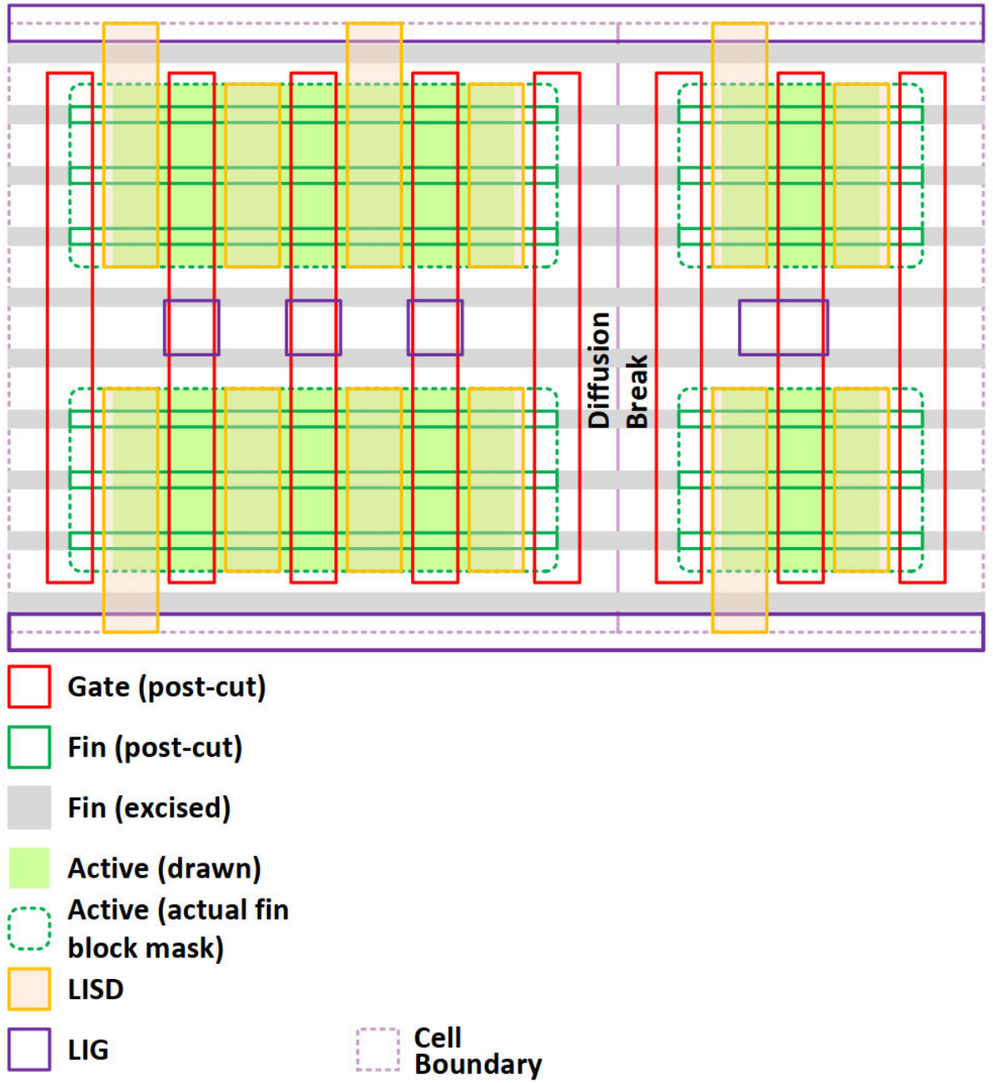

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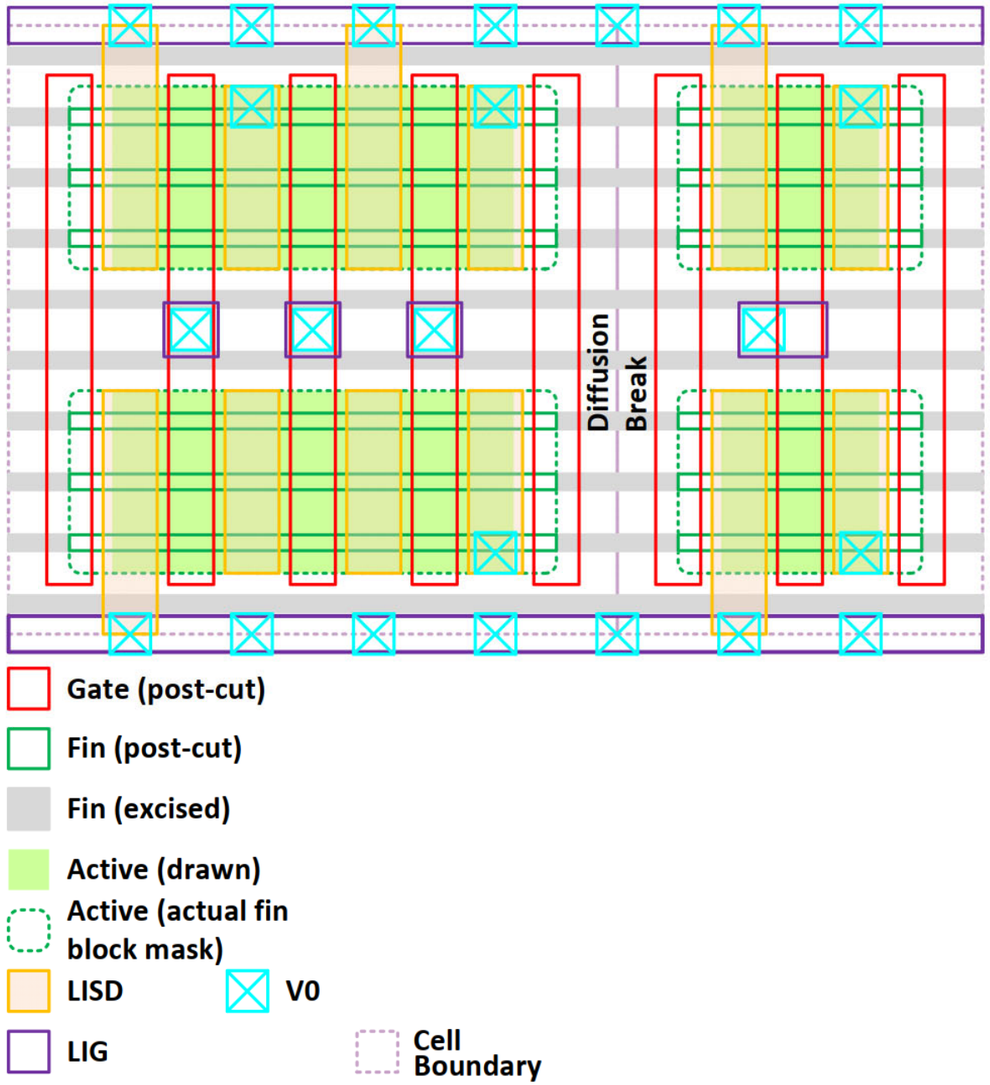

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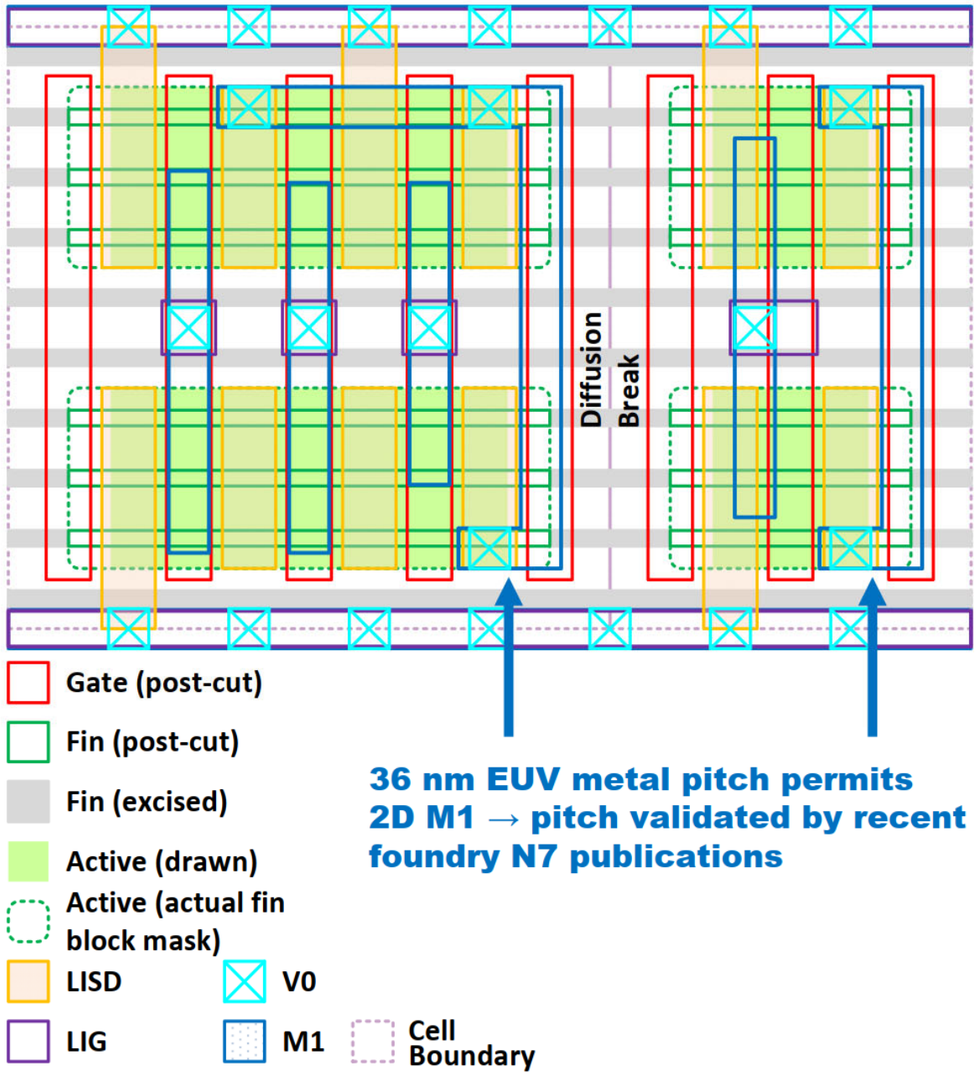

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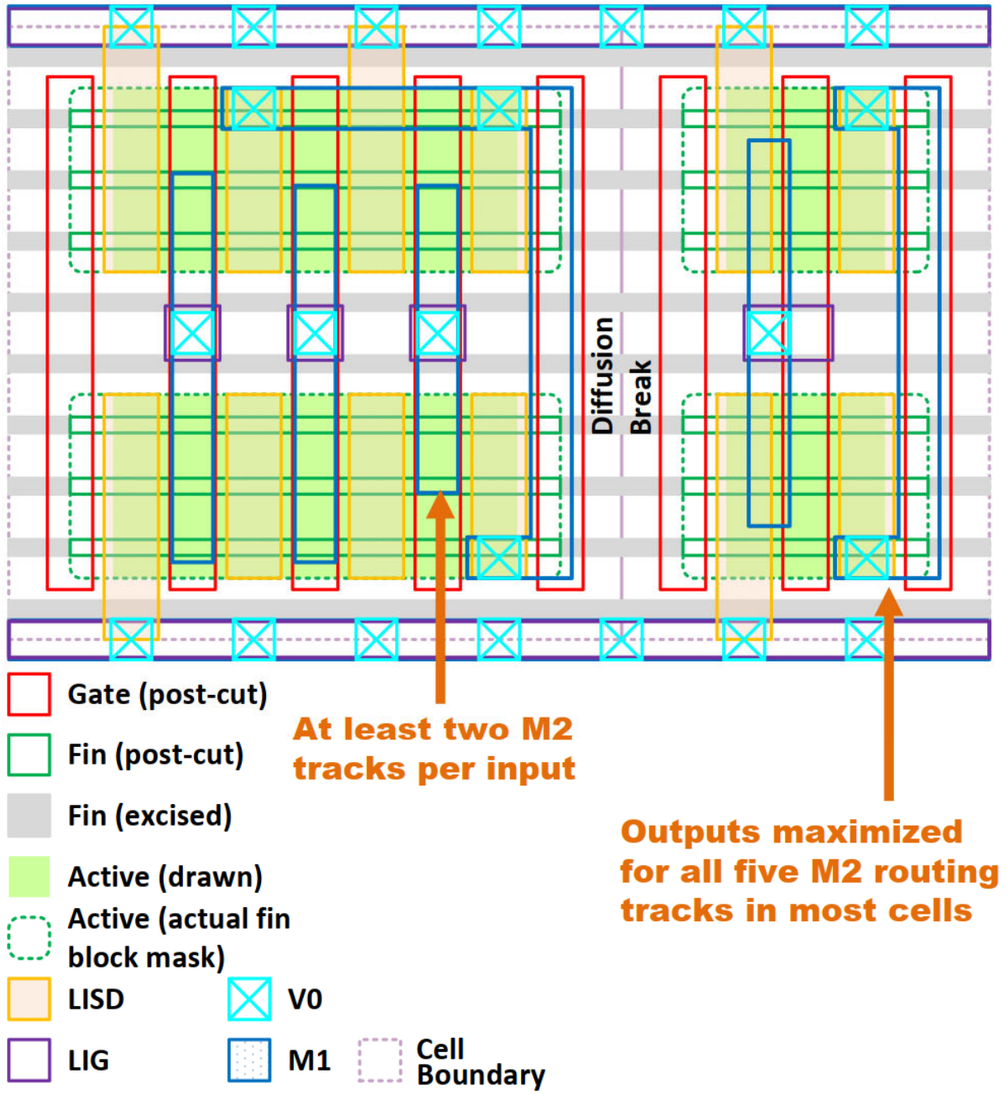

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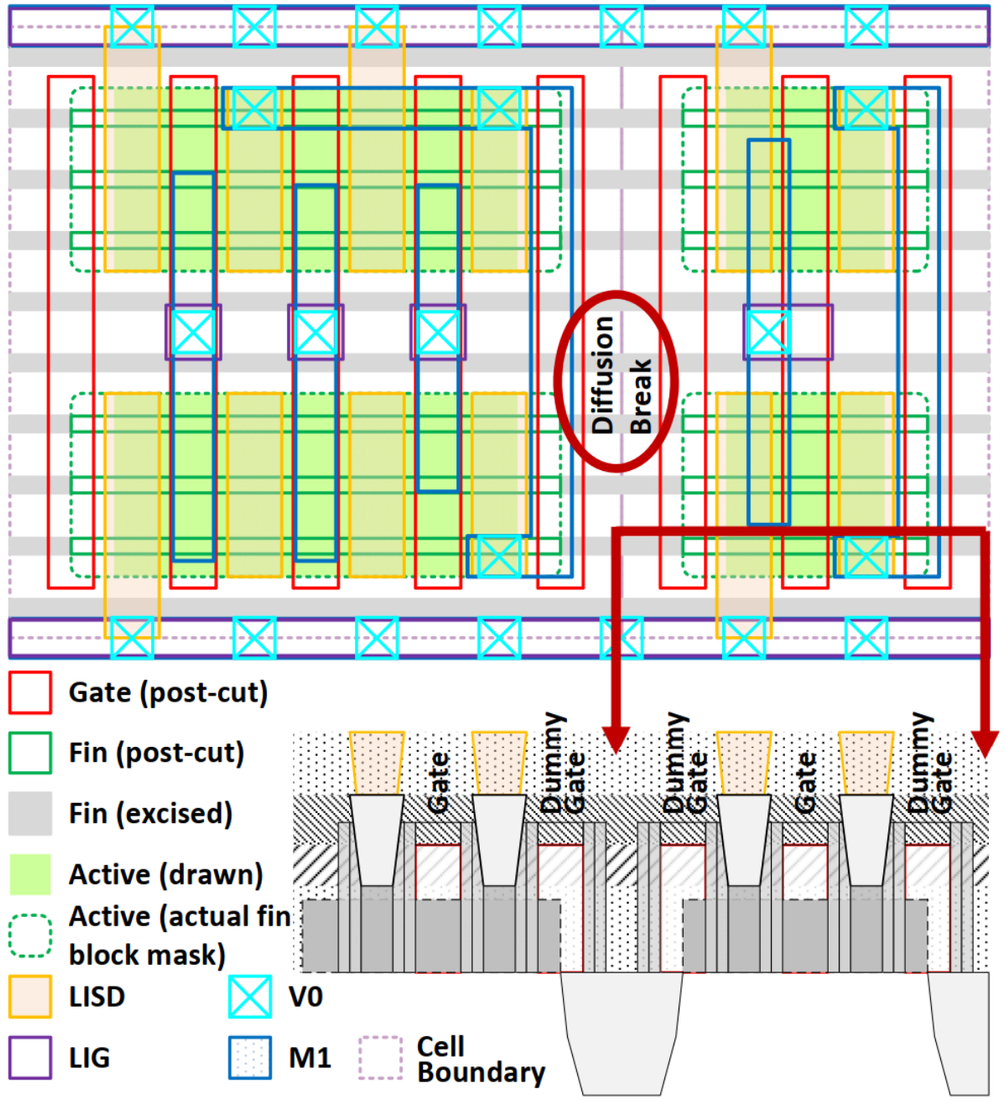
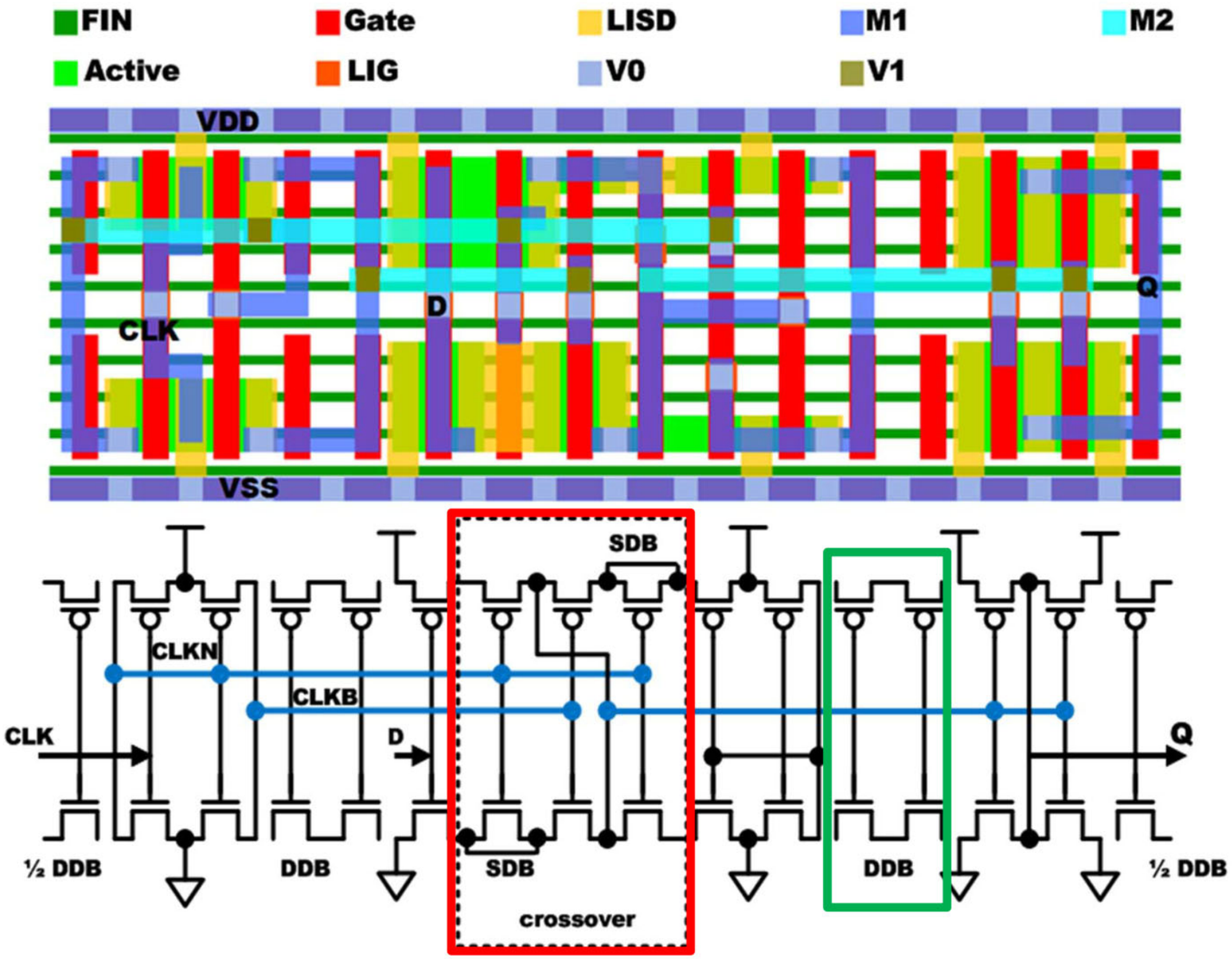
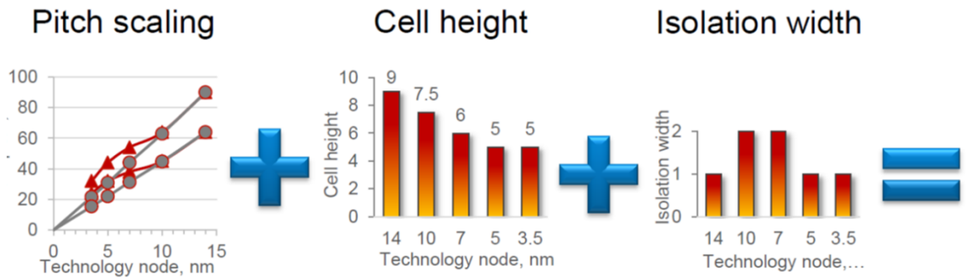


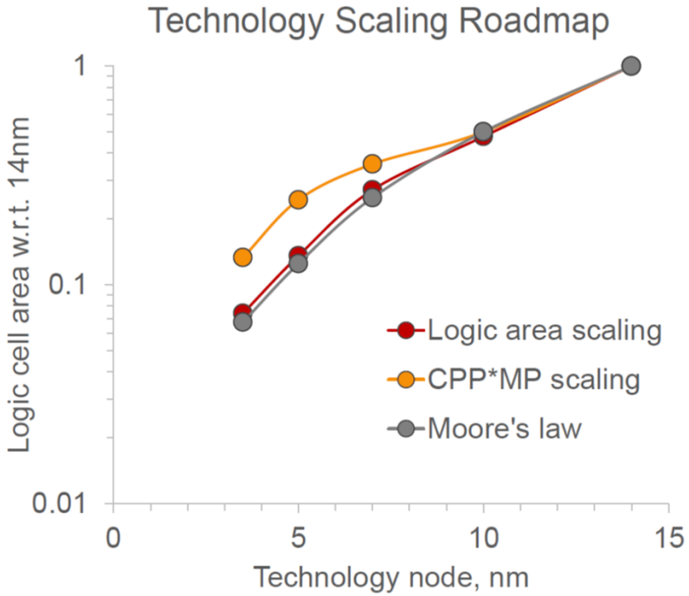
ASAP7 Latch



- **This demonstrates a crossover**
  - **Note single diffusion breaks (SBDs)**
  - **Horizontal M2 can only support limited tracks**
- **Intel, Samsung support SDBs (no DDBs) at N10/N7 [EETimes]**

FinFET Standard Cells





V. Moroz, Semicon Taiwan, 2016

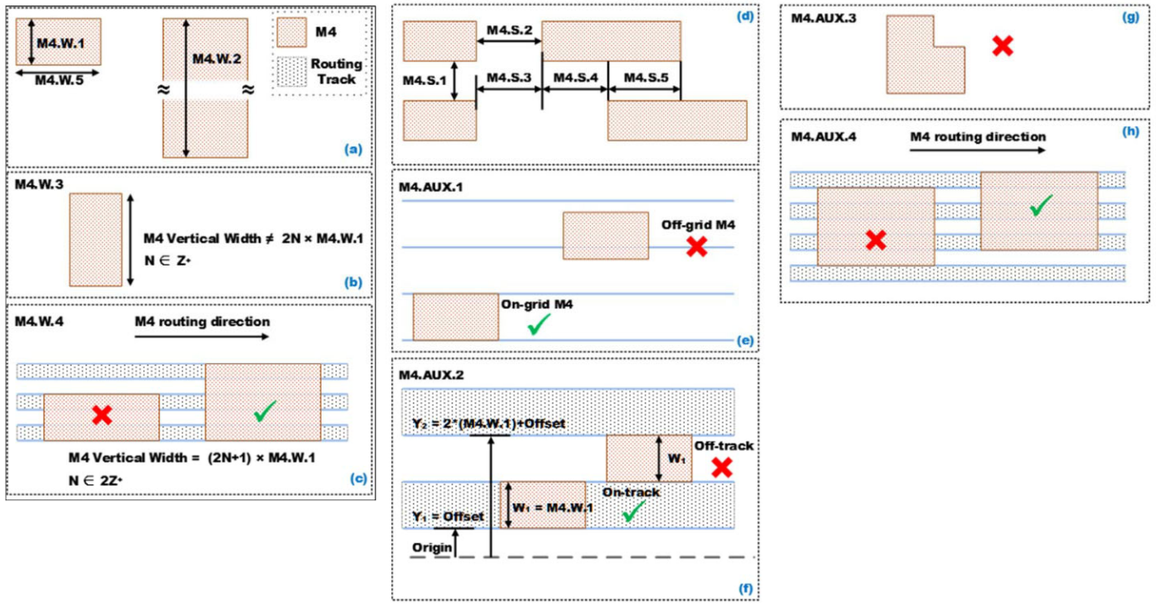
Design Kit Components

- Physical views
  - Layout and schematic, with abstractions
- Netlist
- Logical view
  - Test view
- Timing, power and noise views
- Documentation

EE241B Technology

- ASAP7 7nm predictive technology kit
  - Also available Synopsys 32/28nm Generic Library
- Multi-vth Standard Cell Library 45 IO pads
- SRAMs
- Design rule manual

Rule	Rule Type	Description	Operator	Values	Units
M4.W.1	Width	Minimum vertical width of M4	≥	24	nm
M4.W.2	Width	Maximum vertical width of M4	≤	480	nm
M4.W.3	Width	M4 vertical width may not be an even integer multiple of its minimum width.	-	-	-
M4.W.4	Width	M4 vertical width, resulting in the polygon spanning an even number of minimum width routing tracks vertically, is not allowed.	-	-	-
M4.W.5	Width	Minimum horizontal width of M4	≥	44	nm
M4.S.1	Spacing	Minimum vertical spacing between two M4 layer polygons' edges, regardless of the edge lengths and mask colors	≥	24	nm
M4.S.2	Spacing	Minimum horizontal spacing between two M4 layer polygons' edges, regardless of the edge lengths and mask colors	≥	40	nm
M4.S.3	Spacing	Minimum tip-to-tip spacing between two M4 layer polygons—that do not share a parallel run length—on adjacent tracks	≥	40	nm
M4.S.4	Spacing	Minimum tip-to-tip spacing between two M4 layer polygons—that share a parallel run length—on adjacent tracks	≥	40	nm
M4.S.5	Spacing	Minimum parallel run length of two M4 layer polygons on adjacent tracks	≥	44	nm
M4.AUX.1	Auxiliary	M4 horizontal edges must be at a grid of	==	24	nm
M4.AUX.2	Auxiliary	Minimum width M4 tracks must lie along the horizontal routing tracks. These tracks are located at a spacing equal to: 2N x minimum metal width + offset from the origin, where N ∈ Z-+.	-	-	-
M4.AUX.3	Auxiliary	M4 may not bend.	-	-	-
M4.AUX.4	Auxiliary	Outside edge of a wide M4 layer polygon may not touch a routing track edge.	-	-	-



2.K Class Design Flow

Servers to Use

- **Please use the instructional servers**
  - Labs may not be up to date on BWRC machines
- Servers to use:
  - c152m-{1-15}.eecs.berkeley.edu
  - eda-{1-8}.eecs.berkeley.edu
- Other servers may be missing tools / may be using a different version!
- EECS instructional website is helpful!
  - http://inst.eecs.berkeley.edu/~inst/iesglabs.html

Text Editors/Other commands and tools

- Learn to use vim
  - gvim, emacs are some alternatives
  - You will not be sorry!
  - Gedit can cause some issues
- Use tmux
- Other unix commands
  - ls, cd, cp, rm, mkdir, tar, grep, …
  - Life skills!

Getting Started: Logging in

- From terminal:
  - ssh –Y <username>@<server>
  - Instructional account login
- From Windows:
  - Can use putty
  - Linux subsystem
- Can also you x2go to connect to a remote desktop

Setting up your environment

- Can work in home directory for basic things
- Move to /scratch/ (local to each machine) for running the labs
  - Make your own directory here to work in
- Follow the directions in the lab
  - Clone the lab
  - Tools are configured as submodules
    - Run git submodule update –init –recursive to initialize the submodules
  - Need to source sourceme.sh every time you reinitialize
    - Sets up some Hammer variables
    - Sources course .bashrc

Instructional Tools and Technology

- Most tools can be found in /share/instww/{cadence or synopsys}
- ASAP7 technology new for this semester
  - Open predictive PDK
  - Can be found in ~ee241/spring20-labs/
- Lab requires you to look at technology (and maybe some tool manuals)
  - Manuals are your friend!
  - They can usually be found in a docs/ folder in the tool directory.

git

- Version control
- Another important “learn to use”
- Shouldn’t need much advanced use for this class but it is a lifeskill!
- git clone
  - Initialize
- git submodule update –init –recursive
  - Initialize all submodules
  - Only need to run once in this context

Lab Preview

- Update for this semester
  - Converted to use Hammer and ASAP7
  - Please post on Piazza and come to office hours if you run into issues
- Baseline overview of a portion of the VLSI flow
  - Simulation, synthesis, P&R
  - Looking at log files, reports, etc. to understand the design and tools
  - It's about telling the tools what it wants to hear
- What's missing?
  - Discussed in the summary
  - DRC, LVS, more advanced power analysis, much more!
  - Pay attention to lecture and think about how you can integrate into the flow

Lab Preview (continued)

- Hammer
  - https://github.com/ucb-bar/hammer
  - Python framework for physical design
  - Separation of concerns to enable reuse
  - What are these hammer-cadence-plugins and hammer-synopsys-plugins?
    - Tool specific implementations of APIs
    - Not publicly available so do not share!
  - So where's the technology plugin?
    - hammer/src/hammer-vlsi/technology/asap7/
- ASAP7
  - Take a look at the files!

```
% hammer-vlsi step -e env.yml -p input.yml --obj_dir build
% hammer-vlsi synthesis -e env.yml -p input.yml --obj_dir build
```

Next Lecture

- Library characterization
- Static timing