EE241B : Advanced Digital Circuits

Lecture 7 – Static Timing

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February 7, 2020, (Inc.) Elon Musk Says He's About to Deliver the Future of High-Speed Internet.

Get your investment dollars ready.

Elon Musk has been saying for years that he believes the future of the internet resides in space. And now he's planning to make a major change that could facilitate that transition sooner rather than later.

In a move that could send shock waves through the internet space, SpaceX is planning to spin out its Starlink satellite-based internet service into its own entity. It'll also make Starlink public, allowing investors to get a piece of what Musk believes is the future of internet connectivity.

Announcements

- Homework 1 due on February 17
- No class on February 18 (ISSCC)
- Project abstracts due on February 20
  - Teams of 2
  - Title
  - One paragraph
  - 5 relevant references

Outline

- Module 2
  - Standard cells
  - Static timing

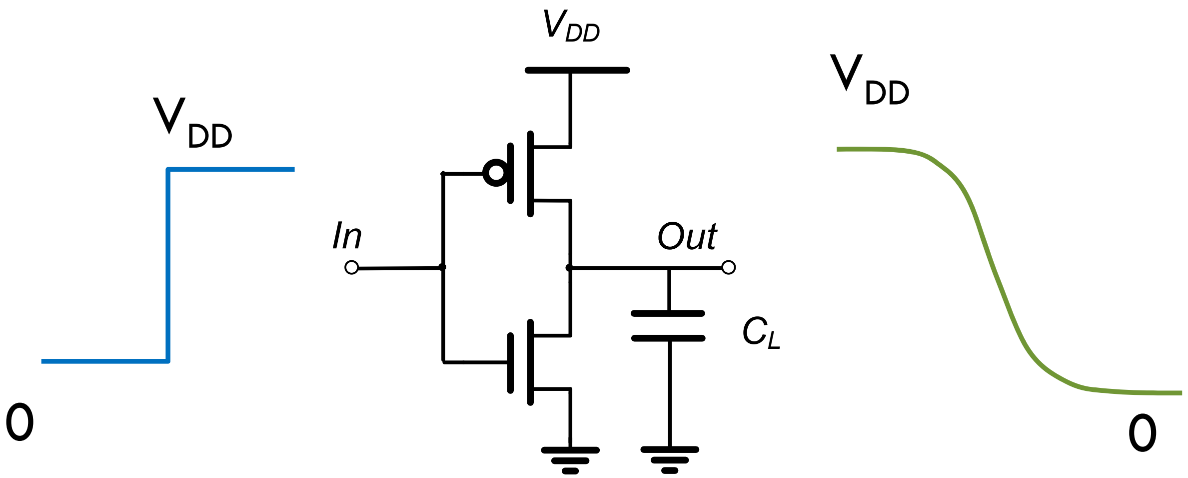
2.L Delay Revisited

How to Account for Input Slope?

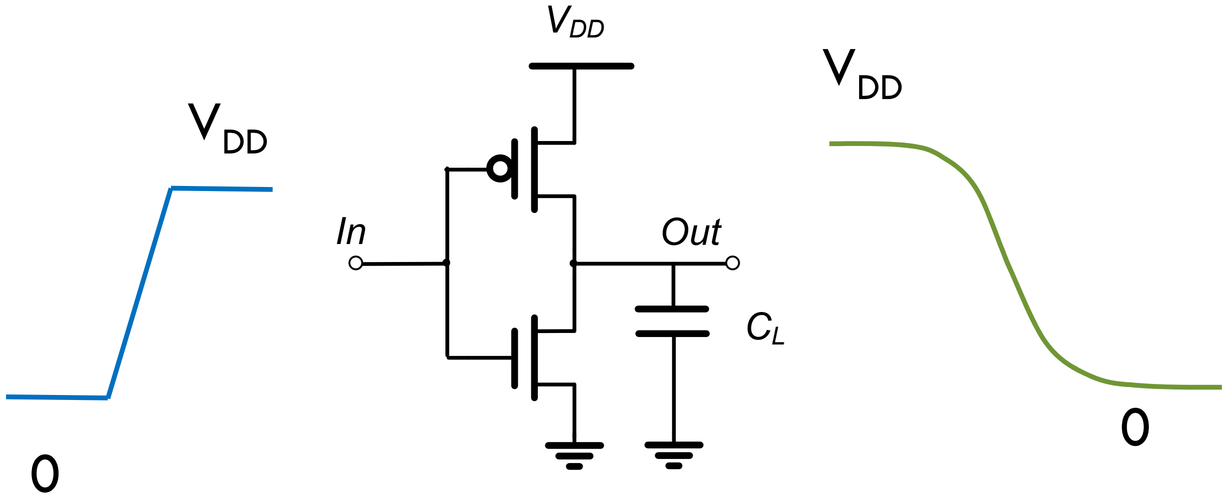
$t_p = \ln 2\ RC = 0.7\ R_{eq}C_L$

$T_{r,10\text{-}90} = 2.2\ R_{eq}C_L$

$T_{r,20\text{-}80} = 1.4\ R_{eq}C_L$



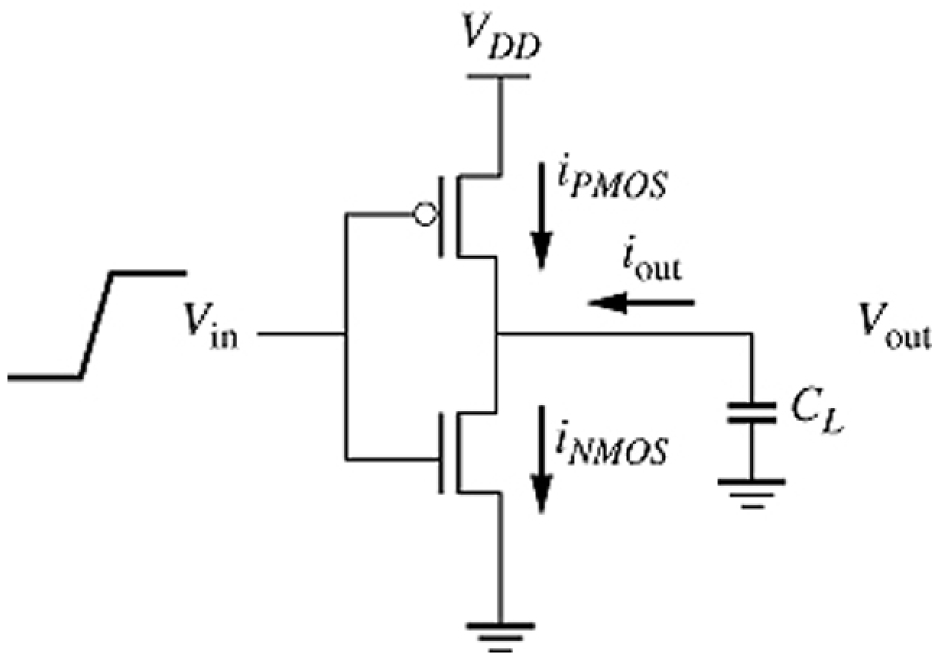
- $t_{pHL} = 0.7\ R_{eq}C_L$



- $t_{pHL} = 0.7\ R_{eq}C_L$

different R_{eq}!

Input Slope Dependence



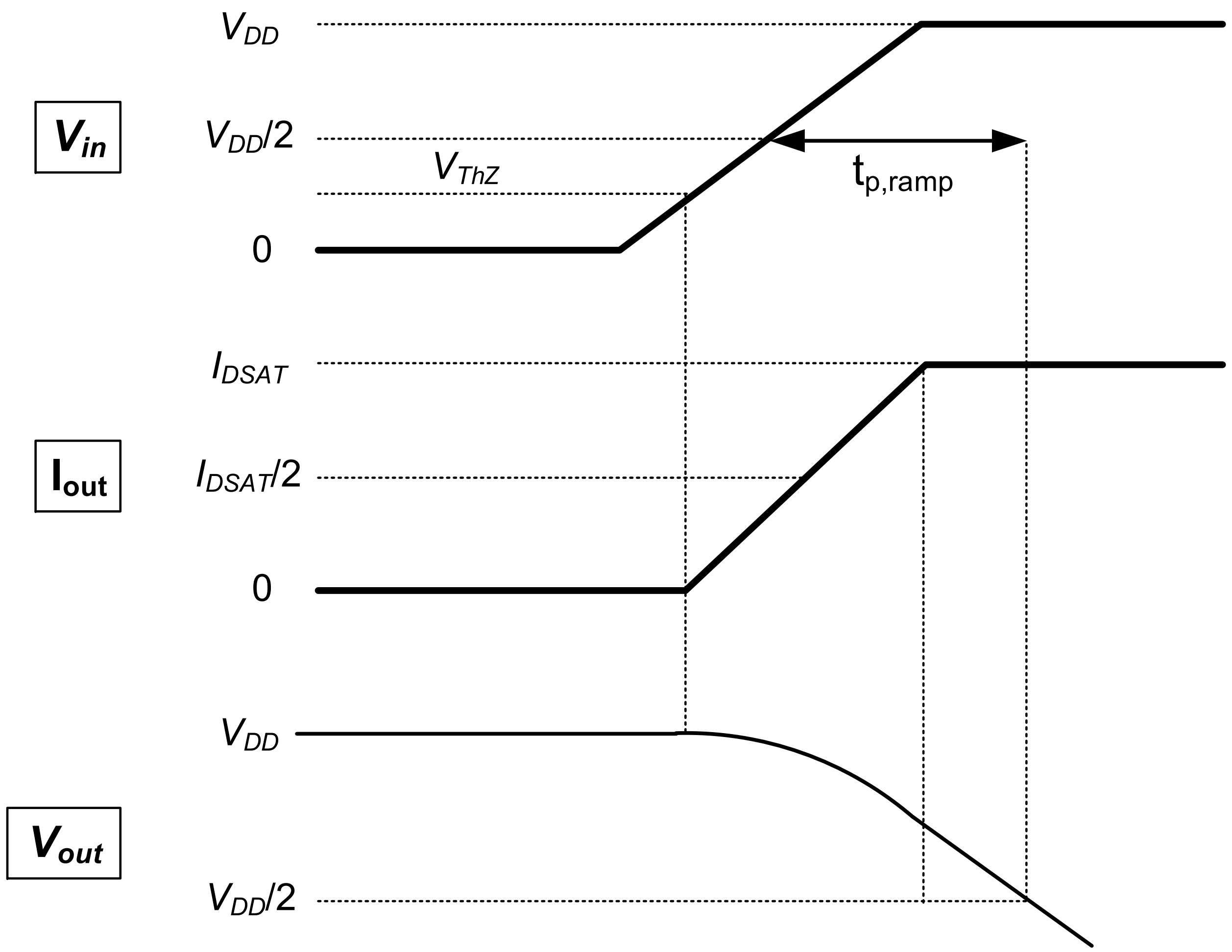
$$I_{out} = C_L \frac{dV_{out}}{dt} = I_{NMOS} - I_{PMOS}$$

- One way to analyze slope effect
  - Plug non-linear I-V into diff. equation and solve…
- Simpler, approximate solution:
  - Use V_{ThZ} model

Slope Analysis

- For falling edge at output:
  - For reasonable inputs, can ignore I_{PMOS}
  - Either V_{DS} is very small, or V_{GS} is very small
- So, output current ramp starts when $V_{in}=V_{ThZ}$
  - Could evaluate the integral
  - Learn more by using an intuitive, graphical approach

Slope Dependence

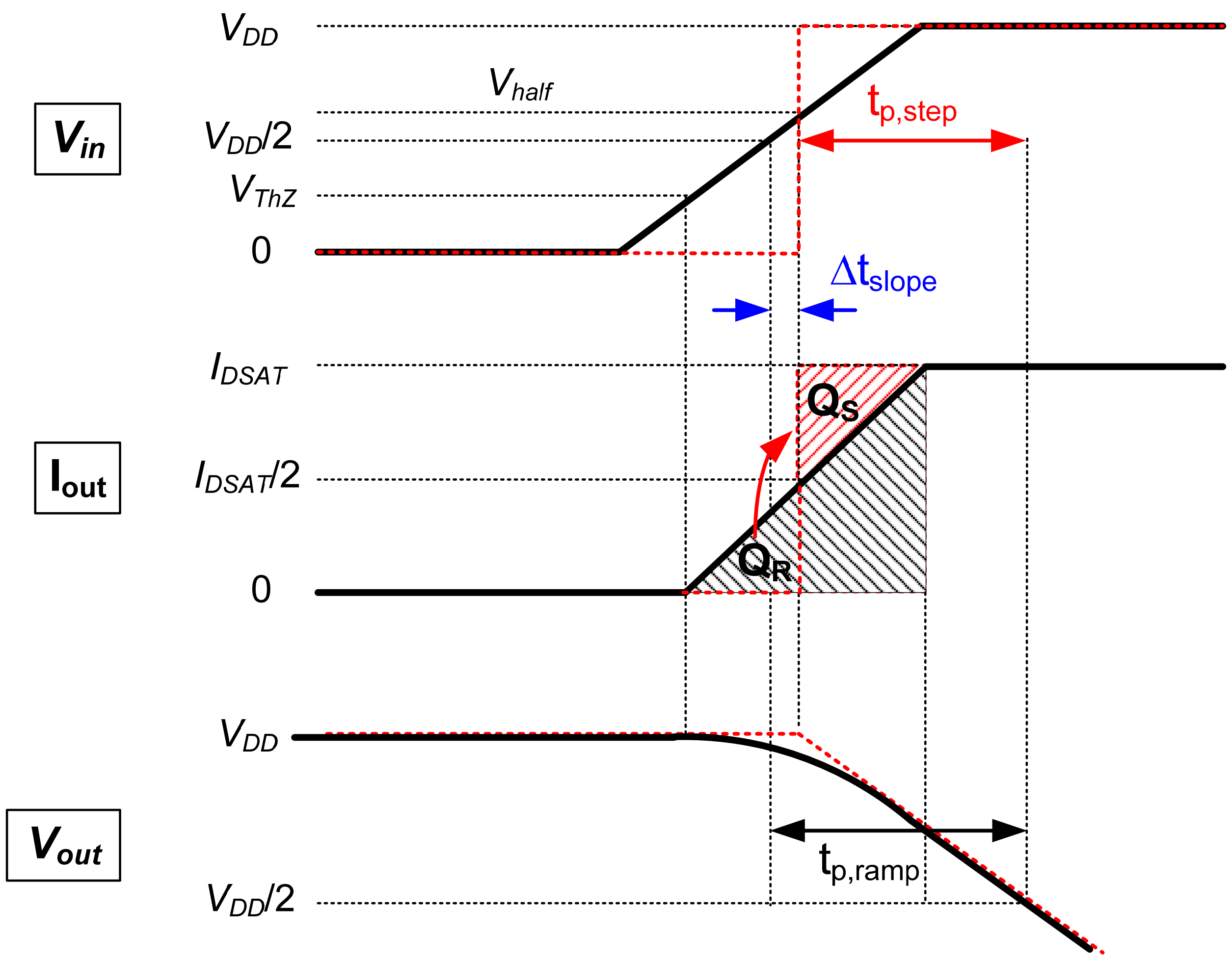


- I_{out} ramps linearly for $V_{ThZ}<V_{in}<V_{DD}$
  - Constant once $V_{in}=V_{DD}$

- C_L integrates I_{out}
  - $V_{ThZ}<V_{in}<V_{DD}$: V_{out} quadratic
  - $V_{in} = V_{DD}$: V_{out} linear

Slope Dependence

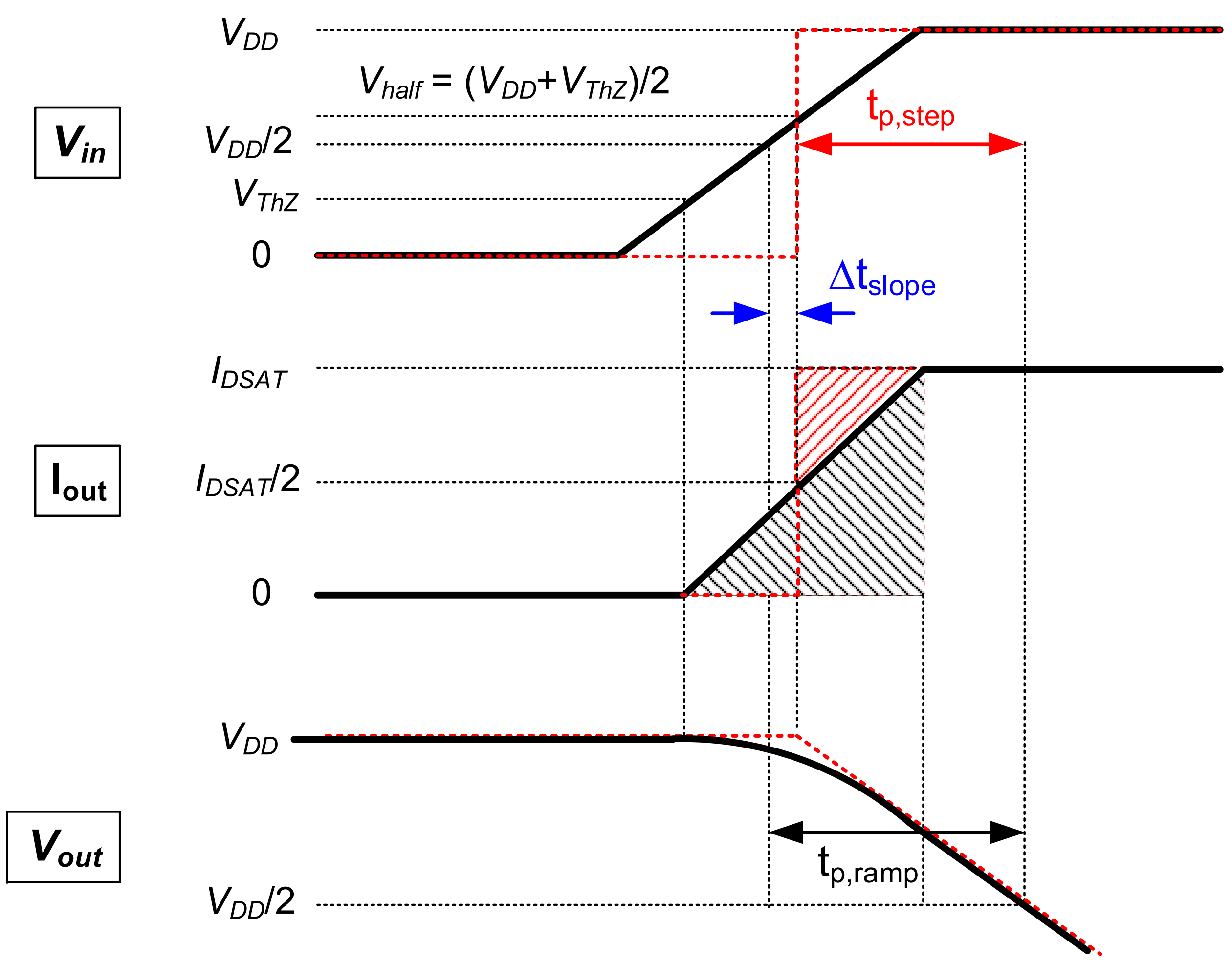
Slope Dependence



- Consider step input whose output crosses $V_{DD}/2$ at same time
- V_{out} set by charge removed from C_L
  - Need to make $Q_R = Q_S$
- Step has to shift to when $I_{out}=I_{DSAT}/2$

From E. Alon

Slope Dependence



$$t_{p,ramp} = t_{p,step} + \frac{V_{ThZ}/2}{k_r} = t_{p,step} + \frac{V_{ThZ}}{V_{DD}} t_{p,in}$$

- To find Δt_{slope}:
  - Find V_{in} when $I_{out} = I_{DSAT}/2$ (V_{half})
  - And use input t_r
- $I_{DSAT} \propto (V_{DD} - V_{ThZ})$:

  $V_{half} - V_{ThZ} = V_{DD}/2 - V_{ThZ}/2$

  $V_{half} = (V_{DD} + V_{ThZ})/2$
- So $\Delta t_{slope} = (V_{ThZ}/2)/k_r$
  - $k_r = V_{DD}/(t_{r,20\text{-}80}) = V_{DD}/(2 * t_{p,in})$

Result Summary

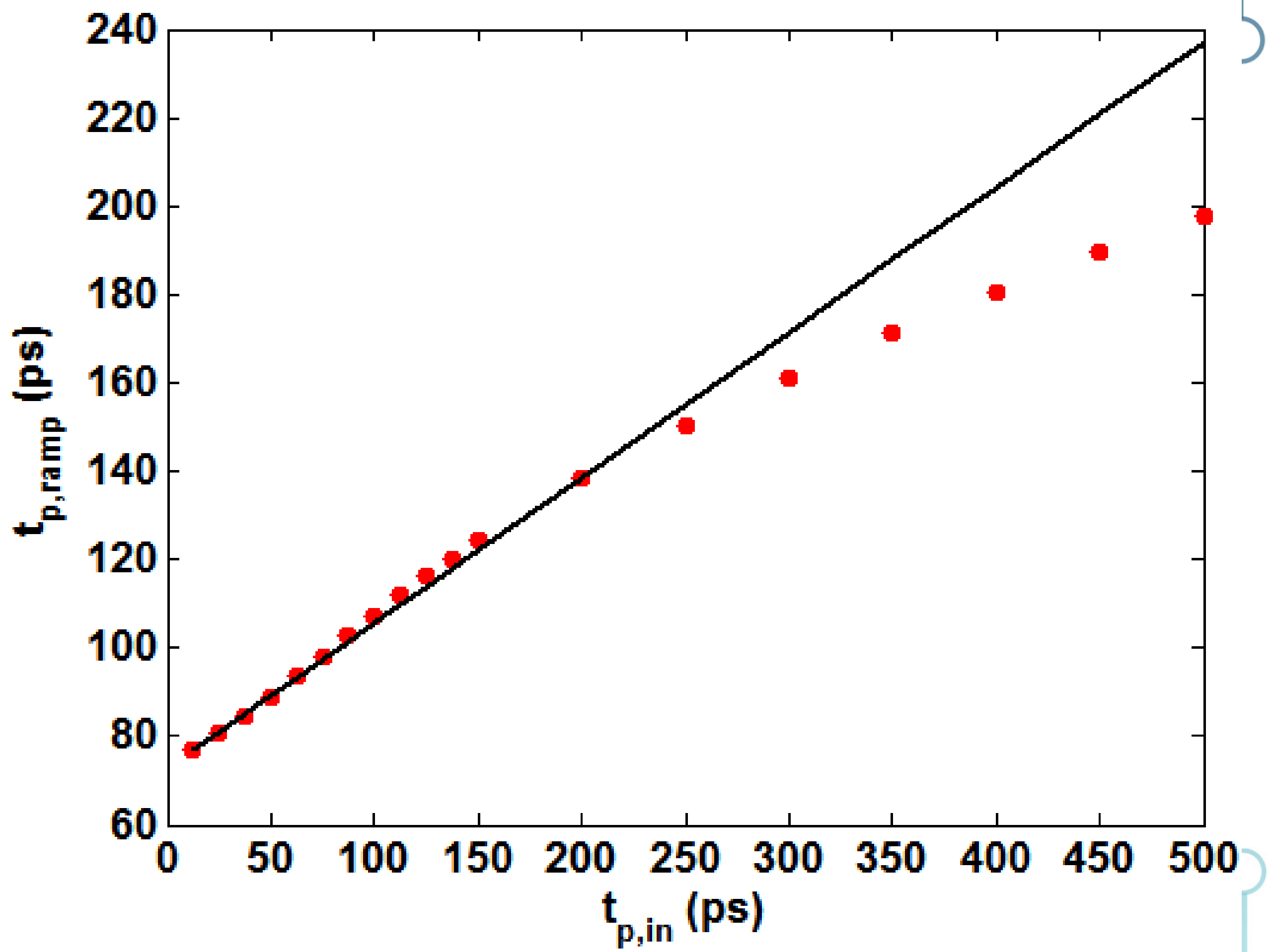
- For reasonable input slopes:

$$t_{p,ramp} = t_{p,step} + \frac{V_{ThZ}/2}{k_r} = t_{p,step} + \frac{V_{ThZ}}{V_{DD}} t_{p,in}$$

- For $t_{p,avg}$, V_{ThZ} is $(V_{ThZN} + V_{ThZP})/2$
  - V_{ThZ}/V_{DD} typically ~1/3-1/2 at nominal supplies
- Propagation delay is a function of
  - Drive strength (R_{eq})
  - Load (C_L)
  - Input rise/fall time (which is proportional to the propagation delay of the previous gate)

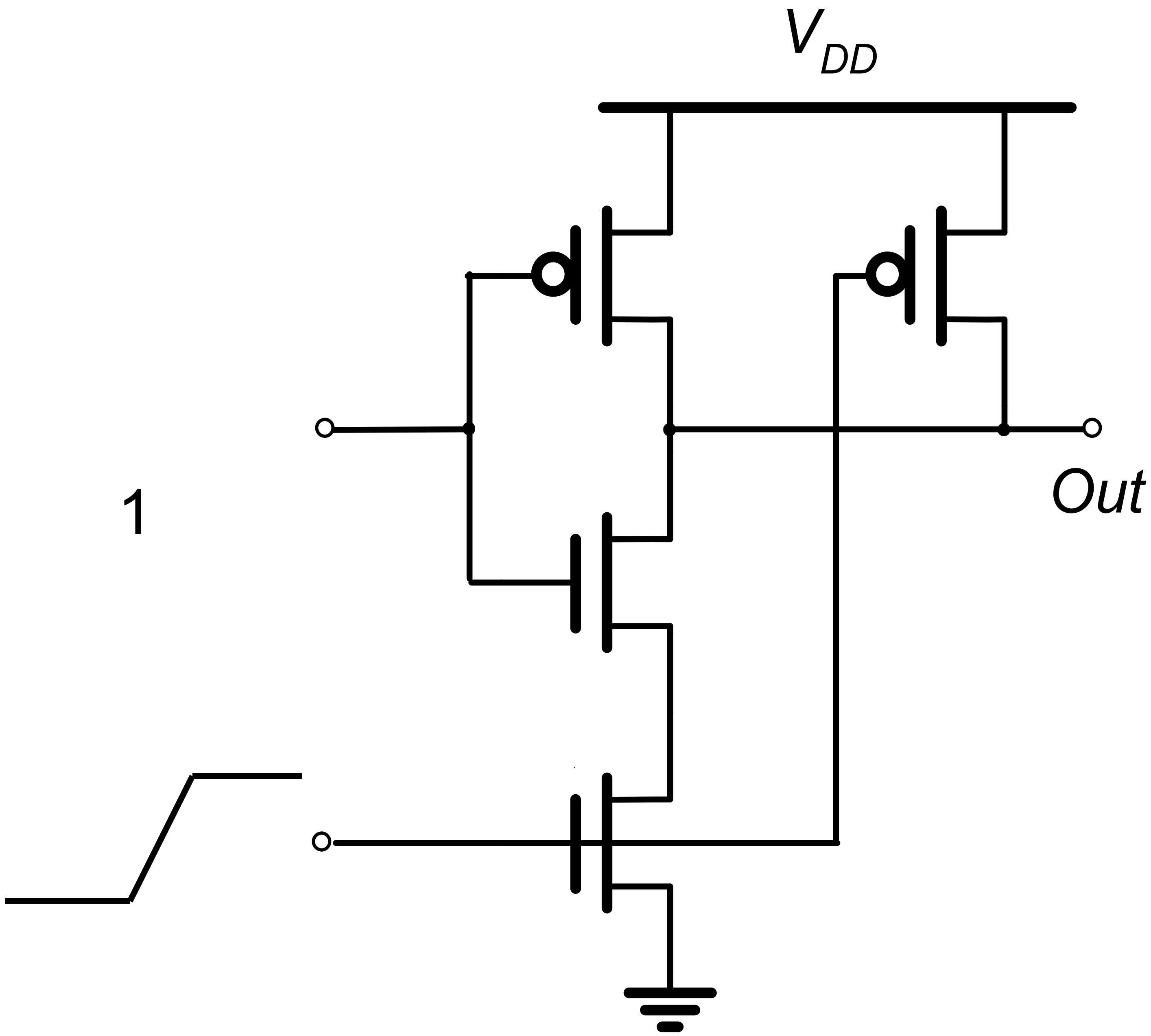
Model vs. Spice Data

- For reasonable input slope
  - Model matches Spice very well
- Model breaks with very large t_r
  - Input looks “DC” – traces out VTC
  - Have other problems here anyways
    - Short-circuit current



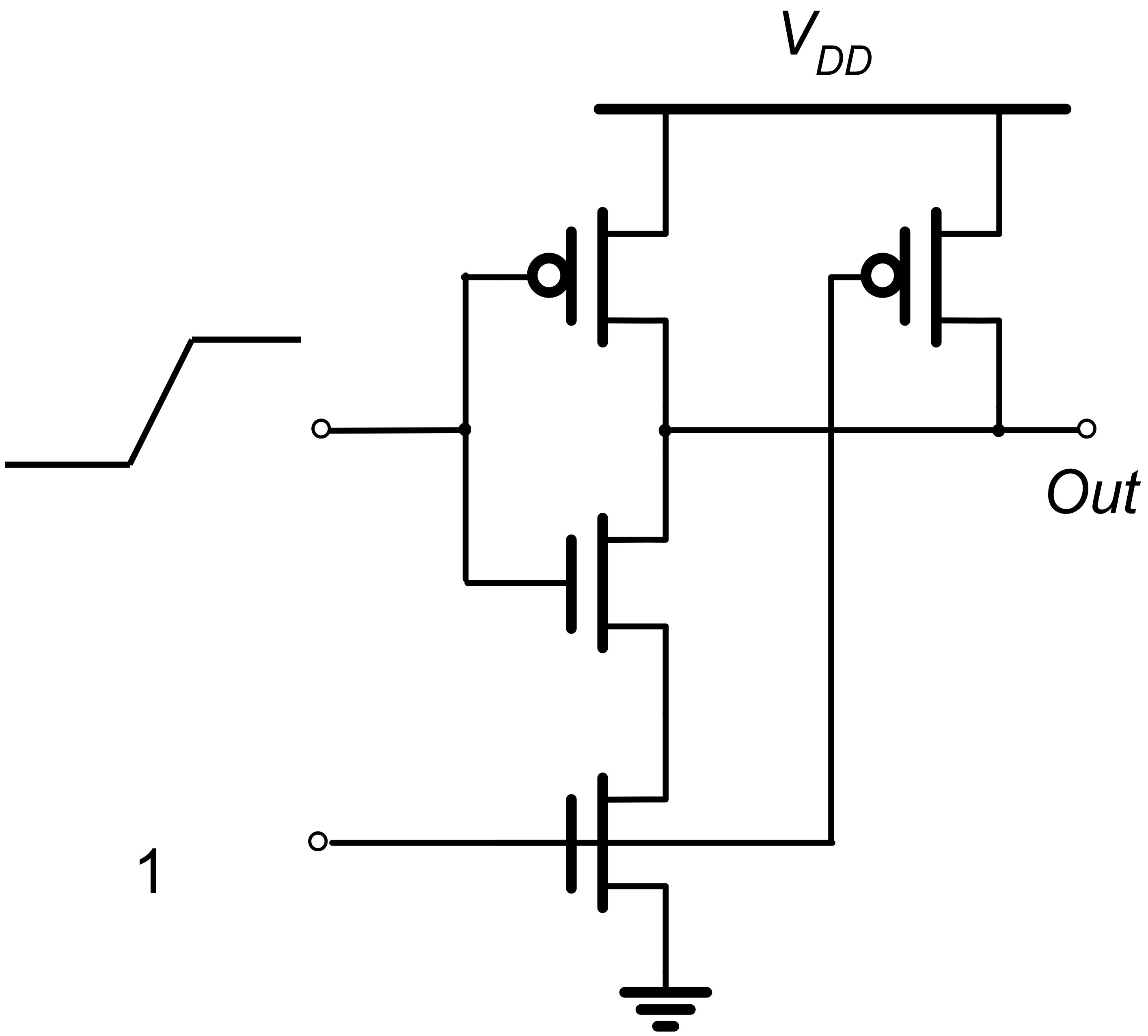
Signal Arrival Times

- NAND gate:



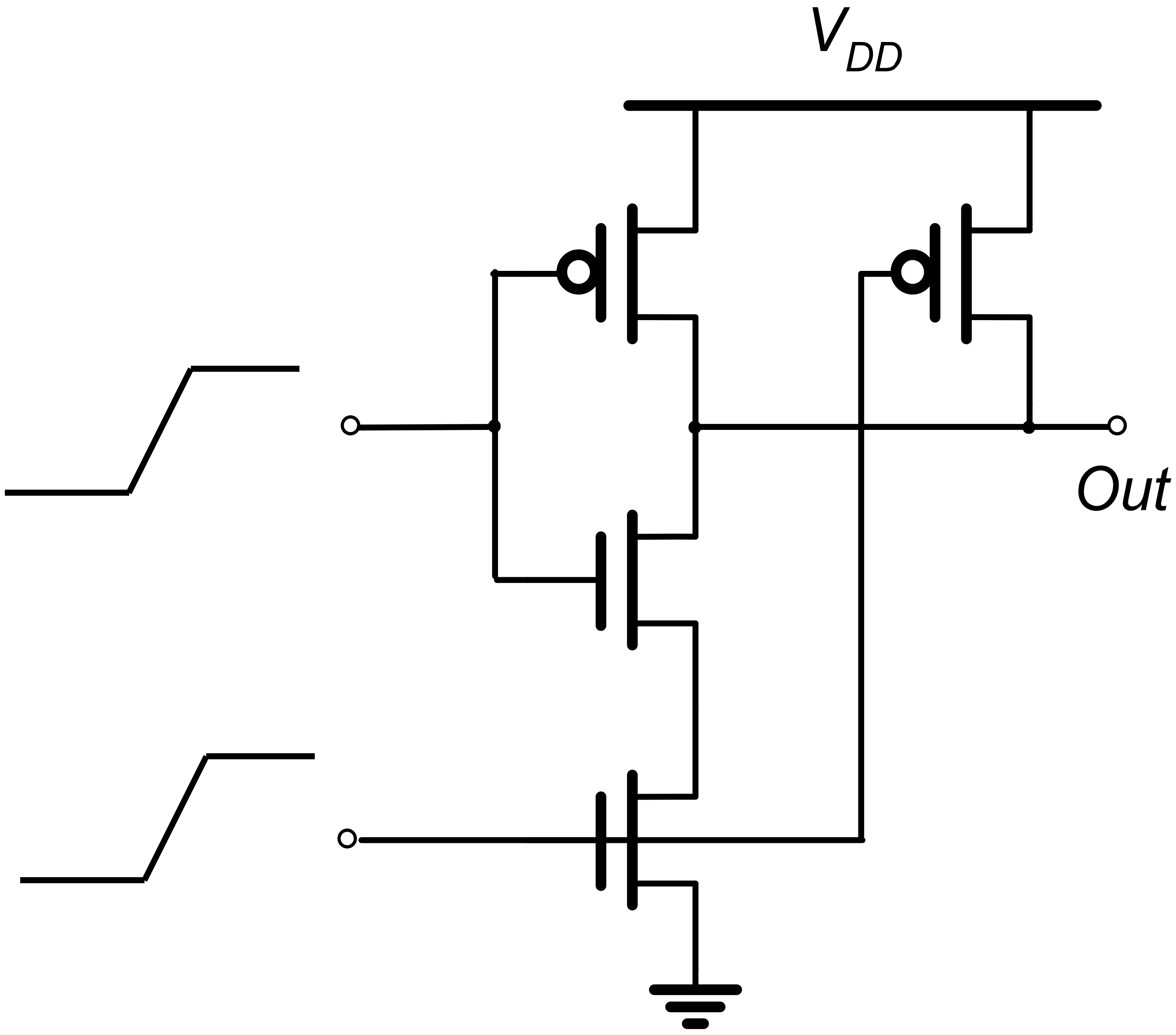
Signal Arrival Times

- NAND gate:

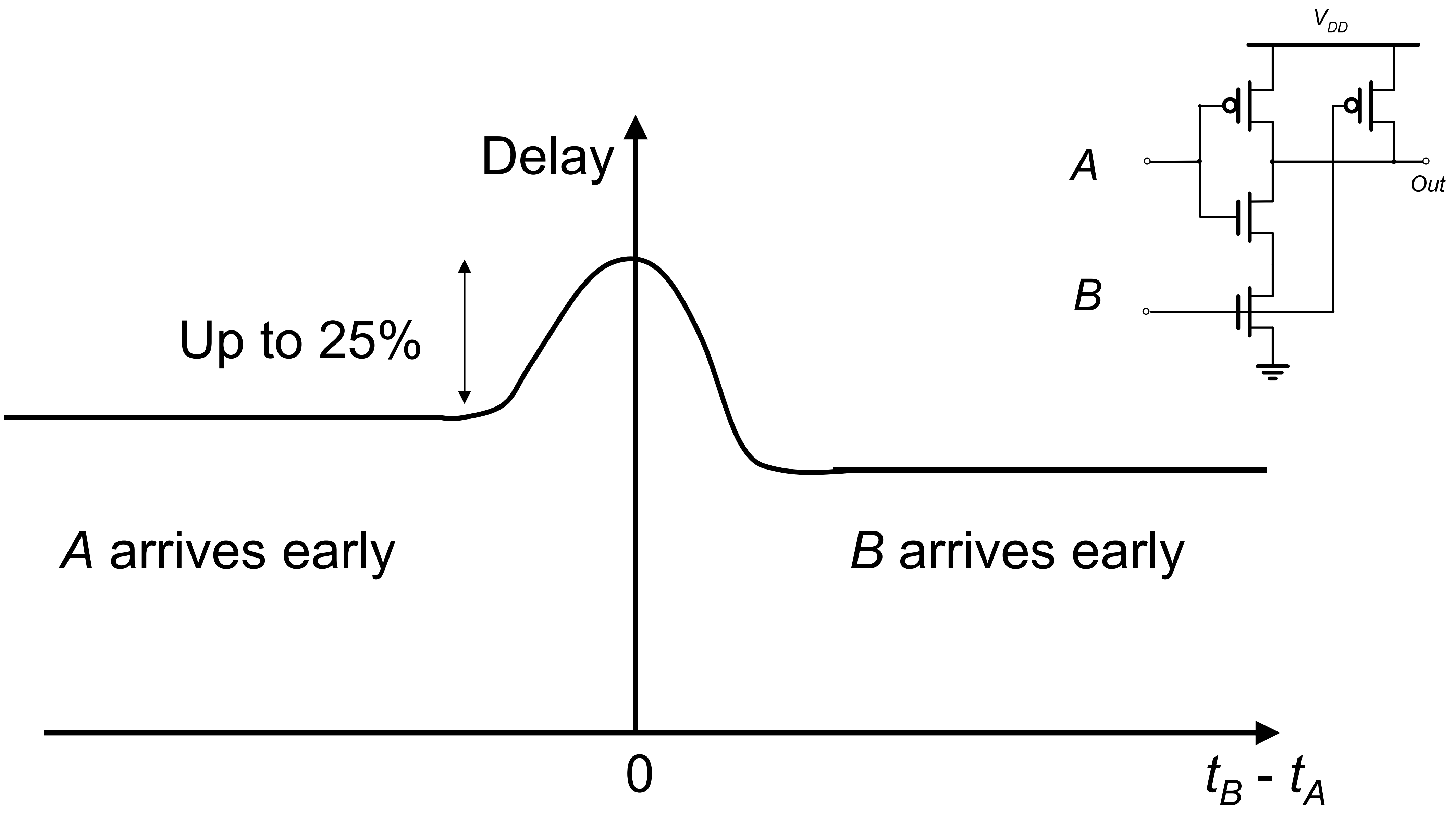


Simultaneous Arrival Times

- NAND gate:



Impact of Arrival Times



The edge can also advance in the opposite transition

Not in models; add derating during design

Key Point

- Timing of a cell is set by its load and input rise/fall time
  - Enables static delay computation
- Circuits described as graphs
  - Timing as a graph solving problem

2.M Standard Cell Library

Standard Cell Library

- Contains for each cell:
  - Functional information: cell = a *b * c
  - Timing information: function of
    - input slew
    - intrinsic delay
    - output capacitance

    non-linear models used in tabular approach
  - Physical footprint (area)
  - Power characteristics
  - Noise senistivity
- Wire-load models - function of
  - Block size
  - Fan-out

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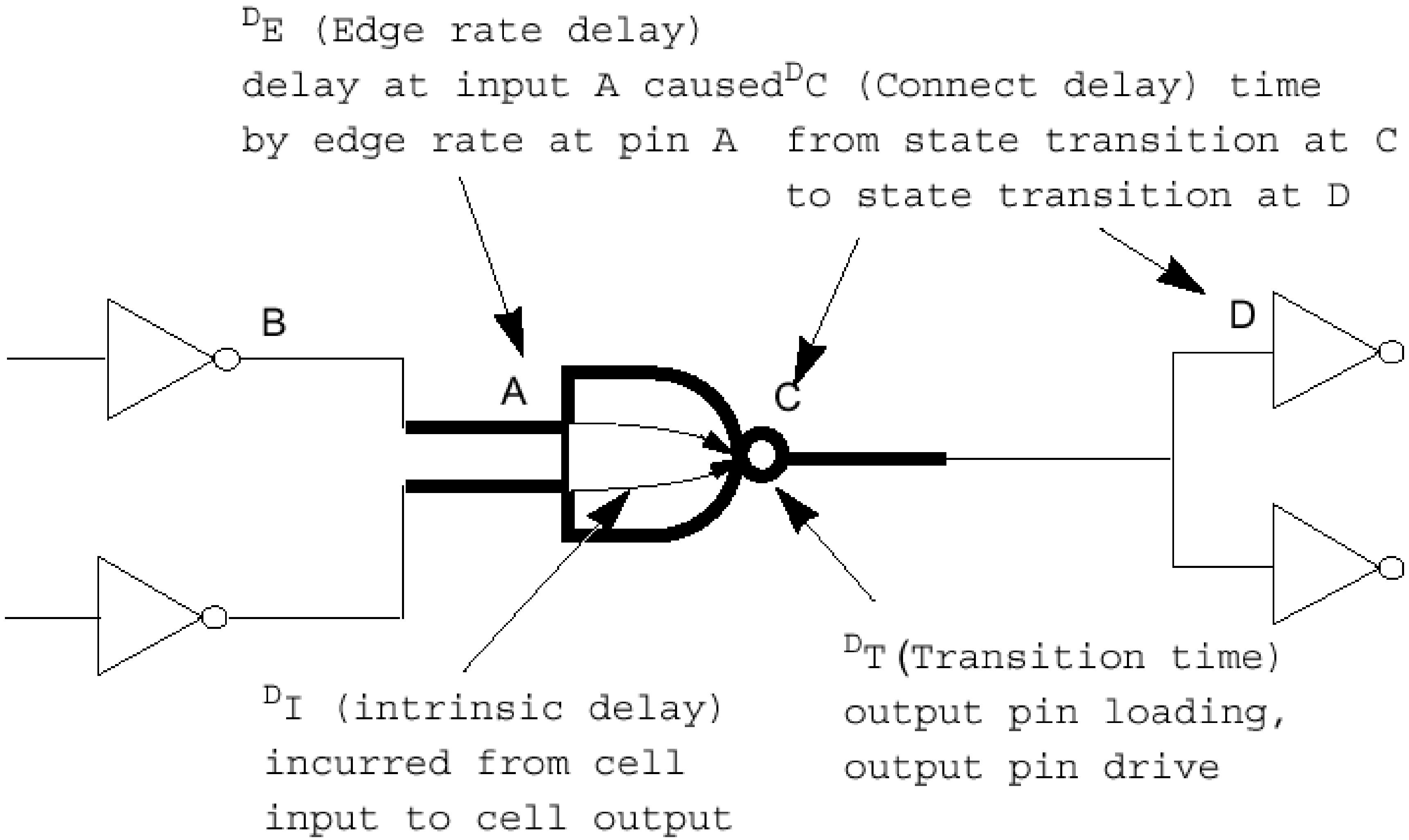
Synopsys Delay Models

- Linear (CMOS2) delay model



Example Cell Timing

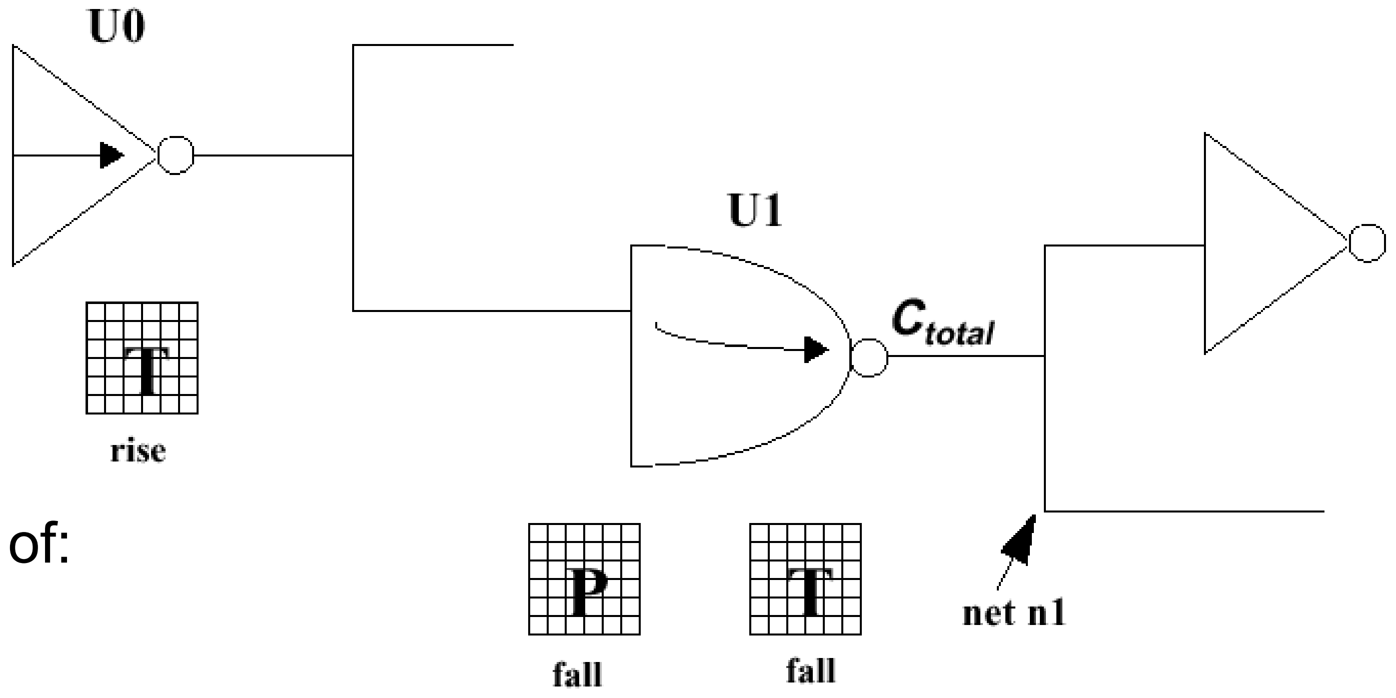
- From Synopsys training materials

```
From pin: U28/A
To pin: U28/Z

arc type :                      cell
arc sense :                     unate
Input net transition times:     Dt_rise = 0.1458, Dt_fall = 0.0653

Rise Delay computation:
rise_intrinsic                  0.48 +
rise_slope * Dt_rise            0 * 0.1458 +
rise_resistance * (pin_cap + wire_cap) / driver_count
0.1443 * (2 + 0) / 1
rise_transition_delay :         0.2886
------------------------------------
Total                           0.7686
```

Cell Characterization (Linear Model)

```
cell(NAND2) {
  area : 1;
  pin(X) {
    function : "(A B)'";
    direction : output;
    edge_rate_rise : 0.24;
    edge_rate_fall : 0.14;
    edge_rate_load_rise : 5.4;
    edge_rate_load_fall : 3.4;
    timing() {
    intrinsic_rise  : 0.34;
    intrinsic_fall  : 0.24;
    rise_resistance : 3.4;
    fall_resistance : 1.4;
    edge_rate_sensitivity_r0 : 0.24;
    edge_rate_sensitivity_f0 : 0.14;
    edge_rate_sensitivity_r1 : 0.14;
    edge_rate_sensitivity_f1 : 0.04;
    related_pin : "A";
    }
    timing() {
    intrinsic_rise  : 0.34;
    intrinsic_fall  : 0.24;
    rise_resistance : 3.4;
    fall_resistance : 1.4;
    edge_rate_sensitivity_r0 : 0.24;
    edge_rate_sensitivity_f0 : 0.14;
    edge_rate_sensitivity_r1 : 0.14;
    edge_rate_sensitivity_f1 : 0.04;
    related_pin : "B";
    }
  }
  pin(A) {
    direction : input;
    capacitance : 0.10;
  }
  pin(B) {
    direction : input;
    capacitance : 0.10;
  }
}
```

Synopsys Nonlinear Delay Model (NLDM)

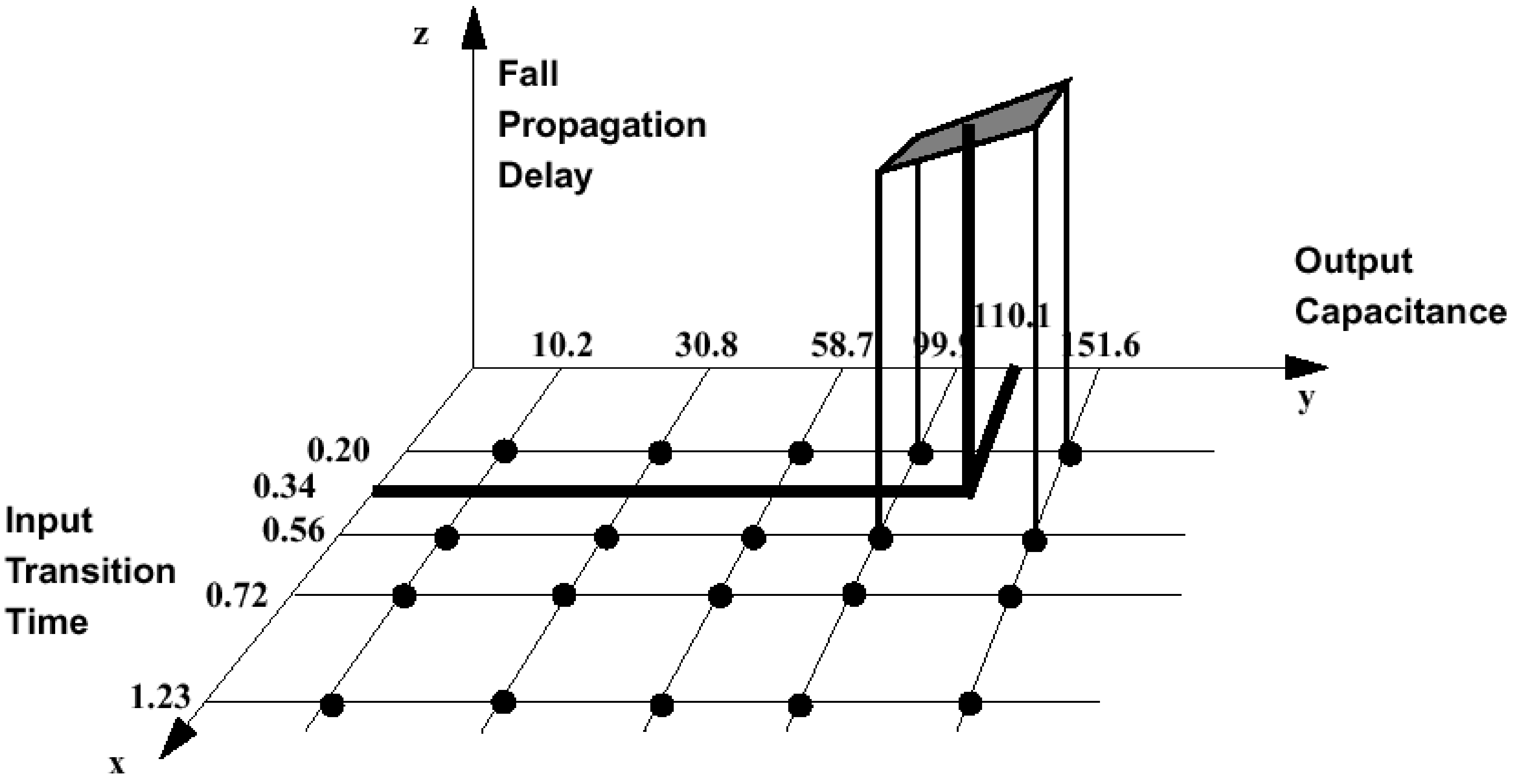


Delay is a function of:

- Rise propagation
- Cell rise
- Fall propagation
- Cell fall
- Rise transition
- Fall transition

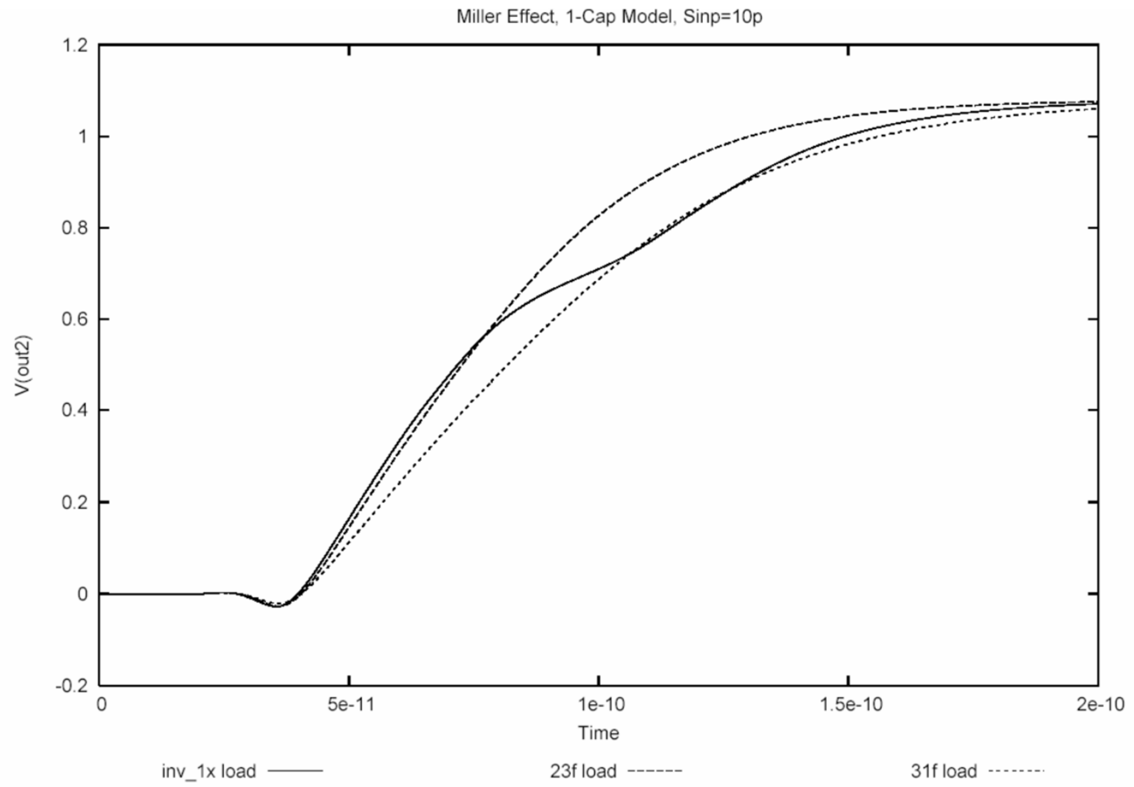
Synopsys Nonlinear Delay Model

- Interpolates between characterization points

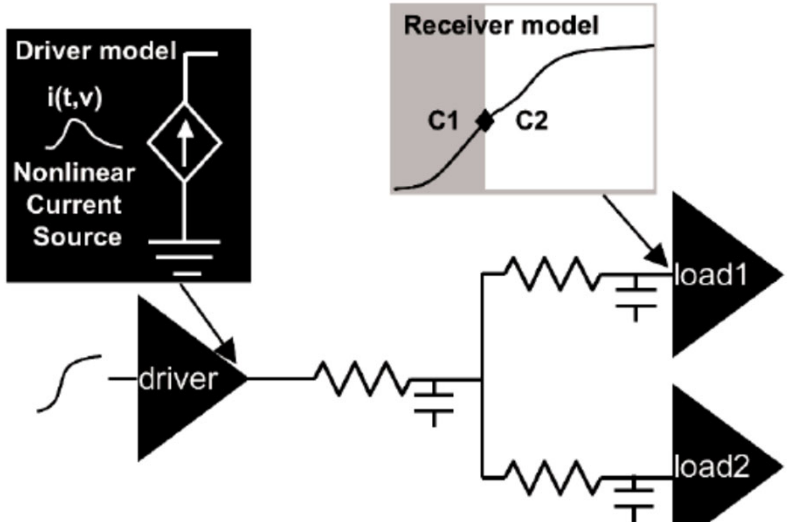


Composite Current Source (CCS) Model

- **Driver model**
  - Composite current source (time and voltage dependent)
- **Receiver model**
  - A set of capacitance models
  - Wire model
- **Interpolate**



Matches both delay and rise/fall times



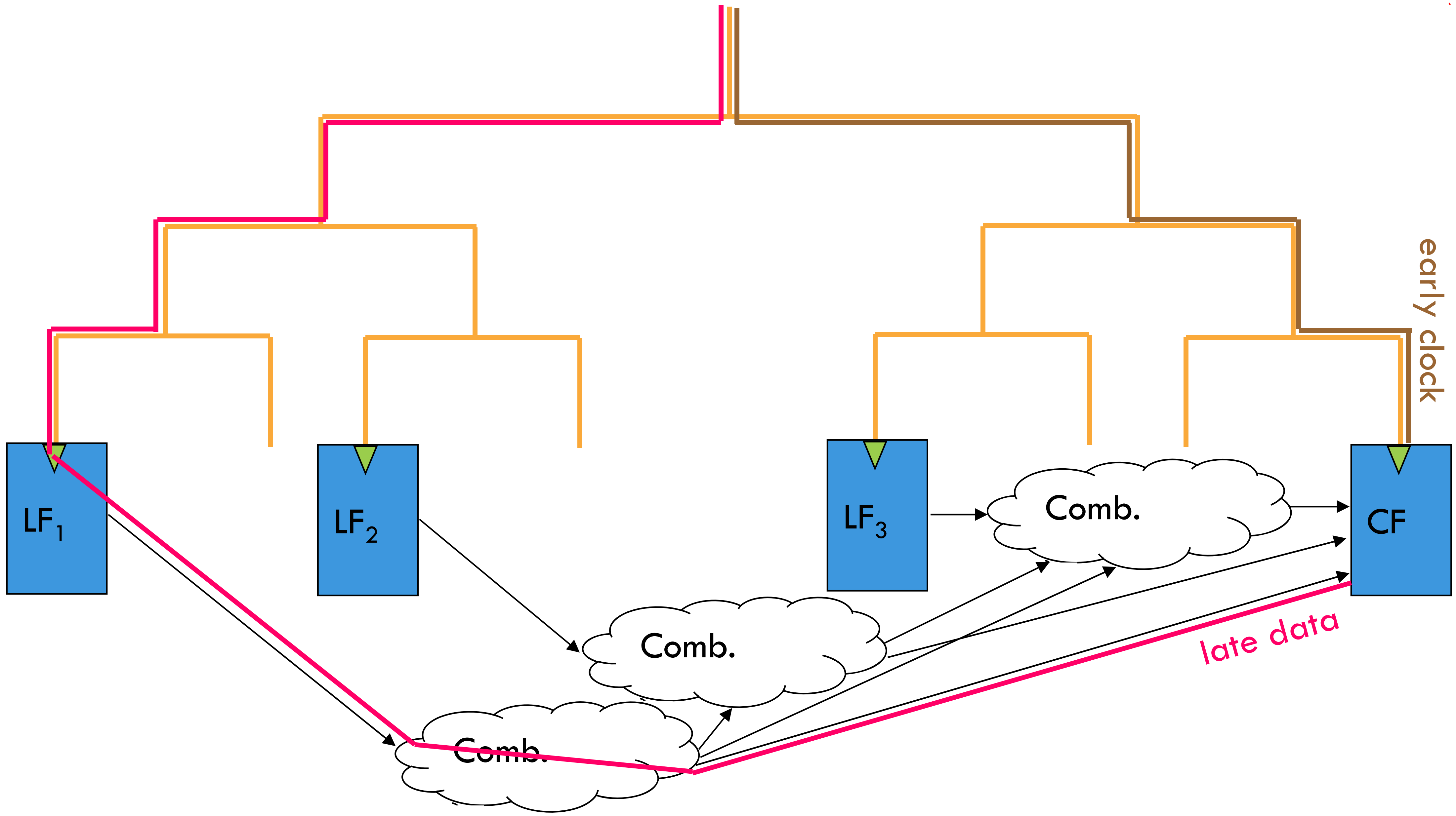
Synopsys

2.N Static Timing

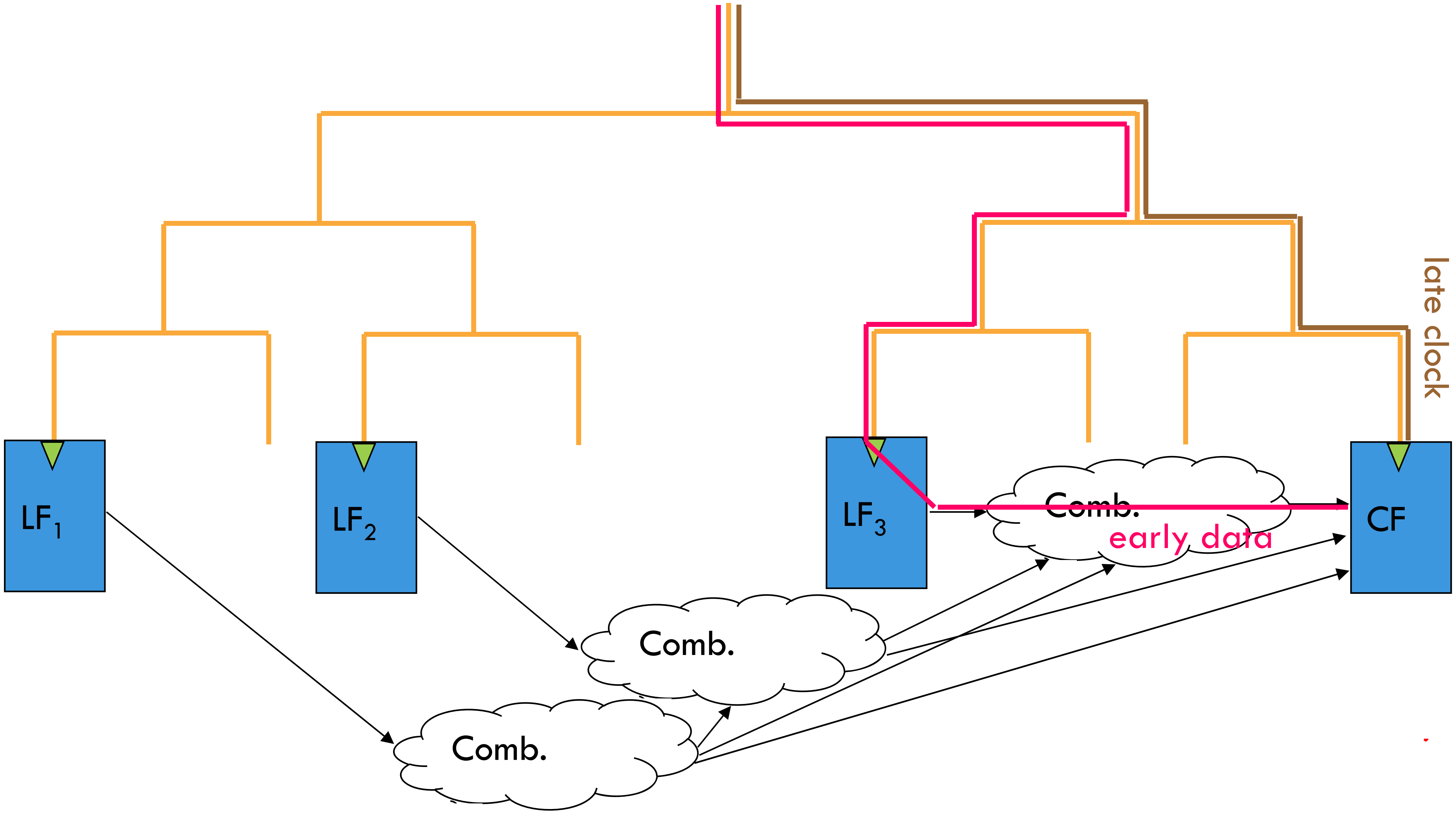
Static Timing

- Pin-to-pin arc delay model
  - Propagates both delay and slew
- Builds a timing graph
- Solves the graph for late and early signal arrivals
  - Compares to early and late clock arrivals

Setup Timing



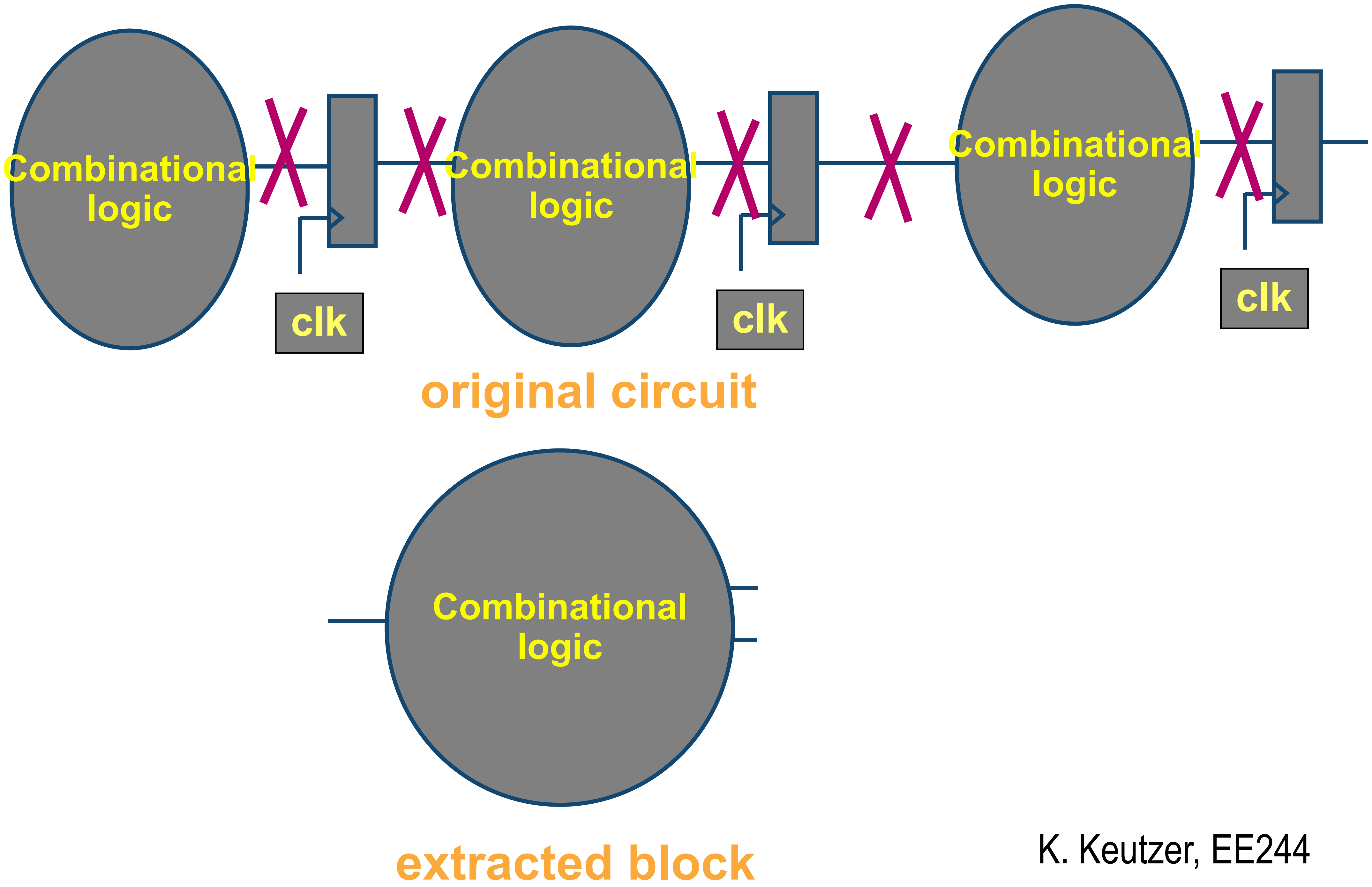
Hold Tests



C. Visweswariah, ICCAD'07 tutorial

Timing Constraints

Static Timing Analysis



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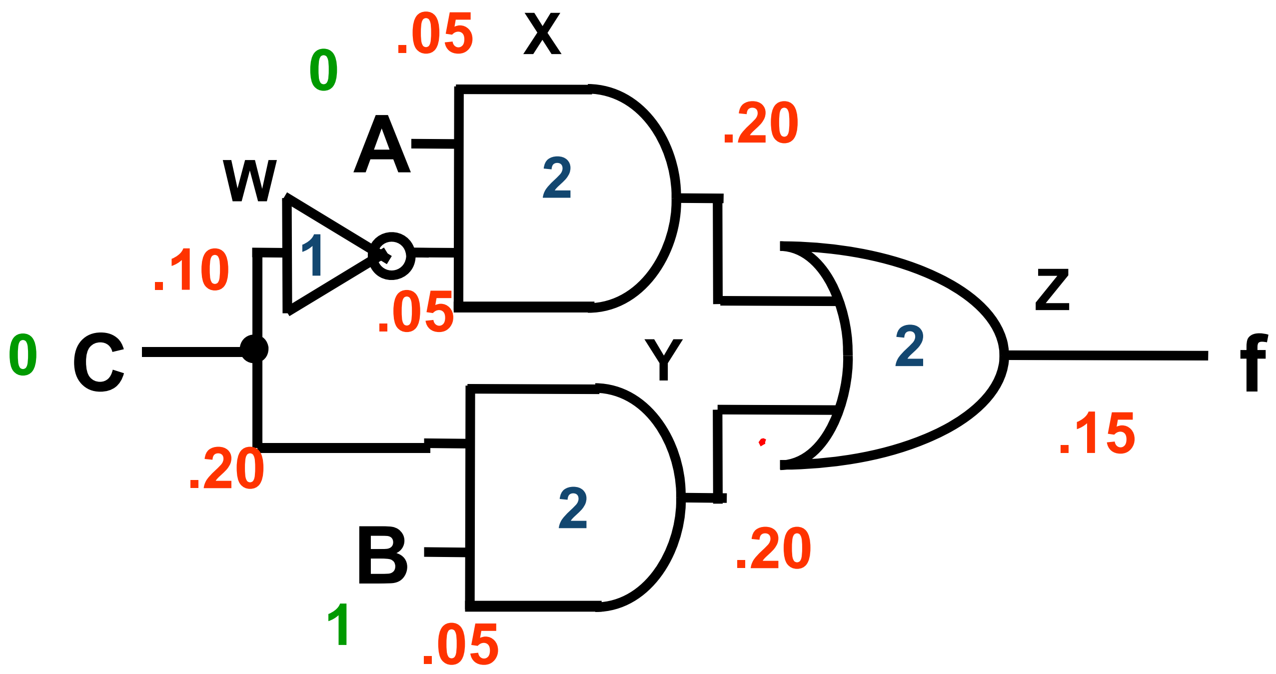
Each Combinational Block

- Arrival time in green



- Interconnect delay in red

- Gate delay in blue

- **What's the right mathematical object to use to represent this physical object?**

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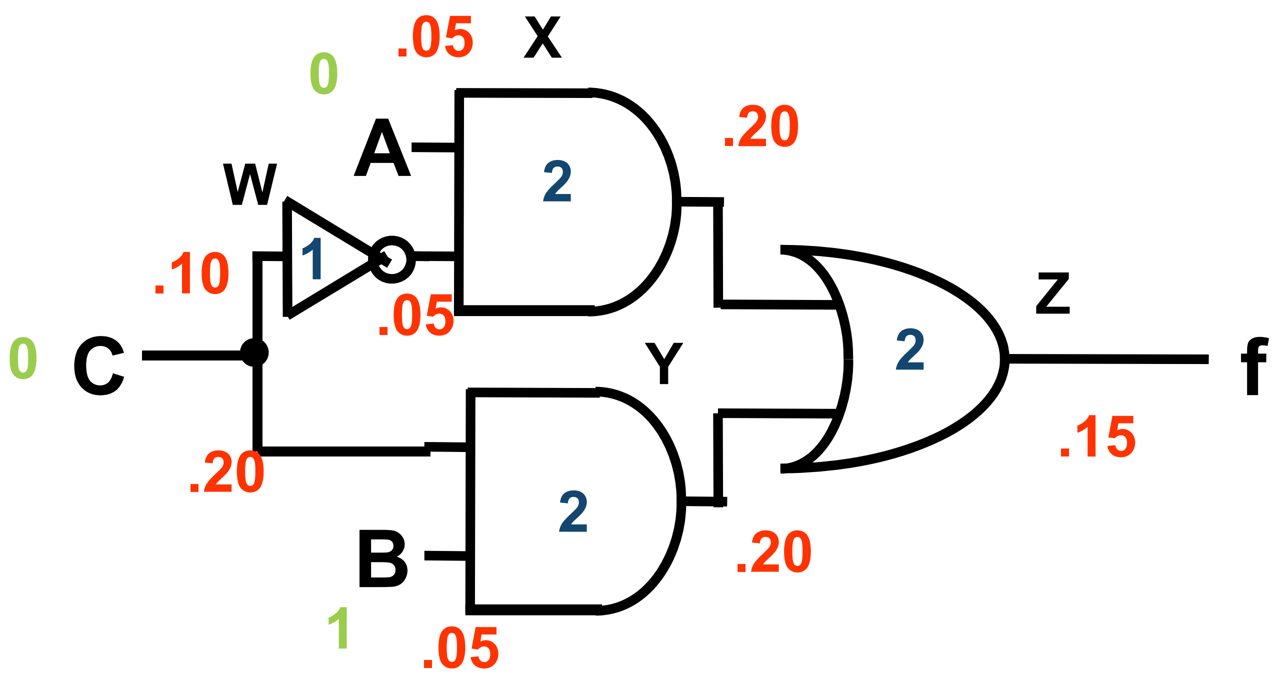
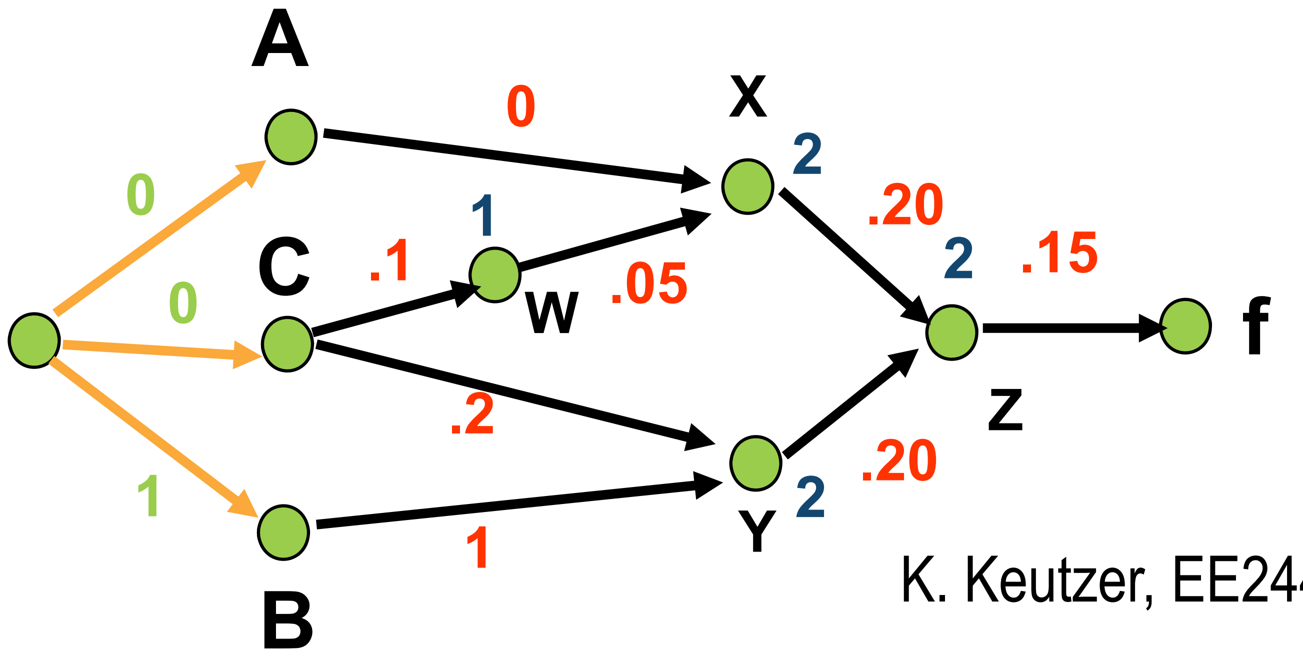
Problem formulation - 1

- Use a labeled *directed* graph
- $G = <V,E>$
- *Vertices* represent gates, primary inputs and primary outputs
- *Edges* represent wires
- *Labels* represent delays
- Now what do we do with this?





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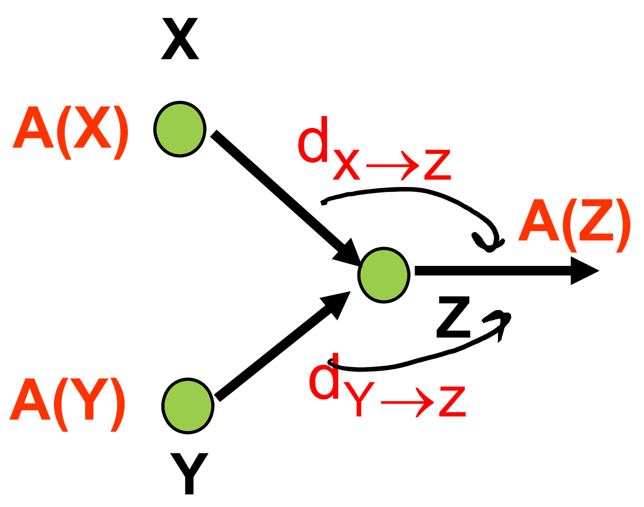
Problem formulation - Arrival Time

- Arrival time A(v) for a node v is time when signal arrives at node v



$$A(\upsilon) = \max_{u \in FI(\upsilon)} (A(u) + d_{u\rightarrow\upsilon})$$

where $d_{\upsilon\rightarrow u}$ is delay from υ to u, *FI(u)* = {X, Y}, **and** υ = {Z}.

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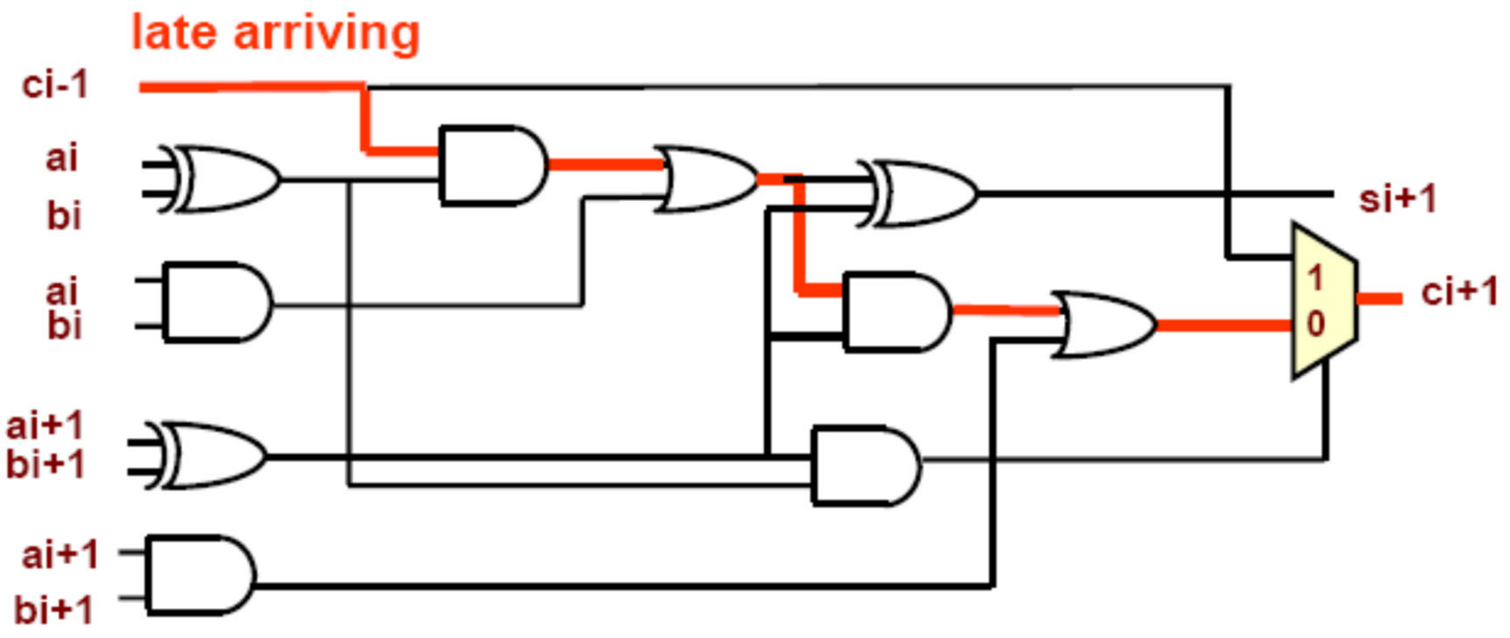
Static Timing Analysis

- Computing critical (longest) and shortest path delay
  - Longest path algorithm on DAG [Kirkpatrick, IBM Jo. R&D, 1966]
- Used in most ASIC designs today
- Limitations
  - False paths
  - Simultaneous arrival times
    - Derate

False Paths

Inside Carry Bypass Adder - 1



Longest graphical/topological path runs along carry chain from stage to stage

Longest path analysis would identify red path as critical

Static Timing - Summary

- Enables design of complex systems
- Simpler, less accurate models are used during design
- More accurate models are used for 'signoff'
- See more in labs!

Next Lecture

- Technology variability