inst.eecs.berkeley.edu/~ee241b

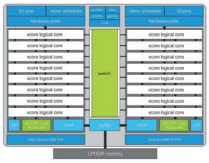
EE241B : Advanced Digital Circuits

Lecture 8 – Technology Variability

Borivoje Nikolić

February 2, 2020, EETimes: XMOS adapts Xcore into AIoT 'crossover processor'

The new chip targets AI-powered voice interfaces in IoT devices — "the most important AI workload at the endpoint.".



Announcements

- Homework 1 due on February 17
- No class on February 18 (ISSCC)
- Project abstracts due on February 20
  - Teams of 2
  - Title
  - One paragraph
  - 5 relevant references
- Can also combine with CS252 or EE290 projects

Outline

- Module 2
  - Technology variability

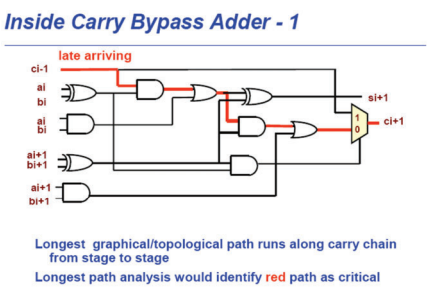
2.N Static Timing

Static Timing Analysis

- Computing critical (longest) and shortest path delay
  - Longest path algorithm on DAG [Kirkpatrick, IBM Jo. R&D, 1966]
- Used in most ASIC designs today
- Limitations
  - False paths
  - Simultaneous arrival times
    - Derate

Timing Constraints

False Paths



Static Timing - Summary

- Enables design of complex systems
- Simpler, less accurate models are used during design
- More accurate models are used for 'signoff'
- See more in labs!

2.O Design Variability Sources and Impact on Design

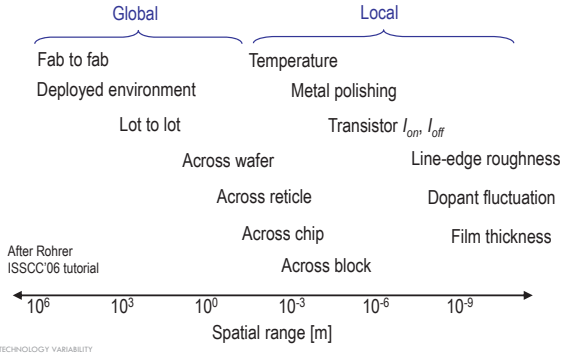
Variability Classification

- Nature of process variability
  - Within-die (WID), Die-to-die (D2D), Wafer-to-wafer (W2W), Lot-to-lot (L2L)
  - Systematic vs. random
  - Correlated vs. non-correlated
- Spatial variability/correlation
  - Device parameters (CD, t_{ox}, …)
  - Supply voltage, temperature
- Temporal variability/correlation
  - Within-node scaling, Electromigration, Hot-electron effect, NBTI, self-heating, temperature, SOI history effect, supply voltage, crosstalk
    [Bernstein, IBM J. R&D, July/Sept 2006]
- Known vs. unknown
  - Goal of model-to-hw correlation is to reduce the unknowns

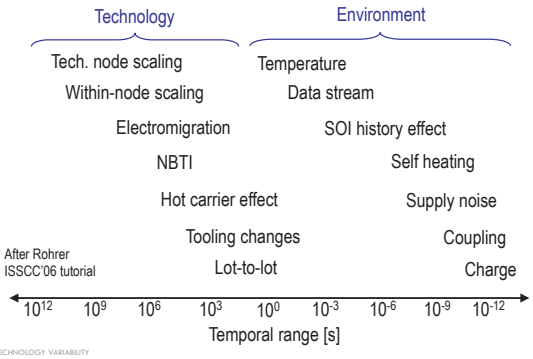
Sources of Variability

- Technology
  - Front-end (Devices)
    - Systematic and random variations in Ion, Ioff, C, …
  - Back-end (Interconnect)
    - Systematic and random variations in R, C
- Environment
  - Supply (IR drop, noise)
  - Temperature

Spatial Variability



Temporal Variability



Systematic vs. Random Variations

- Systematic
  - A systematic pattern can be traced down to lot-to-lot, wafer-to-wafer, within reticle, within die, from layout to layout,…
  - Within-die: usually spatially correlated
- Random
  - Random mismatch (dopant fluctuations, line edge roughness,…)
  - Things that are systematic, but e.g. change with a very short time constant (for us to do anything about it). Or we don't unedrstand it well enough to model it as systematic. Or we don't know it in advance ("How random is a coin toss?").
- Unknown

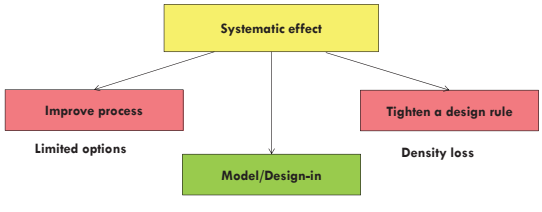
Systematic and Random Device Variations

Parameter	Random	Systematic
Channel Dopant Concentration Nch	Affects δ_{VT} [1] 	Non uniformity in the process of dopant implantation, dosage, diffusion
Gate Oxide Thickness Tox	Si/SiO_2 & SiO_2/Poly-Si interface roughness[2] 	Non uniformity in the process of oxide growth
Threshold Voltage V_T (non Nch related)	Random anneal temperature and strain effects	Non-uniform annealing temperature[5] (metal coverage over gate) Biaxial strain
Mobility μ	Random strain distributions	Systematic variation of strain in the Si due to STI, S/D area, contacts, gate density, etc
Gate Length L	Line edge roughness (LER)[3] 	Lithography and etching: Proximity effects, orientation[4]
Fin geometry/ film thickness variations	Rounding, etc, δ_{VT}, mobility.	Systematic fin thickness Systematic Si film/BOX variations

[1] D. Frank et al, *VLSI Symposium*, Jun. 1999 . [2] A. Asenov et al, *IEEE Trans on Electron Devices*, Jan. 2002.
[3] P. Oldiges et al, SISPAD 2000, Sept. 2000. [4] M. Orshansky et al, *IEEE Trans on CAD*, May 2002. [5] Tuinhout et al, *IEDM*, Dec 1996

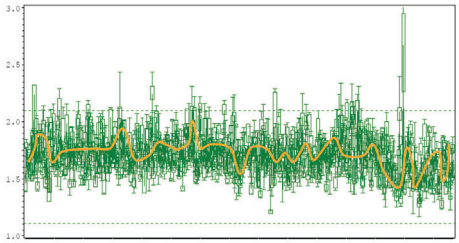
Dealing with Systematic Variations

- Model-to-hardware correlation classifies unknown sources



Systematic (?) Temporal Variability

Metal 3 resistance over 3 months

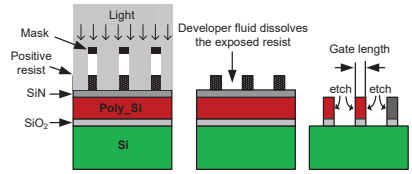


P. Habitz, DAC'06 tutorial

2.P Design Variability
Some Systematic Effects

Layout: Poly Proximity Effects

- Gate CD is a function of its neighborhood



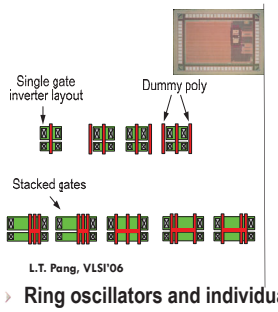
Gate length depends on

- **Light intensity profile falling on the resist**
- **Resist: application of developer fluid[1], post exposure bake (PEB) temperature[2]**
- **Dry etching: microscopic loading effects[3]**

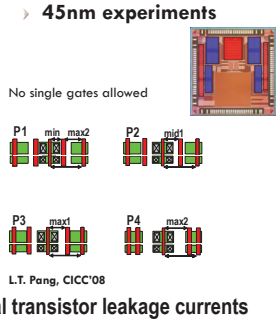
[1] J.Cain, M.S. Thesis, UC Berkeley
[2] D. Steele et al, *SPIE*, vol.4689, July 2002.
[3] J. D. Plummer, M.D. Deal, P.B. Griffin, Silicon VLSI Technology, Prentice-Hall, 2000.

Layout: Proximity Test Structures

- 90nm experiments

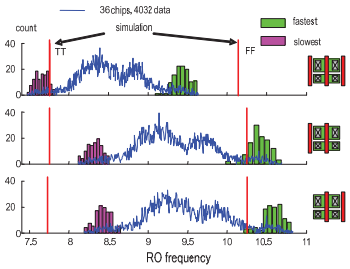


- **45nm experiments**



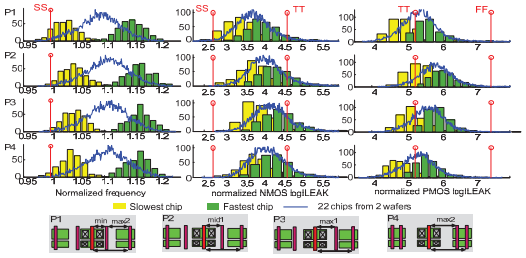
- **Ring oscillators and individual transistor leakage currents**

Results: Single Gates in 90nm



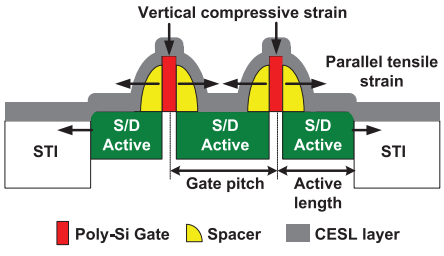
- **Max ΔF between layouts > 10%**
- **Within-die 3σ/μ ~ 3.5%, weak dependency on density**

Results: Single Gates in 45nm



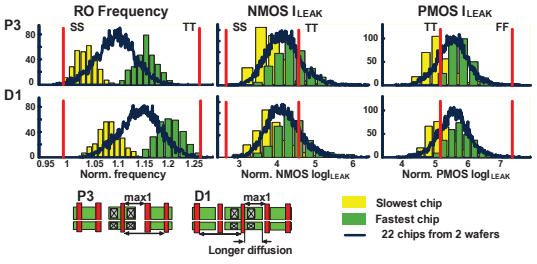
- **Weak effect on performance. ΔF ~ 2%**
- **Small shifts in NMOS leakage and bigger shifts in PMOS leakage**

Impact of Stress



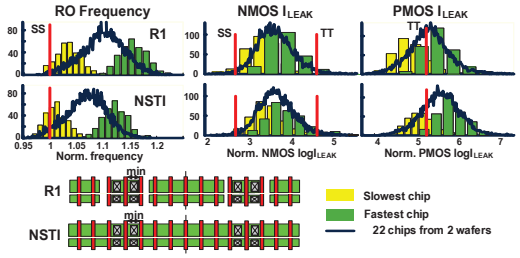
- **45nm STM process: Wafer rotated <100> - higher PMOS mobility**
- **NMOS strained through capping layer**
- **Subatmospheric STI – weak tensile stress**

Impact of Longer Diffusion in 45nm



- **Strongest effect measured in 45nm, ΔF ~ 5%**
- **No significant shift in I_{LEAK}**

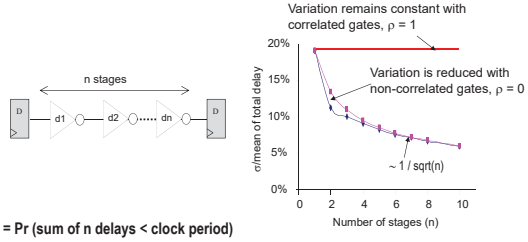
Impact of Shallow Trench Isolation (STI)



- ΔF ~ 3%, small changes in I_{LEAK}
- Due to STI-induced stress

Impact of Correlations

Chip Yield Depends on Inter-Gate Correlation

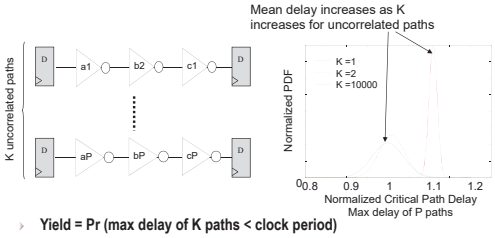


- Yield = Pr (sum of n delays < clock period)
- ρ = 0 gives highest yield through averaging

Non-correlated gates in a path reduce impact of variation

Bowman et al, *JSSC*, Feb 2002 .

Chip Yield Depends on Inter-Path Correlation



- Yield = Pr (max delay of K paths < clock period)
- K = 1 gives highest yield

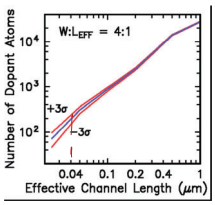
Correlated paths reduce impact of variation

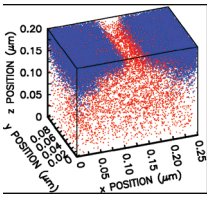
Bowman et al, *JSSC*, Feb 2002 .

2.P Design Variability
Some Random Effects

Random Dopant Fluctuations

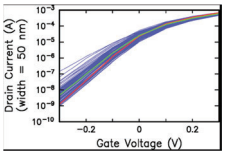
- Number of dopants is finite



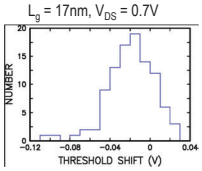


Frank, IBM J R&D 2002

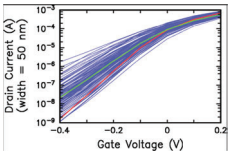
Random Dopant Fluctuations



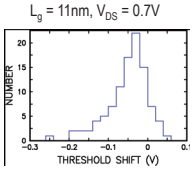
L_g = 17nm, V_{DS} = 0.7V



σ_{VT} = 23mV

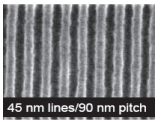


L_g = 11nm, V_{DS} = 0.7V



σ_{VT} = 52mV

Processing: Line-Edge Roughness

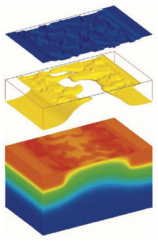


•Sources of line-edge roughness:
- Fluctuations in the total dose due to quantization
- Resist composition
- Absorption positions

Effect:
- Variation (random) in leakage and power

Oxide Thickness

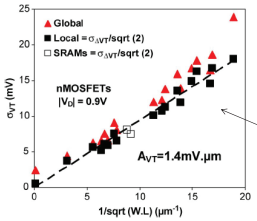
- Systematic variations +
- Roughness in the Si./SiO2 interface
- Smaller effect than RDF



Asenov, TED'2002

Transistor Matching

- V_{Th} matching of geometrically identical transistors varies with size $\sim\sqrt{WL}$ and distance



Pelgrom parameter A_{VT} - Scales with technology (EOT)

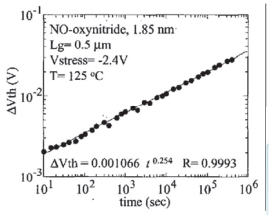
A_{VT} in FDSOI technology

J. Mazurier, Trans E.D., 2011.

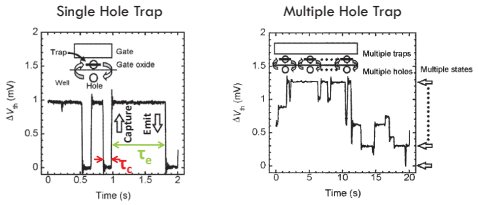
Negative Bias Temperature Instability

- PFET V_{Th}'s shift in time, at high negative bias and elevated temperatures
- The mechanism is thought to be the breaking of hydrogen-silicon bonds at the Si/SiO2 interface, creating surface traps and injecting positive hydrogen-related species into the oxide.
- Also other charge trapping and hot-carrier defect generation
- Systematic + random shifts

Tsujikawa, IRPS'2003



Random Telegraph Signal (RTS)



- Trapping of a carrier in oxide traps modulates V_{th} or I_{ds}
- τ_e and τ_c are random and follow exponential distributions

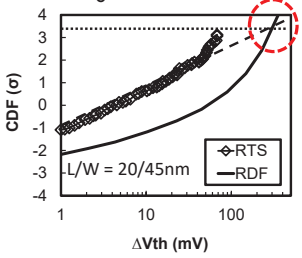
N. Tega et al, IRPS 2008.

RTS and Technology Scaling

- RTS exceeds RDF at 3 sigma with 20nm gates

$$\Delta V_{th,\,RTS} \sim \frac{1}{WL}$$

$$\Delta V_{th,\,RDF} \sim \frac{1}{\sqrt{WL}}$$



Tega *et. al*, VLSI Tech. 09

Next Lecture

- Timing and design for performance
  - After ISSCC