

Homework 1 Solutions

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Credit to students Wahid Rahman and Dan Fritchman for solution figures
EE241B

1 Models

a Threshold Voltage

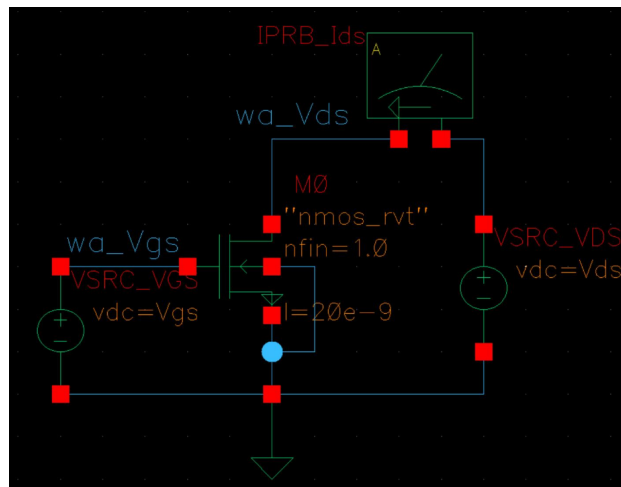


Figure 1: Circuit Setup for NMOS Characterization

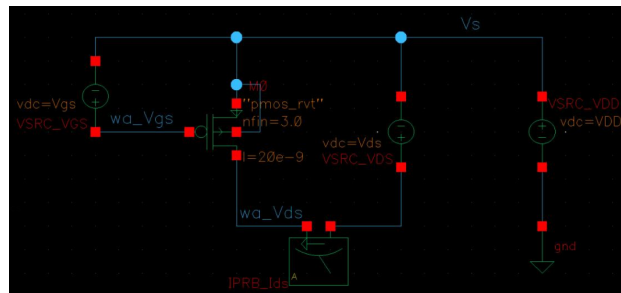
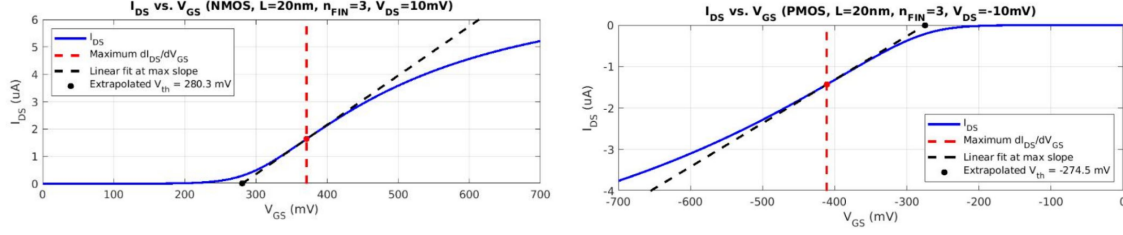


Figure 2: Circuit Setup for PMOS Characterization

The NMOS can be characterized with two sources, one to sweep V_{GS} and one to set V_{DS} . Fixing V_{DS} at a particular voltage and sweeping V_{GS} returns I_D . After the transistor is in the linear region, the current will be roughly linear with respect to V_{GS} and can be extrapolated back to $I_D = 0$ A to find the threshold. Plotting the I_D vs. V_{GS} curves at a low V_{DS} and extrapolating,



From the extrapolation, roughly $V_{TH} = 280 \text{ mV}$ for both the NMOS and PMOS.

b Velocity Saturation Model

Performing a curve fit to the linear I_{DS} vs. V_{GS} , we get

$$E_{c,n}L = 150 \text{ mV} \quad E_{c,p}L = 330 \text{ mV}$$

c Alpha-Power Model

We run the simulation with $V_{DS} = V_{DD}$. Performing a curve fit using the alpha power law model, MATLAB/Python yields the parameters

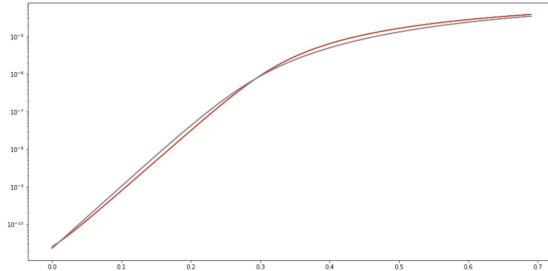
$$\begin{aligned} K_n &= 5.32 \times 10^{-4} & K_p &= 6.57 \times 10^{-4} \\ \alpha_n &= 1.4 & \alpha_p &= 1.8 \\ V_{TH,n} &= 0.284 \text{ V} & |V_{TH,p}| &= 0.297 \text{ V} \end{aligned}$$

d Linear Dependence Alpha-power Law

Setting $\alpha = 1$ and performing another line fit over the linear part of I_{DS} , the V_{TH} values that correspond to a linear dependence on V_{GS} yield representative values of

$$V_{TH,n} = 0.34 \text{ V} \quad |V_{TH,p}| = 0.37 \text{ V}$$

e Subthreshold Slope



The slope of the Subthreshold portion of the NMOS and PMOS devices is found by taking the log of the drain current and performing another linear fit on the subthreshold current. Above is a log plot demonstrating the subthreshold slope at several different values of V_{DS} .

$$S_n = 63 \text{ mV/dec} \quad S_p = 61 \text{ mV/dec}$$

2 Transistor Sizing

a Symmetrically Sized Inverter

The number of PMOS fins that minimizes the average delay for the inverter can be found by applying a square input to a chain of inverters and measuring the high-to-low and low-to-high delay. Doing so in ASAP7 yields that the minimum average delay is achieved by matching the number of PMOS and NMOS fins. This result is generally expected for a technology like ASAP7, which squares with some of the results from question 1. A representative minimum delay is about $t_p = 2$ ps.

b Intrinsic Delay

Recall that the delay of an inverter is expressed as

$$t_d = t_{unit}(\gamma + F)$$

where γ is the ratio of drain to gate capacitance and F is electrical effort. In the previous part, the inverter is loaded, which affects the delay. In this case, we want to also consider an unloaded inverter, since then the delay becomes $t_{unit} * \gamma$ (fully dependent on process parameters). By simulating the unloaded inverter and the loaded inverter in the previous part, we can determine both the intrinsic delay of about 950 fs and a gamma of about 0.97 (almost the nominal value of 1 typically given), by fitting a line to the two points and using the delay equation.

c Optimal Fanout

Recall from EECS151 or another course/textbook that the formula to find optimal fanout is

$$f_{opt} = e^{1 + \frac{\gamma}{f_{opt}}}$$

Using the value of γ we found in the previous part, solving this transcendental equation (with the help of a tool such as Wolfram Alpha) gives an optimal fanout of

$$f_{opt} = 3.56$$

This generally matches with the typical wisdom of fanout-of-4 for optimal fanout.

d Optimal NAND2

The model for I_{DSAT} is

$$I_{DSAT} = \frac{W}{L} \frac{\mu_{eff} C_{ox} E_C L}{2} \frac{(V_{GS} - V_{TH})^2}{(V_{GS} - V_{TH}) + E_C L}$$

i Hand Calculation

The equation above can be used to find the ratio of currents between the original single NMOS and the stacked NMOS devices in the NAND2. The sample values in the problem can be used, or your likely more accurate values from problem 1. Note that the $E_C L$ is now effectively doubled since there is a stack of two NMOS devices. Plugging in these values will yield that the number of NMOS fins should be increased by about 1.5x (quantized to an integer number of fins).

ii Using Measured Values

Using Spice, we can sweep the number of fins to find the optimized NAND2 delay and also measure the saturation currents directly. This will yield a similar result such that the number of fins should be increased by somewhere between 1x and 2x to minimize delay.

There are many possible reasons why the hand calculated values may not match the Spice values exactly. Some possible reasons may range from how you did your fitting/calculations in problem 1 to the saturation current equation oversimplifying and not accounting for the more complex switching dynamics and trajectories in the NAND2.

e Logical Effort

In the previous part, we essentially sized the devices so they would have about the same driving resistance as the minimum sized inverter. We can use this fact to calculate the logical effort directly as a ratio of the input capacitance of the NAND2 to the input capacitance of the inverter. This can be estimated by using the widths/fin multipliers which would give a result something like the following:

$$LE = (1.5 X_{fins} + 1 X_{fins}) / (1 X_{fins} + 1 X_{fins}) = 1.25$$

where X is the base number of fins (final number of fins should be quantized). The intrinsic delay can again be found by measuring the gate delay in Spice with no loading capacitance/gate.

f ASAP7 NAND2 Library

The data on delays and pin capacitance in the ASAP7 standard cell library can be used to calculate the logical effort and intrinsic delay compared to the previous calculations and Spice simulations.

g Optimal NAND3

The analysis for the NAND3 is essentially a repeat of the analysis for the NAND2, except we now have a stack of three NMOS transistors. The hand calculations and Spice simulations should now yield a fin multiplier of about 2x for optimal delay. This then yields a logical effort of around 1.5.

h Optimal NOR2

The previous analysis can again be mostly repeated for the NOR2, except now we have a stack of two PMOS devices in the gate. This yields a fin scaling similar to the NAND2 case of around 1.5x and then a logical effort of around 1.25.