

Homework 2 Solutions

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EE241B

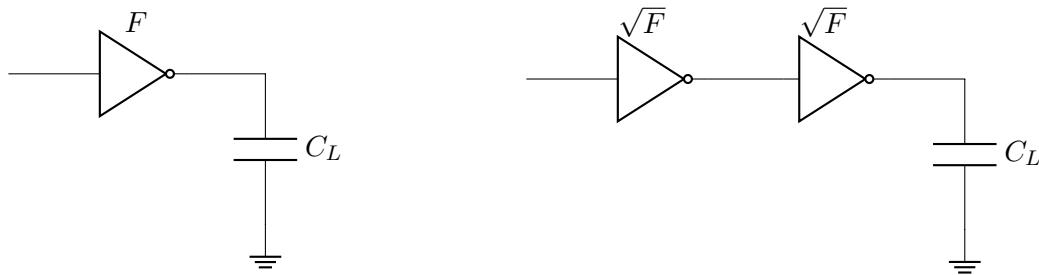
1 Lab 2

Everyone did well running through the DRC and LVS flow in Lab 2.

2 Delays

a Optimal Number of Inverters

Begin by considering the delays of both networks. For an optimally sized inverter chain starting at minimum size of depth N with fanout $F = \frac{C_L}{C_{in}}$, each stage must be sized to have an effective fanout of $\sqrt[N]{F}$, as illustrated in the figure below.



Writing out the delay equations for the two circuits,

$$t_{p1} = t_{unit}(1 + F)$$

$$t_{p2} = t_{unit}(2 + 2\sqrt{F})$$

In this technology, the input capacitance of a minimum sized inverter is $C_{in} = C_n + C_p = 1 \text{ fF} + 2 \text{ fF} = 3 \text{ fF}$. Solving the equations for when $t_{p1} = t_{p2}$, we find that,

$$(1 + F) = (2 + 2\sqrt{F})$$

$$\frac{(F - 1)}{2} = \sqrt{F}$$

$$(F - 1)^2 = 4F$$

$$F^2 - 6F + 1 = 0$$

$$F = 5.83 \rightarrow C_L = 17.48 \text{ fF}$$

So for load capacitances less than 17.48 fF, a single inverter is faster than a 2-stage inverter chain.

b Parasitics

To get the optimum value for C_2 , write out the delay equation and optimize for C_2

$$t_d = t_{unit}(2\gamma + f_1 + f_2) = t_{unit} \left(2\gamma + \frac{C_w + C_2}{C_1} + \frac{C_L}{C_2} \right)$$

$$\frac{\partial t_d}{\partial C_2} = t_{unit} \left(\frac{1}{C_1} - \frac{C_L}{C_2^2} \right) = 0$$

$$\frac{1}{C_1} = \frac{C_L}{C_2^2} \rightarrow C_2 = 6.364 \text{ fF}$$

If we compare this to the case without C_w ,

$$f = \sqrt{\frac{C_L}{C_1}} = \sqrt{\frac{13.5}{3}}$$

$$C_2 = C_L/f = 13.5 \text{ fF}/2.12 = 6.364 \text{ fF}$$

This is the same as with C_w ! This is actually intuitive, because the addition of C_w does not change the fact that each stage of the chain must have the same fanout, and we have fixed the value of C_1 . We can treat the introduction of C_w as a static delay added between Inv_1 and Inv_2 when sizing C_2 , so our answer does not change.

3 Latch Timing

a Minimum Clock Period

The limiting path in this design is from $R0 \rightarrow R3$, which sets the absolute minimum clock period to be

$$2T_{min} \geq t_{clk-q} + t_{S1} + t_{S2} + t_{S3} + 2t_{d-q} + t_{su}$$

$$2T_{min} \geq 2600 \text{ ps}$$

$$T_{min} \geq 1300 \text{ ps}$$

With this minimum period, we will have to relaunch from each register (no slack borrowing), so we are constrained by $R2 \rightarrow R3$,

$$T_{min} \geq t_{clk-q} + t_{S3} + t_{su}$$

$$T_{min} \geq 1500 \text{ ps}$$

The loop is another constraining path, which requires a minimum period of

$$T_{min} \geq t_{clk-q} + t_{S1} + t_{d-q} + t_{S2}$$

$$T_{min} \geq 1100 \text{ ps}$$

So the minimum clock period is

$$T_{min} = 1500 \text{ ps}$$

b Variability

The delay changes inversely proportional with current, so a decrease in current translates to an increase in delay. A 10% decrease in current will translate to a 10% increase in delay, so we can write

$$\frac{I_{on}}{I_{on,new}} = \frac{(1.1) * Delay}{Delay}$$
$$\frac{K(V_{DD} - V_{thz})}{K(V_{DD} - V_{thz,max})} = 1.1$$

$$V_{thz,max} = 0.318 \text{ V}$$

c Yield

In this case, we care about the margin in the design with regard to violating timing paths due to increased delay. With the parameters given, and the max threshold voltage calculated in part b, we can write the following expression to find the z-score and use the properties of a normal distribution to calculate a yield of 98.8%.

$$\frac{V_{thz,max} - \mu_{Vthz}}{\sigma_{Vthz}} = 2.27\sigma_{Vthz}$$