EE241 Advanced Digital Integrated Circuits **Spring 2020.**

HOMEWORK 1. **Due: Friday, February 14, 2020.**

This is an individual assignment!
The goal of this assignment is to get familiar with the class technology. It could be fairly long – knowledge of some scripting language (like Python) could be useful.

1. Models

Use the SPICE model to characterize the class 7nm ASAP CMOS process; parameter files correspond to devices nmos_rvt and pmos_rvt in the process directory (~ee241/spring20-labs/asap7PDK_r1p5/models/hspice/7nmTT.pm). The nominal supply voltage for this process is 0.7V.

a) Determine the threshold voltage V_{Th}, for the NMOS and PMOS devices (for $V_{BS} = 0$, $L = 20$nm and $W = 100$nm), by extrapolating from the I_D-V_{GS} curve at low V_{DS}. Explain your circuit setup. How does this result compare to values reported in the model file and the DC OP analysis?

b) For the model used in class $I_{DSat} = \frac{W}{L}\frac{\mu_{eff} C_{ox} E_C L}{2}\frac{(V_{GS} - V_{Th})^2}{(V_{GS} - V_{Th}) + E_C L}$, find the values of $E_C L$ that best fit the NMOS and PMOS characteristics. Use the V_{Th} value from part a). Note that you may want to modify the I_{Dsat} equation to account for finite output resistance.

c) We will try to extract the parameters V_{Th} and α for the alpha-power-law model $I_D = K(V_{GS} - V_{Th})^{\alpha}$ from SPICE simulations. Use Matlab to determine K, V_{Th} and α (hint: use the `lsqcurvefit` function). Determine the parameters for both NMOS and PMOS transistors.

d) By setting $\alpha = 1$, find the best V_{Th}'s that correspond to linear dependence of current on V_{GS}.

e) Find the subthreshold slope for both NMOS and PMOS devices.

2. Transistor sizing

In this problem, we will explore optimal transistor sizing.

a) Using SPICE and 7nm RVT model with 0.7V supply, find the required width of the PMOS transistor that minimizes the propagation delay $(t_{pHL} + t_{pLH})/2$ for the CMOS inverter. NMOS transistor width is fixed at 100nm. We will call this an optimally or symmetrically sized inverter.

b) Find the intrinsic delay of this inverter, p. It is set by the ratio of diffusion to gate capacitances, but it is better to find it from the delay measurements.

c) What is the optimal inverter fanout in this technology?

d) Optimally size the CMOS NAND2 gate. Find the required width (W) for the NMOS transistors in the pull-down such that the equivalent resistance of the pull-down network is the same as the equivalent resistance of the pull down transistor in an inverter from part a). Use hand analysis with parameters from Problem 1. (In case you haven't been able to solve Problem 1, you can use $E_CL = 0.7$V, $V_{DD} = 0.7$V, and $V_{Th} = 0.2$V). Compare with SPICE and discuss any discrepancies.

e) Find the logical effort and the intrinsic delay of the NAND2 gate from part c).

f) Now find a library cell for the NAND2 gate in the class standard cell library. Find the logical effort and the intrinsic delay form the datasheet or the .lib file.

g) Repeat part c) for a NAND3 gate. Compare with SPICE and discuss any discrepancies. Find the logical effort of this gate.

h) Optimally size NOR2 gate by using SPICE to match the inverter from part a). Find the logical effort.

3. Run a GCD module through a typical VLSI flow

a) Run through lab 1 on the course website/piazza/github. All questions that need to be answered in the lab are embedded in the lab document in bold with a "Q:" before it.