

HOMEWORK 3.

Due: Friday, March 20, 2020.

This is an individual assignment!**1. Lab 3**

- a. Complete Lab 3, answer the labeled questions, and submit them with this assignment.

2. Flip-Flop

A flip-flop is shown in Figure 2.

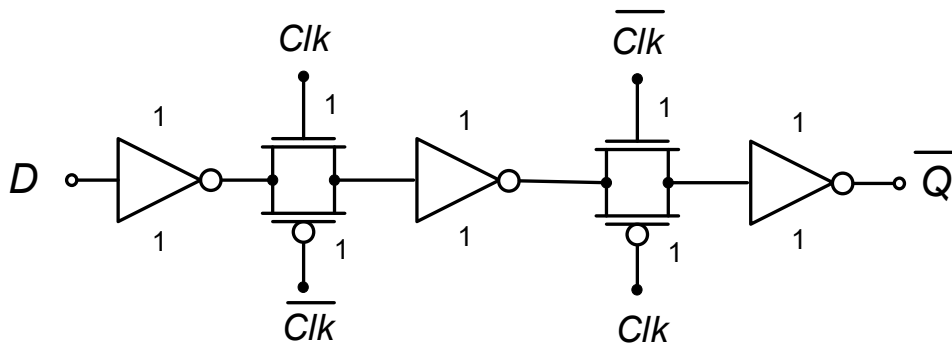


Figure 2.

In this process, a symmetrically-sized inverter has $W_p = W_n$, and a unit-sized transistor has gate and drain capacitances of 1fF and the on-resistance of $5k\Omega$. The resistance of a stack of two devices is 1.5x of the resistance of a single transistor with the same width. You can assume that the true and complementary clocks are ideal, and the logical effort of creating \overline{Clk} from Clk is 1.

- a) Is the flip-flop triggered by a rising or a falling edge of the Clk ?
- b) Calculate the $Clk - \overline{Q}$ delay for a $0 \rightarrow 1$ transition at the output and show your work.
- c) Calculate the hold time for $D = 1$.

3. SRAM

Consider a conventional 6-T SRAM cell, sized to be stable at nominal operating conditions. The cell is supposed to be operated within a conventional, precharged-to- V_{DD} bitline array. We would like to operate it at a reduced supply voltage so we are considering assist techniques. Let's analyze the effect of peripheral signals on the operation of the cell (briefly explain your answers).

- a) How does increased wordline voltage affect the read stability of the cell?
- b) How does increased wordline voltage affect the read access time of the cell?
- c) How does increased wordline voltage affect the writeability of the cell?

- d) How does shortened wordline pulse affect the read stability of the cell?
- e) How does shortened wordline pulse affect the writeability of the cell?
- f) How does increased cell supply voltage (without changing other signal levels) affect the writeability of the cell?