EE241B : Advanced Digital Circuits

Lecture 1 – Introduction

Borivoje Nikolić

Tuesdays and Thursdays 9:30-11am
293 Cory
Class Goals
and Expected Outcomes
Practical Information

• Instructor:
  • Borivoje Nikolić
    509 Cory Hall , 3-9297, bora@eecs
    Office hours: Tu 11am-12pm or by appointment

• GSI:
  • Daniel Grubb   dpgrubb@berkeley

Class Discussion
  http://piazza.com/berkeley/spring2020/ee241b
  Sign up for Piazza!
Class Web page
  inst.eecs.berkeley.edu/~ee241b
Class Topics

• This course aims to convey a knowledge of advanced concepts of digital circuit and system design in state-of-the-art technologies.
  • Emphasis is on the circuit and chip design and optimization for both energy efficiency and high performance for use in applications such as microprocessors, signal and multimedia processors, communications, memory and periphery. Special attention will be devoted to the most important challenges facing digital circuit designers today and in the coming decade, being the impact of slowdown in scaling, nanoscale effects, variability, power-limited design and timing.

• We will use qualitative analysis when practical
• Many case studies
EECS251A vs. EE241B

• EECS 251A:
  • Emphasis on digital logic design
  • (Very) basic transistor and circuit models
  • Basic circuit design styles
  • First experiences with design – creating a solution given a set of specifications
  • A complete pass through the design process

• EE 241B (likely 251B from next year):
  • Understanding of technology possibilities and limitations
  • Transistor models of varying accuracy
  • Design under constraints: power-constrained, flexible, robust,…
  • Learning more advanced techniques
  • Study the challenges facing design in the coming years
  • Creating new solutions to challenging design problems, design exploration
Special Focus in Spring 2020

- Current technology issues
- Process variations
- Robust design
- Memory
- Energy efficiency
- Power management
- SoC components
- (Circuits for machine learning)
• Module 1: Fundamentals – Current technologies (1.5 wks)
• Module 2: Models – From devices to gates, logic and standard cells (3 wks)
• Module 3: Design for performance (1.5 wks)
• Module 4: Memory, SRAM, variability, scaling options (2.5 wks)
• Module 5: Energy-efficient design (3 wks)
• Module 6: Clock and power distribution (1 week)
• Project presentations, final exam (1 week)
Class Organization

• 4 (+/-) assignments (20%)

• 4 quizzes (10%)

• 1 term-long design project (40%)
  • Phase 1: Topic selection (Feb 20, after ISSCC)
  • Phase 2: Study (report by March 19, before Spring break)
  • Phase 3: Design (report in RRR week)
  • Presentations, May 4, afternoon

• Final exam (30%) (Thursday, April 30, in-class)
Class Material

  • Available at www.springerlink.com

• Other reference books:
  • “VLSI Design Methodology Development” by, T. Dillinger, Pearson 2019.
  • “CMOS VLSI Design,” 4th ed, by N.Weste, D. Harris
Class Material

• List of background material available on website

• Selected papers will be made available on website
  • Linked from IEEE Xplore and other resources
  • Need to be on campus to access, or use library proxy, library VPN
    (check http://library.berkeley.edu)

• Class notes on website
  • No printed handouts in class!
Reading Assignments

• Three types of readings:
  • Assigned reading, that should be read before the class
  • Recommended reading that covers the key points covered in lecture in greater detail
  • Occasionally, background material will be listed as well
Reading Sources

- IEEE Journal of Solid-State Circuits (JSSC)
- IEEE International Solid-State Circuits Conference (ISSCC)
- Symposium on VLSI Circuits (VLSI)
- Other conferences and journals
Project Topics

• Focus this semester: Memories, Circuits for ML
• Design components that are very efficient in running matrix multiplications and convolutions.
  • Logic, in-memory computing
  • Build a complete system based on RISC-V Rocket
  • Negative results are ok
• Project teams: 2+ members, proportional to the size of the project
• More details in Week 2
Tools

• 7nm predictive model (ASAP7), with (mostly) complete design kit
• HSPICE
  • You need an instructional (or research) account
• Cadence, Synopsys, available on instructional servers
• Other predictive sub-100nm models
  • Such as SAED32
Webcast

• No recording! Focus on interactive lectures.
• Course notes available in advance.
• Be engaged in the discussions. You are part of the learning process.
Trends and Challenges in Digital Integrated Circuit Design
Reading (Lectures 1 & 2)

• Assigned
  • Rabaey, LPDE, Ch 1 (Introduction)
  • G.E. Moore, No exponential is forever: but "Forever" can be delayed! Proc. ISSCC’03, Feb 2003.
  • T.-C. Chen, Where CMOS is going: trendy hype vs. real technology. Proc. ISSCC’06, Feb 2006.

• Recommended
  • Chandrakasan, Bowhill, Fox, Chapter 1 – Impact of physical technology on architecture (J.H. Edmondson),
  • Chandrakasan, Bowhill, Fox, Chapter 2 – CMOS scaling and issues in sub-0.25μm systems (Y. Taur)

• Background: Rabaey et al, DIC Chapter 3.

• The contributions to this lecture by a number of people (J. Rabaey, S. Borkar, etc) are greatly appreciated.
Semiconductor Industry Revenues

Current State of Semiconductor Industry

Current GWP ~ 78,000 billion

Source: Statista
In 1965, Gordon Moore noted that the number of transistors on a chip doubled every 12 months. He made a prediction that semiconductor technology will double its effectiveness every 12 months.

“The complexity for minimum component costs has increased at a rate of roughly a factor of two per year. Certainly over the short term, this rate can be expected to continue, if not to increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain nearly constant for at least 10 years. That means by 1975, the number of components per integrated circuit for minimum cost will be 65,000.”

Gordon Moore, Cramming more Components onto Integrated Circuits, (1965).
“Reduced cost is one of the big attractions of integrated electronics, and the cost advantage continues to increase as the technology evolves toward the production of larger and larger circuit functions on a single semiconductor substrate.”
Electronics, Volume 38, Number 8, April 19, 1965

Source: Intel

Graph from S.Chou, ISSCC’2005
Moore’s Law - 2018

- Slowdown is apparent, but scaling continues
Moore’s Law and Cost

Transistor Price in US Dollars

- Ten
- One
- One Tenth
- One Hundredth
- One Thousandth
- One Ten Thousandth
- One Hundred Thousandth
- One Millionth
- One Ten Millionth
Progress in Nano-Technology

- Spintronic Storage
- Molecular Electronics
- Nanomechanics
- Silicon Nanowires
- Carbon Nanotubes

Millipede

Spintronic device

T.C. Chen, Where Si-CMOS is going: Trendy Hype vs. Real Technology, ISSCC’06
Plan A: Extending Si CMOS

Plan B: Subsysytem Integration

Plan C: Post Si CMOS Options

Plan Q: Quantum Computing

T.C. Chen, Where Si-CMOS is going: Trendy Hype vs. Real Technology, ISSCC’06
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<tbody>
<tr>
<td>Dram ½ pitch [nm]</td>
<td>90</td>
<td>65</td>
<td>45</td>
<td>32</td>
<td>22</td>
</tr>
<tr>
<td>MPU transistors/chip</td>
<td>550M</td>
<td>1100M</td>
<td>2200M</td>
<td>4400M</td>
<td>8800M</td>
</tr>
<tr>
<td>Wiring levels</td>
<td>10-14</td>
<td>11-15</td>
<td>12-16</td>
<td>12-16</td>
<td>14-18</td>
</tr>
<tr>
<td>High-perf. physical gate [nm]</td>
<td>37</td>
<td>25</td>
<td>18</td>
<td>13</td>
<td>9</td>
</tr>
<tr>
<td>High-perf. $V_{DD}$ [V]</td>
<td>1.2</td>
<td>1.1</td>
<td>1.0</td>
<td>0.9</td>
<td>0.8</td>
</tr>
<tr>
<td>Local clock [GHz]</td>
<td>4.2</td>
<td>9.3</td>
<td>15</td>
<td>23</td>
<td>40</td>
</tr>
<tr>
<td>High-perf. power [W]</td>
<td>160</td>
<td>190</td>
<td>220</td>
<td>250</td>
<td>288</td>
</tr>
<tr>
<td>Cost-perf. power [W]</td>
<td>84</td>
<td>104</td>
<td>120</td>
<td>138</td>
<td>158</td>
</tr>
<tr>
<td>Low-power $V_{DD}$ [V]</td>
<td>0.9</td>
<td>0.8</td>
<td>0.7</td>
<td>0.6</td>
<td>0.5</td>
</tr>
<tr>
<td>'Low-power’ power [W]</td>
<td>2.2</td>
<td>2.5</td>
<td>2.8</td>
<td>3.0</td>
<td>3.0</td>
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Roadmap Acceleration in the Past

(Including MPU/ASIC "Physical Gate Length" Proposal)

* Note: MPU ASIC Physical Bottom Gate Length Preliminary 2000 Update still under discussion.

1994
1997
1998/1999

Technology Node (DRAM Half Pitch)

MPU/ASIC Gate Length
Minimum Feature Size

MPU/ASIC Gate “Physical”

MPU/ASIC Gate “In Resist”

[9/15 - Litho Proposed “In Resist” (70% of “Best Case” Half Pitch)]

[9/15 - Litho Proposed “Physical” (1 year ahead of “In Resist”)]

2000 7/11 IRC Proposal
Best Case Opportunity Scenario [2.0]

Alternative Scenario [1.5]

Alternative Scenario [1.0]

~ 7X per technology node (.5x per 2 nodes)
Printed vs. Physical Gate

Nominal feature size

Gate Length

Physical gate length > nominal feature size after 22nm

Source: Intel, IEDM presentations
Transistors are Changing

- From bulk to finFET and FDSOI

65/55 nm 45/40 nm 32/28 nm 22/20 nm 16/14 nm 10 nm 7 nm 5 nm

Bulk

SiO₂/SiN Strain

FinFET

HK/MG Strain

FDSOI

Intel, IEDM'07

TSMC, Samsung

Intel, IEDM'09

ST, VLSI'12

Intel, VLSI'14

Intel, IEDM'12

Intel, IEDM'14

Intel, IEDM'17
Varying Flavors in Each Node

- 32nm (and 28nm): Various flavors - Intel

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<tr>
<th>Logic Transistor</th>
<th>Low Power Transistor</th>
<th>HVI/O Transistor</th>
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<tr>
<td>(HP or SP)</td>
<td>(LP)</td>
<td>(1.8 V or 3.3 V)</td>
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</tbody>
</table>

- **Logic Transistor**: Various flavors - Intel
- **Low Power Transistor**: Larger gate length
- **HVI/O Transistor**: High voltage input/output

Lg = 30/34nm  
Lg = 46nm  
Lg > 140nm

C.-H. Jan, IEDM’09, P. VanDerVoorn, VLSI Tech’10
Major Roadblocks

1. Managing complexity
   How to design a 10 billion (100 billion) transistor chip?
   And what to use all these transistors for?

2. Cost of integrated circuits is increasing
   It takes >>$10M to design a chip
   Mask costs are many $M in 16nm technology

3. Power as a limiting factor
   End of frequency scaling
   Dealing with power, leakages

4. Robustness issues
   Variations, SRAM, memory, soft errors, signal integrity

5. The interconnect problem
Power and Performance Trends

• What do we do next?
Cost Of Developing New Products

- These are non-recurring (NRE) costs, need to be amortized over the lifetime of a product
- We will attempt to dismantle this...
Next Lecture

• Impact of technology scaling (and its end)
• Characteristics of current technologies