Announcements

- Response to project abstracts today, by e-mail
- Team web pages
- Be careful not to leak proprietary info (interface tools via Hammer)

- Quiz 1 today

- Reading

- Chapter 11 (Partovi) in Chandrakasan, Fox, Bowhill

Outline

- Module 3
  - Flip-flop timing
  - Latch-based timing

Clock Uncertainties

Clock Generation

Power Supply

Interconnect

Capacitive Load

Temperature

Coupling to Adjacent Lines

Sources of clock uncertainty

Clock Constraints in Edge-Triggered Systems

Pictorial View of Setup and Hold Tests
Handling of Across-Chip Variation

- Each gate has a range of delay: \([lb, ub]\)
- The lower bound is used for early timing
- The upper bound is used for late timing
- This is called an early/late split
- Static timing obtains bounds on timing slacks
- Timing is performed as one forward pass and one backward pass

How is the Early/Late Split Computed?

- The best way is to take known effects into account during characterization of library cells
- History effect, simultaneous switching, pre-charging of internal nodes, etc.
- This drives separate characterization for early and late; this is the most accurate method
- Failing that, the most common method is derating factors
- Example: Late delay = library delay \(\times 1.03\)
  Early delay = library delay \(\times 0.95\)
- The IBM way of achieving derating is LCD factors (Linear Combination of Delay) (FC=fast chip, SC=slow chip, see next page)
- Late delay = \(\alpha_L \times FC\_delay + \beta_L \times NOM\_delay + \gamma_L \times SC\_delay\)
- Early delay = \(\alpha_E \times FC\_delay + \beta_E \times NOM\_delay + \gamma_E \times SC\_delay\)
- Across-chip variation is therefore assumed to be a fixed proportion of chip-to-chip variation for each cell type

IBM Delay Modeling*

At a given corner
late delay = intrinsic + systematic + random
early delay = intrinsic – systematic – random

The Problem with an Early/Late Split

- The early/late split is very useful
  - Allows bounds during delay modeling
  - Any unknown or hard-to-model effect can be swept under the rug of an early/late split
- But, it has problems
  - Additional pessimism (which may be desirable)
  - Unnecessary pessimism (which is never desirable)

How to Have Less Pessimism?

- Common path pessimism removal
- Account for correlations
- Credit for statistical averaging of random

Statistical Timing

- Deterministic
- Statistical

Statistical Max Operation

\[ A = a_0 + \sum_{i=1}^{n} a_i X_i + \sum_{i=1}^{m} a_i \Delta X_i \]

\[ \bar{A} = \bar{a}_0 + \sum_{i=1}^{n} \bar{a}_i X_i + \sum_{i=1}^{m} \bar{a}_i \Delta X_i \]

\[ \sigma_A = \sqrt{\left(\sum_{i=1}^{n} \sigma_{a_i}^2 \right) + \left(\sum_{i=1}^{m} \sigma_{\Delta a_i}^2 \right) + \left(\sum_{i=1}^{m} \sigma_{\Delta a_i}^2 \right)} \]


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*EECS241B L10 LATCH TIMING*
### Unified View of Correlations

\[ D = a_i + \sum a_i \Delta X_i + a_i \Delta X_d \]

- Independently random part
- Spatially correlated part: within-chip distance-related correlation
- Globally correlated part: chip-to-chip, wafer-to-wafer, batch-to-batch variation

### Spatial Correlation vs. Early/Late Split

- LF1, LF2, LF3:
  - Early clock
  - 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99

### Key Point

- Latch-based sequencing can improve performance, but is more complicated
- Timing analysis not limited to a consecutive pair of latches

### Latch Timing

- When data arrives to transparent latch:
  - Latch is a ‘soft’ barrier
- When data arrives to non-transparent latch:
  - Data has to be ‘re-launched’

### Preventing Late Arrivals

- Data can launch during transparency

### Preventing Premature Arrivals

- Data should not be able to race through during transparency
Two-Phase Latch-Based Design

- L1 latch is transparent when Clk = 1
- L2 latch is transparent when Clk = 0

* Two-phase non-overlapping is safer, but adds margin

Latch Design and Hold Times

- Slack passing – logical partition uses left over time (slack) from the previous partition
- Time borrowing – logical partition utilizes a portion of time allotted to the next partition
- Makes most impact in unbalanced pipelines

Bernstein et al, Chapter 8, Chandrakasan, Chap 11 (by Partovi)
Next Lecture

• Flip-flops