February 25, 2020, NY Times: Should robots have a face?

As automation comes to retail industries, companies are giving machines more humanlike features in order to make them liked, not feared.
Announcements

• Response to project abstracts sent
  • Please let me know if you didn’t receive it
  • Team web pages
    • Be careful not to leak proprietary info (interface tools via Hammer)

• Assignment 2 posted
Outline

• Module 3
  • Design of latches and flip-flops
3. Design for Performance

3. D Latch Design
MUX

• 2-input MUX
Transmission Gates

![Transmission Gate Diagram]

The diagram shows a transmission gate with inputs A and S, and output Y. The circuit is designed to pass the input signal A to the output Y when the control signal S is high, and block the signal when S is low.
Latch vs. Flip-Flop

(a) Latch

(b) Flip-flop
Latches

Transmission-Gate Latch

C²MOS Latch

Usually without contention
Latches

(a) The transparent high latch (THL)

(b) The transparent low latch (TLL)

(c) Timing waveforms for the THL.

Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)
Setup-Hold Time Illustrations

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Circuit before clock arrival (Setup-1 case)
Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)

Clk-Q Delay

Data

Clock

Time

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Setup-Hold Time Illustrations

Hold-1 case

Clock and Data signals with corresponding delay times.

- $D_{1}$
- $S_{M}$
- $Q_{M}$
- $CN$
- $CP$
- $Inv1$
- $Inv2$
- $T_{Hold-1}$
- $T_{Clk-Q}$
- $Time$
Setup-Hold Time Illustrations

Hold-1 case

Clock Data

T_{Hold-1}

t=0

T_{Hold-0}

Time

Clk-Q Delay

D

Inv1

D_1

CN

TG1

S_M

Inv2

Q_M

CP

0

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Setup-Hold Time Illustrations

Hold-1 case

Clk-Q Delay

Time

Q_M

Inv2

D_1

CP

S_M

CN

TG1

Inv1

D

Clock

Data

Time

t=0

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Setup-Hold Time Illustrations

Hold-1 case

Diagram showing the relationship between clock (Clk) and data (Q) with setup and hold times indicated.

Clock Data

Time

t=0

Clk-Q Delay

T_{Clk-Q}

T_{Hold-1}

Diagram elements include:
- Clk-Q Delay
- THold-1
- TClk-Q
- Setup-Hold Time Illustrations
Setup-Hold Time Illustrations

Hold-1 case

Data  Clock

\( T_{\text{Hold-1}} \)

\( t=0 \)

Setup-Hold Time Illustrations

Hold-1 case

Data  Clock

\( T_{\text{Hold-1}} \)

\( t=0 \)
More Precise Setup Time

\[ t_{D} \]

\[ t_{C} \]

\[ t_{Q} \]

\[ Clk \]

\[ D \]

\[ Q \]

\[ 1.05(t_{clk-q}) \]

\[ t_{Su} \]

\[ t_{H} \]

\[ T_{d-clk} \]
Generating Complementary Clocks
Latch $t_{D-Q}$ and $t_{Clk-Q}$
Key Point

• Two ways to design a flip-flop
  • Latch pair
  • Pulsed latch
3. Design for Performance

3.E Flip-Flop Design
Latch vs. Flip-Flop

(a) Latch

(b) Flip-flop

Flip-Flops

• Performance metrics

• Delay metrics
  • Insertion delay
  • Inherent race immunity
  • ‘Softness’ (Clock skew absorption)
  • Inclusion of logic
  • Small (+constant) clock load

• Power/Energy Metrics
  • Power/energy

• Design robustness
  • Noise immunity
Types of Flip-Flops

Latch Pair
(Master-Slave)

Pulse-Triggered Latch
Sources of Noise

1. Noise on input
2. Leakage
3. $\alpha$-Particle and cosmic rays
4. Unrelated signal coupling
5. Power supply ripple
Master-Slave Latch Pairs

- Example: PowerPC 603 (Gerosa, JSSC 12/94)
Flip-Flop Clk-Q, setup, hold
Pulse-Triggered Latches

• First stage is a pulse generator
  • generates a pulse (glitch) on a rising edge of the clock

• Second stage is a latch
  • captures the pulse generated in the first stage

• Pulse generation results in a negative setup time

• Frequently exhibit a soft edge property

• Note: power is always consumed in the pulse generator
  • Often shared by a group (register)
Pulsed Latch

Simple pulsed latch

Kozu, ISSCC’96
Pulsed Latches

Hybrid Latch Flip-Flop, AMD K-6
Partovi, ISSCC’96

[Diagram of a hybrid latch flip-flop]
HLFF Operation

1-0 and 0-1 transitions at the input with 0ps setup time

VDD=2.3v, 85°C, Typical Devices
C_{ch} = 60ff, C_{qb} = 300ff

T_{qu} = T_{dq} = 340ps
T_{hold} = 180ps
T_{su(min)} = -50ps
Hybrid Latch Flip-Flop

Skew absorption

Partovi et al, ISSCC'96
Pulsed Latches

Inputs are dynamically received
Clock edge is *hard*

To 3 other flip-flops

Pulsed Latches

Used in a synthesized flow

Partovi, VLSI’12
Pulsed Latches

7474, from mid-1960’s
Pulsed Latches

DEC Alpha 21264, StrongARM 110

First stage is a sense amplifier, precharged to high, when $Clk = 0$.
After rising edge of the clock sense amplifier generates the pulse on $S$ or $R$.
The pulse is captured in S-R latch.
Cross-coupled NAND has different propagation delays of rising and falling edges.
Sense Amplifier-Based Flip-Flop
Sampling Window Comparison

Naffziger, JSSC 11/02
Next Lecture

• Memory