February 25, 2020, NY Times: Should robots have a face?

As automation comes to retail industries, companies are giving machines more humanlike features in order to make them liked, not feared.

Announcements

• Response to project abstracts sent
• Please let me know if you didn’t receive it
• Team web pages
• Be careful not to leak proprietary info (interface tools via Hammer)
• Assignment 2 posted

Outline

• Module 3
  * Design of latches and flip-flops

3. Design for Performance

3.D Latch Design

Latches

Transmission-Gate Latch

CMOS Latch

Usually without contention
Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)

Data \[ T_{Setup-1} \] Clock

Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)

Data \[ T_{Setup-1} \] Clock

Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)

Data \[ T_{Setup-1} \] Clock

Setup-Hold Time Illustrations

Circuit before clock arrival (Hold-1 case)

Clock \[ T_{Hold-1} \] Data
Setup-Hold Time Illustrations

Hold-1 case

Setup-Hold Time Illustrations

Hold-1 case

Setup-Hold Time Illustrations

Hold-1 case

Setup-Hold Time Illustrations

Hold-1 case

Setup-Hold Time Illustrations

Hold-1 case

Setup-Hold Time Illustrations

Hold-1 case

Setup-Hold Time Illustrations

Hold-1 case

More Precise Setup Time

Generating Complementary Clocks

Latch $t_{D-Q}$ and $t_{CLK-Q}$

Key Point

- Two ways to design a flip-flop
  - Latch pair
  - Pulsed latch
3. Design for Performance
3.E Flip-Flop Design

Flip-Flops
- Performance metrics
- Delay metrics
  - Insertion delay
  - Inherent race immunity
  - ‘Softness’ (Clock skew absorption)
  - Inclusion of logic
  - Small (±constant) clock load
- Power/Energy Metrics
  - Power/energy
- Design robustness
- Noise immunity

Types of Flip-Flops
- Latch Pair (Master-Slave)
- Pulse-Triggered Latch

Sources of Noise
1. Noise on input
2. Leakage
3. α-Particle and cosmic rays
4. Unrelated signal coupling
5. Power supply ripple

Latch vs. Flip-Flop
(a) Latch
(b) Flip-flop

Scan Test

Latch Pair as a Flip-Flop

Master-Slave Latch Pairs
- Example: PowerPC 603 (Gerosa, JSSC 12/94)
Flip-Flop Clk-Q, setup, hold

Pulse-Triggered Latches
- First stage is a pulse generator
  - generates a pulse (glitch) on a rising edge of the clock
- Second stage is a latch
  - captures the pulse generated in the first stage
- Pulse generation results in a negative setup time
  - Frequently exhibit a soft edge property

* Note: power is always consumed in the pulse generator
  * Often shared by a group (register)

Pulsed Latch
Simple pulsed latch

Intel/HP Itanium 2

Pulsed Latches
Hybrid Latch Flip-Flop, AMD K-6
Partovi, ISSCC'96

Pulsed Latches
Hybrid Latch Flip-Flop, AMD K-7
Partovi et al, ISSCC'96

HLFF Operation
1-0 and 0-1 transitions at the input with 0ps setup time

Pulsed Latches
AMD K-7

Skew absorption

To 3 other flip-flops

Pulsed Latches

DEC Alpha 21264, StrongARM 110

First stage is a sense amplifier, precharged to high, when \( \text{Clk} = 0 \)
After rising edge of the clock sense amplifier generates the pulse on \( S \) or \( R \)
The pulse is captured in S-R latch
Cross-coupled NAND has different propagation delays of rising and falling edges

Sampling Window Comparison

Naffziger, JSSC 11/02

Next Lecture
• Memory