Announcements

• Assignment 2 due on Friday
• Quiz 2 on Tuesday, March 10
Outline

• Module 3
  • Design of flip-flops
  • SRAM basics
3. Design for Performance

3.D Latch Design
Lecture 11 Errata

• Latch $t_{D-Q}$ (with $C_L = C_{in}$)
  • $t_{D-Q} = 4.9 \, t_{unit} \sim 1 \, FO4$ (not $1.25 \, FO4$)
  • $t_{su} = 6.6 \, t_{unit} \sim 1.3 \, FO4$ (not $1.55 \, FO4$)
3. Design for Performance

3.E Flip-Flop Design
Key Point

• Two ways to design a flip-flop
  • Latch pair
  • Pulsed latch
Types of Flip-Flops

Latch Pair
(Master-Slave)

Pulse-Triggered Latch
Latch Pair as a Flip-Flop

CLK

D

P1

T1

SM

B1

IS

T2

SS

B2

Q

CLKB

P2

D

Q

CLK

$\text{Valid}$

$\text{t}_{\text{DV}}$

$\text{t}_{\text{CQ}}$

$\text{t}_{\text{SH}}$

$\text{t}_{\text{SU}}$

$\text{t}_{\text{DQ}}$
Sources of Noise

1. Noise on input
2. Leakage
3. α-Particle and cosmic rays
4. Unrelated signal coupling
5. Power supply ripple

Distant driver

VSS

D

T1

B1

QB

VDD

Master-Slave Latch Pairs

- Example: PowerPC 603 (Gerosa, JSSC 12/94)
Flip-Flop Clk-Q, setup, hold
Flip-Flop Timing Characterization

• Combinational logic delay is a function of output load and input slope

• Sequential timing (flip-flop):
  • $t_{\text{clk-q}}$ is function of output load and clock rise time
  • $t_{\text{Su}}$, $t_{\text{H}}$ are functions of D and Clk rise/fall times
Pulse-Triggered Latches

- First stage is a pulse generator
  - generates a pulse (glitch) on a rising edge of the clock

- Second stage is a latch
  - captures the pulse generated in the first stage

- Pulse generation results in a negative setup time

- Frequently exhibit a soft edge property

- **Note:** power is always consumed in the pulse generator
  - Often shared by a group (register)
Pulsed Latch

Simple pulsed latch

Kozu, ISSCC’96

(a) Sub-nano Pulse Generator
(b) Pulse Register

(a) Sub-nano Pulse Generator
(b) Pulse Register
Pulsed Latches

Hybrid Latch Flip-Flop, AMD K-6
Partovi, ISSCC’96
HLFF Operation

1-0 and 0-1 transitions at the input with 0ps setup time

VDD=2.3V, 85°C, Typical Devices
C\textsubscript{dh} = 60\text{ff}, C\textsubscript{QH} = 300\text{ff}

T\textsubscript{su} = T\textsubscript{du} = 340\text{ps}
T\textsubscript{hold} = 180\text{ps}
T\textsubscript{su(min)} = 90\text{ps}
Hybrid Latch Flip-Flop

Skew absorption

Partovi et al, ISSCC’96
Pulsed Latches

AMD K-7

Inputs are dynamically received
Clock edge is hard

To 3 other flip-flops

Pulsed Latches

Used in a synthesized flow

Partovi, VLSI’12
Pulsed Latches

7474, from mid-1960's
Pulsed Latches

First stage is a sense amplifier, precharged to high, when $Clk = 0$
After rising edge of the clock sense amplifier generates the pulse on $S$ or $R$
The pulse is captured in $S$-$R$ latch
Cross-coupled NAND has different propagation delays of rising and falling edges

DEC Alpha 21264, StrongARM 110
Sense Amplifier-Based Flip-Flop

![Diagram of Sense Amplifier-Based Flip-Flop](image)

3. Memory
Random Access Memory Architecture

• Conceptual: Linear array of addresses
  • Each box holds some data
  • Not practical to physically realize
    – millions of 32b/64b words

• Create a 2-D array
  • Decode Row and Column address to get data
Basic Memory Array (From 151/251A)

• Core
  • Wordlines to access rows
  • Bitlines to access columns
  • Data multiplexed onto columns

• Decoders
  • Addresses are binary
  • Row/column MUXes are ‘one-hot’ - only one is active at a time
SRAM Cell Trends

![Graph showing SRAM cell trends across technology nodes. The graph plots cell size [µm²] against technology node (nm). The diagram includes a curve for ITRS Cell, ITRS Eff. Cell, Individual Cell, Array Cell, and Eff. Cell.]
SRAM Scaling or Not?

- TSMC at IEDM’19
- Bora’s spreadsheet

- TSMC at ISSCC’20
SRAM Topics

A. Basics and trends
B. Static retention margin
C. Static read/write margins
D. Dynamic margins
D. Assist techniques
E. Periphery, redundancy and error correction
F. Scaling options
3. Memory
3.A SRAM Basics and Trends
6-T SRAM Cell

- Improve CD control by unidirectional poly
- Special SRAM design rules
• Key enabling technology:

• Impact:
SRAM Cell Trends (22nm)

A little analysis by using a ruler:
- Aspect ratio 2.9
- Height ~178nm, Width ~518nm
- Gate ~ 45nm (Lg is smaller)

0.092\(\mu\)m\(^2\) cell in 22nm from Intel (IDF’09)

0.346\(\mu\)m\(^2\) cell in 45nm from Intel (IEDM’07)
22nm SRAM – Discrete Widths

- FinFET cell design

HDC 0.092\,\text{um}^2

LVC 0.108\,\text{um}^2

E. Karl, ISSCC'12
14nm SRAM

- Aspect ratio $\sim 2.5$
- Cell area $= 0.05 \mu m^2$
  - Height $= 140nm$ (2 gate p)
  - Width $= 350nm$
  - $L_g \sim 32nm$

E. Karl, ISSCC’15
10nm SRAM

- HDC 1:1:1
- LVC 1:1:2

Guo, ISSCC’18
10nm SRAM + Ruler

288nm = 8 MxP

2CPP = 108nm

Lg ~ 20nm

HDC
0.0312 μm²

LVC
0.0367 μm²

340nm
Next Lecture

• SRAM read and write