EE241B : Advanced Digital Circuits

Lecture 21 – DVS II

Borivoje Nikolić

April 8, NY Times: Computers Already Learn From Us. But Can They Teach Themselves?

Scientists are exploring approaches that would help machines develop their own sort of common sense.

Features Pieter Abbeel and Sergey Levine from UC Berkeley
Announcements

• Assignment 4 due next Friday.

• Reading
Outline

• Module 5
  • Dynamic voltage and frequency scaling
5.F Dynamic Voltage Scaling
# Power/Energy Optimization Space

<table>
<thead>
<tr>
<th>Energy</th>
<th>Constant Throughput/Latency</th>
<th>Variable Throughput/Latency</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Design Time</td>
<td>Sleep Mode</td>
</tr>
<tr>
<td><strong>Active</strong></td>
<td>Logic design</td>
<td>Clock gating</td>
</tr>
<tr>
<td></td>
<td>Scaled $V_{DD}$</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Trans. sizing</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Multi-$V_{DD}$</td>
<td></td>
</tr>
<tr>
<td><strong>Leakage</strong></td>
<td>Stack effects</td>
<td>Sleep T’s</td>
</tr>
<tr>
<td></td>
<td>Trans sizing</td>
<td>Multi-$V_{DD}$ Variable $V_{Th}$</td>
</tr>
<tr>
<td></td>
<td>Scaling $V_{DD}$</td>
<td>+ Input control</td>
</tr>
<tr>
<td></td>
<td>+ Multi-$V_{Th}$</td>
<td></td>
</tr>
</tbody>
</table>

DFS, DVS

DVS

Variable $V_{Th}$
Adaptive Supply Voltages

Exploit Data Dependent Computation Times To Vary the Supply

from [Nielsen94]
(IEEE Transactions on VLSI Systems)
Processors for Portable Devices

- PERFORMANCE (MIPS)
- PROCESSOR ENERGY (Watt*sec)

- Dynamic Voltage Scaling

- PDAs
- Pocket-PCs
- Notebook Computers

- Eliminate performance ↔ energy trade-off

Burd
ISSCC’00
Typical MPEG IDCT Histogram
**Processor Usage Model**

**Desired Throughput**

- Compute-intensive and low-latency processes
- Background and high-latency processes

**System Optimizations:**
- Maximize Peak Throughput
- Minimize Average Energy/operation

*System Optimizations: Burd, ISSCC'00*
Compute ASAP:

Delivered Throughput

Always high throughput

Excess throughput

Clock Frequency Reduction:

Delivered Throughput

Energy/operation remains unchanged…

while throughput scaled down with $f_{CLK}$ Reduced

Common Design Approaches (Fixed VDD)
Scale $V_{DD}$ with Clock Frequency

- Constant supply voltage
  - $3.3V$
  - $1.1V$

Throughput ($\propto f_{CLK}$)

- ~10x Energy Reduction
  - Reduce $V_{DD}$, slow circuits down.

Burd
ISSCC'00
CMOS Circuits Track Over $V_{DD}$

- Normalized max. $f_{CLK}$

- Delay tracks within +/- 10%

- Inverter
- RingOsc
- RegFile
- SRAM

Burd
ISSCC’00
Dynamic Voltage Scaling (DVS)

• Dynamically scale energy/operation with throughput.
• Always minimize speed $\rightarrow$ minimize average energy/operation.
• Extend battery life up to 10x with the exact same hardware!

Burd
ISSCC’00
• DVS requires a voltage scheduler (VS).
• VS predicts workload to estimate CPU cycles.
• Applications supply completion deadlines.

\[
\frac{\text{CPU cycles}}{\Delta \text{time}} = F_{\text{DESIRED}}
\]
Converter Loop Sets $V_{DD}$, $f_{CLK}$

- Feedback loop sets $V_{DD}$ so that $F_{ERR} \rightarrow 0$.
- Ring oscillator delay-matched to CPU critical paths.
- Custom loop implementation $\rightarrow$ Can optimize $C_{DD}$.

Burd
ISSCC'00
Design Over Wide Range of Voltages

- Circuit design constraints. (Functional verification)
- Circuit delay variation. (Timing verification)
- Noise margin reduction. (Power grid, coupling)
- Delay sensitivity. (Local power distribution)

Design verification complexity similar to high-performance processor design @ fixed $V_{DD}$
Delay Variation & Circuit Constraints

- Cannot use NMOS pass gates – fails for $V_{DD} < 2V_T$.
- Functional verification only needed at one $V_{DD}$ value.

Normalized max. $f_{CLK}$

<table>
<thead>
<tr>
<th>Circuit</th>
<th>$V_T$</th>
<th>$2V_T$</th>
<th>$3V_T$</th>
<th>$4V_T$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter</td>
<td>1.0</td>
<td>0.5</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>RingOsc</td>
<td>0.5</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>RegFile</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>SRAM</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Burd
ISSCC'00
Delay relative to ring oscillator

Four extreme cases of critical paths:

All vary monotonically with $V_{DD}$.

- Timing verification only needed at min. & max. $V_{DD}$. 

Burd
ISSCC’00
Multiple Path Tracking

A. Drake, ISSCC'07
Multiple Path Tracking

Cho, ISSCC’16
Tracking with SRAM in Critical Path

» Mismatch between logic and SRAM

![Mismatch between logic and SRAM](image)

» SRAM multiplicative replica

![SRAM multiplicative replica](image)

Niki, JSSC’11
Design for Dynamically Varying VDD

- Static CMOS logic.
- Ring oscillator.
- Dynamic logic (& tri-state busses).
- Sense amp (& memory cell).

\[ \text{Max. allowed } |dV_{\text{DD}}/dt| \rightarrow \text{Min. } C_{\text{DD}} = 100\text{nF} \ (0.6\mu\text{m}) \]

Circuits continue to properly operate as V_{\text{DD}} changes
Static CMOS Logic

- Static CMOS robustly operates with varying V_{DD}.

\[ V_{in} = 0 \quad V_{out} = V_{DD} \]

\[
\begin{align*}
\text{max. } \tau &= 4\text{ns} \\
0.6\mu\text{m CMOS: } |dV_{DD}/dt| &< 200\text{V}/\mu\text{s}
\end{align*}
\]

- Static CMOS robustly operates with varying V_{DD}.
Ring Oscillator

Simulated with $dV_{DD}/dt = 20V/\mu s$

• Output $f_{CLK}$ instantaneously adapts to new $V_{DD}$. 
Dynamic Logic

\[ V_{DD} \]
\[ V_{out} \]
\[ V_{in} \]
\[ clk \]
\[ clk \]
\[ Volts \]
\[ Time \]
\[ V_{DD} \]
\[ V_{out} \]
\[ \Delta V_{DD} \]
\[ -\Delta V_{DD} \]

Errors

- False logic low: \( \Delta V_{DD} > V_{TP} \)
- Latch-up: \( \Delta V_{DD} > V_{be} \)

Errors

- Cannot gate clock in evaluation state.
- Tri-state busses fail similarly \( \rightarrow \) Use hold circuit.

0.6\( \mu \)m CMOS: \( |dV_{DD}/dt| < 20V/\mu s \)
Dynamic operation can increase energy efficiency > 10x.
V\textsubscript{DD}-Hopping

Application slicing and software feedback guarantee real-time operation.

Two hopping levels are sufficient.

Transition time between $f$ levels = 200µs

MPEG-4 encoding

Time

Normalized power

# of frequency levels

n-th slice finished here

Next milestone

#n

#n+1

EECS241B L21 DVS2
Done with switched-capacitor DC-DC converters which efficiently work only at discrete levels

Keller et al, ESSCIRC’16
Dithering Between Supply Levels

- Dithering fills in between fixed DC-DC modes

Keller et al, ESSCIRC’16
Next Lecture

- Low-power design
  - Clock gating
  - Power gating