EE241B : Advanced Digital Circuits

Lecture 21 – DVS II

Borivoje Nikolić

April 8, NY Times: Computers Already Learn From Us. But Can They Teach Themselves?

Scientists are exploring approaches that would help machines develop their own sort of common sense.

Features Pieter Abbeel and Sergey Levine from UC Berkeley.
Announcements

• Assignment 4 due next Friday.

• Reading
Outline

• Module 5
  • Dynamic voltage and frequency scaling
5.F Dynamic Voltage Scaling
<table>
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<th>Energy</th>
<th>Constant Throughput/Latency</th>
<th>Variable Throughput/Latency</th>
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<td>Sleep Mode</td>
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<td><strong>Active</strong></td>
<td>Logic design</td>
<td>Clock gating</td>
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<td>Scaled $V_{DD}$</td>
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<td>Multi-$V_{DD}$</td>
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<td>Scaling $V_{DD}$</td>
<td>+ Input control</td>
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<td>+ Multi-$V_{Th}$</td>
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Quiz

• [www.yellkey.com/wonder](http://www.yellkey.com/wonder)

Reducing supply by 1% around nominal levels:

• Lowers energy consumption by 1%
• Lowers energy consumption by 2%
• Lowers power by 2%
• Lowers performance by 1%
• Lowers performance by 2%
• Improves energy efficiency
• Lowers energy efficiency
Adaptive Supply Voltages

Exploit Data Dependent Computation Times To Vary the Supply

from [Nielsen94]

(IEEE Transactions on VLSI Systems)
Processors for Portable Devices

- Eliminate performance ↔ energy trade-off

Dynamic Voltage Scaling

Performance (MIPS)

Processor Energy (Watt*sec)

PDAs

Pocket-PCs

Notebook Computers

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Typical MPEG IDCT Histogram

![Graph showing typical MPEG IDCT histogram with frequency of occurrence on the y-axis and number of IDCTs per frame on the x-axis. There is a peak around 1500 IDCTs per frame.]
Processor Usage Model

**Desired Throughput**

- Compute-intensive and low-latency processes
- Maximum Processor Speed
- System Idle
- Background and high-latency processes

**System Optimizations:**
- Maximize Peak Throughput
- Minimize Average Energy/operation

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Common Design Approaches (Fixed VDD)

**Compute ASAP:**
- Excess throughput
- Always high throughput

**Clock Frequency Reduction:**
- Energy/operation remains unchanged...
- while throughput scaled down with $f_{CLK}$ Reduced

Delivered Throughput vs. Time
Scale $V_{DD}$ with Clock Frequency

Constant supply voltage

$\sim 10x$ Energy Reduction

Reduce $V_{DD}$, slow circuits down.

EECS241B L21 DVS2

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CMOS Circuits Track Over $V_{DD}$

Delay tracks within +/- 10%

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Dynamic Voltage Scaling (DVS)

1. Vary $f_{\text{CLK}}, V_{\text{DD}}$
2. Dynamically adapt

- Dynamically scale energy/operation with throughput.
- Always minimize speed $\rightarrow$ minimize average energy/operation.
- Extend battery life up to 10x with the exact same hardware!
DVS requires a *voltage scheduler* (VS).

VS predicts workload to estimate CPU cycles.

Applications supply completion deadlines.

\[
\frac{\text{CPU cycles}}{\Delta \text{time}} = F_{\text{DESIRED}}
\]
Converter Loop Sets $V_{DD}$, $f_{CLK}$

- Feedback loop sets $V_{DD}$ so that $F_{ERR} \rightarrow 0$.
- Ring oscillator delay-matched to CPU critical paths.
- Custom loop implementation $\rightarrow$ Can optimize $C_{DD}$. 

环节包括:
- Counter
- Latch
- Ring Oscillator (CPU replica)
- Digital Loop Filter
- Buck converter

Set by O.S.

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Design Over Wide Range of Voltages

- Circuit design constraints. (Functional verification)
- Circuit delay variation. (Timing verification)
- Noise margin reduction. (Power grid, coupling)
- Delay sensitivity. (Local power distribution)

Design verification complexity similar to high-performance processor design @ fixed $V_{DD}$
• Cannot use NMOS pass gates – fails for \( V_{DD} < 2V_T \).

• Functional verification only needed at one \( V_{DD} \) value.
Four extreme cases of critical paths:

All vary monotonically with $V_{DD}$.

• Timing verification only needed at min. & max. $V_{DD}$. 

Delay relative to ring oscillator
Multiple Path Tracking

A. Drake, ISSCC’07
Multiple Path Tracking

Cho, ISSCC’16
Tracking with SRAM in Critical Path

Mismatch between logic and SRAM

SRAM multiplicative replica

Niki, JSSC'11
Alternative: Error Detection

Bull, ISSCC'2010
Design for Dynamically Varying VDD

- Static CMOS logic.
- Ring oscillator.
- Dynamic logic (& tri-state busses).
- Sense amp (& memory cell).

Max. allowed $|dV_{DD}/dt| \rightarrow \text{Min. } C_{DD} = 100\text{nF (0.6}\mu\text{m)}$

Circuits continue to properly operate as $V_{DD}$ changes
Static CMOS Logic

- Static CMOS robustly operates with varying $V_{DD}$.

$$V_{in} = 0 \quad \Rightarrow \quad V_{out} = V_{DD}$$

$|dV_{DD}/dt| < 200V/\mu s$

- 0.6$\mu$m CMOS: $|dV_{DD}/dt| < 200V/\mu s$

$\tau_{max} = 4\text{ns}$
Ring Oscillator

Simulated with $dV_{DD}/dt = 20 V/\mu s$

• Output $f_{CLK}$ instantaneously adapts to new $V_{DD}$. 
Dynamic Logic

0.6μm CMOS: |dV_{DD}/dt| < 20V/μs

- Cannot gate clock in evaluation state.
- Tri-state busses fail similarly → Use hold circuit.

Errors
- False logic low: ΔV_{DD} > V_{TP}
- Latch-up: ΔV_{DD} > V_{be}

\[ \Delta V_{DD} \]
• Dynamic operation can increase energy efficiency > 10x.

85 MIPS @ 5.6 mW/MIPS (3.8V)

6 MIPS @ 0.54 mW/MIPS (1.2V)
Application slicing and software feedback guarantee real-time operation.

Two hopping levels are sufficient.
Dithering Between Supply Levels

- Done with switched-capacitor DC-DC converters which efficiently work only at discrete levels

Keller et al, ESSCIRC’16
Dithering Between Supply Levels

- Dithering fills in between fixed DC-DC modes

Keller et al, ESSCIRC’16
Next Lecture

- Low-power design
  - Clock gating
  - Power gating

\[ \text{Low power} \]

\[ \text{Supply + clk} \]

Thu 4/30

Projects May 4 or 5