February 2, 2020, EETimes: XMOS adapts Xcore into AIoT ‘crossover processor’

The new chip targets AI-powered voice interfaces in IoT devices — “the most important AI workload at the endpoint.”.
Announcements

• Homework 1 due on February 17

• No class on February 18 (ISSCC)

• Project abstracts due on February 20
  • Teams of 2
  • Title
  • One paragraph
  • 5 relevant references

• Can also combine with CS252 or EE290 projects
Outline

• Module 2
  • Technology variability
2. N Static Timing
Static Timing Analysis

• Computing critical (longest) and shortest path delay
  • Longest path algorithm on DAG [Kirkpatrick, IBM Jo. R&D, 1966]

• Used in most ASIC designs today

• Limitations
  • False paths
  • Simultaneous arrival times
    • Derate
Timing Constraints

\[ \text{RAT, early} \]

\[ \begin{align*}
\text{AT, early} & = T_{\text{skew}} - T_j - T_{\text{so}} \\
\text{AT, late} & = T_{\text{ck}} - T_{\text{skew}} + T_{\text{logic}, \text{max}} \\
\text{RAT, early} & = T_{\text{skew}} + T_h + T_j^* \\
\text{AT, early} & = T_{\text{ck}} - T_{\text{skew}} + T_{\text{logic}, \text{min}} \\
\text{Tj^*} & < T_j \\
\text{receive} & \quad \text{AT, late} < \text{RAT, late} \\
\text{AT, early} & > \text{RAT, early}
\end{align*} \]
False Paths

Inside Carry Bypass Adder - 1

Longest graphical/topological path runs along carry chain from stage to stage
Longest path analysis would identify red path as critical

\[ p_1 \cdot p_{i+1} = 1 \]
Static Timing - Summary

• Enables design of complex systems
• Simpler, less accurate models are used during design
• More accurate models are used for ‘signoff’
• See more in labs!
2.0 Design Variability Sources and Impact on Design
Variability Classification

• Nature of process variability
  • Within-die (WID), Die-to-die (D2D), Wafer-to-wafer (W2W), Lot-to-lot (L2L)
  • Systematic vs. random
  • Correlated vs. non-correlated

• Spatial variability/correlation
  • Device parameters (CD, $t_{ox}$, …)
  • Supply voltage, temperature

• Temporal variability/correlation
  • Within-node scaling, Electromigration, Hot-electron effect, NBTI, self-heating, temperature, SOI history effect, supply voltage, crosstalk
  [Bernstein, IBM J. R&D, July/Sept 2006]

• Known vs. unknown
  • Goal of model-to-hw correlation is to reduce the unknowns
Sources of Variability

• Technology
  • Front-end (Devices)
    • Systematic and random variations in $I_{on}$, $I_{off}$, $C$, ...
  • Back-end (Interconnect)
    • Systematic and random variations in $R$, $C$

• Environment
  • Supply (IR drop, noise)
  • Temperature
Spatial Variability

- Global
  - Fab to fab
  - Deployed environment
  - Lot to lot

- Local
  - Temperature
  - Metal polishing
  - Transistor $I_{on}$, $I_{off}$
  - Line-edge roughness
  - Dopant fluctuation
  - Film thickness

Across wafer
- Across reticle
- Across chip
- Across block

After Rohrer
ISSCC’06 tutorial

Spatial range [m]

- $10^6$ to $10^{-9}$
Temporal Variability

**Technology**
- Tech. node scaling
- Within-node scaling
- Electromigration
- NBTI
- Hot carrier effect
- Tooling changes
- Lot-to-lot

**Environment**
- Temperature
- Data stream
- SOI history effect
- Self heating
- Supply noise
- Coupling
- Charge

**Temporal range [s]**

- $10^{12}$
- $10^9$
- $10^6$
- $10^3$
- $10^0$
- $10^{-3}$
- $10^{-6}$
- $10^{-9}$
- $10^{-12}$

After Rohrer
ISSCC’06 tutorial
Systematic vs. Random Variations

• Systematic
  • A systematic pattern can be traced down to lot-to-lot, wafer-to-wafer, within reticle, within die, from layout to layout,…
  • Within-die: usually spatially correlated

• Random
  • Random mismatch (dopant fluctuations, line edge roughness,…)
  • Things that are systematic, but e.g. change with a very short time constant (for us to do anything about it). Or we don’t understand it well enough to model it as systematic. Or we don’t know it in advance (“How random is a coin toss?”).

• Unknown
## Systematic and Random Device Variations

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Random</th>
<th>Systematic</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel Dopant Concentration Nch</td>
<td>Affects $6_{VT}$[^1]</td>
<td>Non uniformity in the process of dopant implantation, dosage, diffusion</td>
</tr>
<tr>
<td>Gate Oxide Thickness Tox</td>
<td>Si/SiO$_2$ &amp; SiO$_2$/Poly-Si interface roughness[^2]</td>
<td>Non uniformity in the process of oxide growth</td>
</tr>
<tr>
<td>Threshold Voltage $V_T$ (non Nch related)</td>
<td>Random anneal temperature and strain effects</td>
<td>Non-uniform annealing temperature[^5] (metal coverage over gate) Biaxial strain</td>
</tr>
<tr>
<td>Mobility $\mu$</td>
<td>Random strain distributions</td>
<td>Systematic variation of strain in the Si due to STI, S/D area, contacts, gate density, etc</td>
</tr>
<tr>
<td>Gate Length L</td>
<td>Line edge roughness (LER)[^3]</td>
<td>Lithography and etching: Proximity effects, orientation[^4]</td>
</tr>
<tr>
<td>Fin geometry/ film thickness variations</td>
<td>Rounding, etc, $6_{VT}$, mobility.</td>
<td>Systematic fin thickness Systematic Si film/BOX variations</td>
</tr>
</tbody>
</table>

Dealing with Systematic Variations

- Model-to-hardware correlation classifies unknown sources

Systematic effect

- Improve process
  - Limited options
- Tighten a design rule
  - Density loss
- Model/Design-in
  - Extraction/Compact modeling/Design techniques
Systematic (?) Temporal Variability

Metal 3 resistance over 3 months
2.P Design Variability
Some Systematic Effects
Layout: Poly Proximity Effects

- Gate CD is a function of its neighborhood

Gate length depends on

- Light intensity profile falling on the resist
- Resist: application of developer fluid\(^1\), post exposure bake (PEB) temperature\(^2\)
- Dry etching: microscopic loading effects\(^3\)

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Layout: Proximity Test Structures

- **90nm experiments**

- **45nm experiments**

No single gates allowed

- **Ring oscillators and individual transistor leakage currents**

L.T. Pang, VLSI'06

L.T. Pang, CICC'08
Results: Single Gates in 90nm

- Max $\Delta F$ between layouts > 10%
- Within-die $3\sigma/\mu \sim 3.5\%$, weak dependency on density
Results: Single Gates in 45nm

- Weak effect on performance. $\Delta F \sim 2\%$
- Small shifts in NMOS leakage and bigger shifts in PMOS leakage
Impact of Stress

- 45nm STM process: Wafer rotated <100> - higher PMOS mobility
- NMOS strained through capping layer
- Subatmospheric STI – weak tensile stress
Impact of Longer Diffusion in 45nm

- Strongest effect measured in 45nm, $\Delta F \sim 5\%$
- No significant shift in $I_{\text{LEAK}}$

RO Frequency

NMOS $I_{\text{LEAK}}$

PMOS $I_{\text{LEAK}}$

- Faster chip
- Slowest chip
- 22 chips from 2 wafers

Longer diffusion
Impact of Shallow Trench Isolation (STI)

- $\Delta F \sim 3\%$, small changes in $I_{\text{LEAK}}$
- Due to STI-induced stress

\[ \text{Fastest chip} \quad \text{Slowest chip} \]
\[ 22 \text{ chips from 2 wafers} \]

\[ \begin{align*}
\text{RO Frequency} & \quad \text{NMOS } I_{\text{LEAK}} & \quad \text{PMOS } I_{\text{LEAK}} \\
\text{Norm. frequency} & \quad \text{Norm. NMOS log } I_{\text{LEAK}} & \quad \text{Norm. PMOS log } I_{\text{LEAK}}
\end{align*} \]
Impact of Correlations

\[ T = \sum \theta_{t_i} \]

\[ \mu_T = \sum \theta_{t_p} \]

\[ \frac{\mu_T}{\sigma_T} = \sqrt{\frac{1}{N}} \]

\[ \text{uncorr} \quad \frac{\sigma_T}{\theta_{t_p}} = \sqrt{\frac{n}{\sum \sigma^2_{t_p}}} \]

\[ \text{correlate} \quad \frac{\sigma_T}{\theta_{t_p}} = \sqrt{\frac{n}{\sum \sigma_{t_p}^2}} \]
Yield = Pr (sum of n delays < clock period)

\( \rho = 0 \) gives highest yield through averaging

Non-correlated gates in a path reduce impact of variation

Bowman et al, JSSC, Feb 2002.
Chip Yield Depends on Inter-Path Correlation

Yield = Pr (max delay of K paths < clock period)
K = 1 gives highest yield

Correlated paths reduce impact of variation

Bowman et al, JSSC, Feb 2002.
2. P Design Variability
Some Random Effects
Random Dopant Fluctuations

- Number of dopants is finite

Frank, IBM J R&D 2002
Random Dopant Fluctuations

$L_g = 17\text{nm}, V_{DS} = 0.7V$

$\sigma_{VT} = 23\text{mV}$

$L_g = 11\text{nm}, V_{DS} = 0.7V$

$\sigma_{VT} = 52\text{mV}$
Processing: Line-Edge Roughness

- Sources of line-edge roughness:
  - Fluctuations in the total dose due to quantization
  - Resist composition
  - Absorption positions

Effect:
- Variation (random) in leakage and power
Oxide Thickness

- Systematic variations +
- Roughness in the Si./SiO2 interface
- Smaller effect than RDF

Asenov, TED’2002
Transistor Matching

• $V_{Th}$ matching of geometrically identical transistors varies with size $\sim \sqrt{WL}$ and distance


Pelgrom parameter $A_{VT}$
- Scales with technology (EOT)

$A_{VT}$ in FDSOI technology