An increasing percentage of the world’s capacity is getting concentrated in the hands of the largest producers.
Announcements

• Project abstracts due today, by e-mail
  • Teams of 2
  • Title
  • One paragraph
  • 5 relevant references

• Can also combine with CS252 or EE290 projects

• Quiz 1 on Tuesday, Feb 25, in class

• Office hour moved to 11am on Monday
Outline

• ISSCC recap
• Module 2
  • Technology variability
• Module 3
  • Flip-flop timing
2. P Design Variability
Some Random Effects
Negative Bias Temperature Instability

- PFET $V_{th}$‘s shift in time, at high negative bias and elevated temperatures

- The mechanism is thought to be the breaking of hydrogen-silicon bonds at the Si/SiO2 interface, creating surface traps and injecting positive hydrogen-related species into the oxide.

- Also other charge trapping and hot-carrier defect generation

- Systematic + random shifts

Tsujikawa, IRPS’2003
Random Telegraph Signal (RTS)

- Trapping of a carrier in oxide traps modulates $V_{th}$ or $I_{ds}$
- $\tau_e$ and $\tau_c$ are random and follow exponential distributions

### RTS and Technology Scaling

- RTS exceeds RDF at 3 sigma with 20nm gates

\[
\Delta V_{th, \text{RTS}} \sim \frac{1}{WL}
\]

\[
\Delta V_{th, \text{RDF}} \sim \frac{1}{\sqrt{WL}}
\]

- Tega et al., VLSI Tech. 09

\[ L/W = 20/45 \text{nm} \]
3. Design for Performance

3.A Flip-Flop Timing
Flip-Flop Parameters

Delays can be different for rising and falling data transitions
Latch Parameters

Delays can be different for rising and falling data transitions

Unger and Tan
Trans. on Comp.
10/86
Clock Nonidealities

- Clock skew
  - Spatial variation in temporally equivalent clock edges; deterministic + random, $t_{SK}$

- Clock jitter
  - Temporal variations in consecutive edges of the clock signal; modulation + random noise
  - Cycle-to-cycle (short-term) - $t_{JS}$
  - Long-term - $t_{JL}$

- Variation of the pulse width
  - for level-sensitive clocking
Clock Skew and Jitter

- Both skew and jitter affect the effective cycle time
- Only skew affects the race margin, if jitter is from the source
  - Distribution-induced jitter affects both
Clock Uncertainties

Sources of clock uncertainty

1. Clock Generation
2. Power Supply
3. Interconnect
4. Devices
5. Temperature
6. Capacitive Load
7. Coupling to Adjacent Lines
Clock Constraints in Edge-Triggered Systems

\[ t_{CL} \leq (t_{CY} - t_{SK} - t_{JS}) - (t_{SU} + t_{CQ}) \]

\[ t_{CL} \geq t_{SK} + (t_{H} - t_{CQ}) \]
3.B Timing with Uncertainty/Variations
Pictorial View of Setup and Hold Tests

- Actual early AT
- Actual late AT
- Early RAT
- Late RAT
- Data must be stable
- Hold time
- Early slack
- Late slack
- Setup time
- Latest clock arrival time
- Earliest clock arrival time (next cycle)
- 0 or more switching(s) allowed
- Early RAT
- Late RAT
- Data must be stable
- Early slack
- Late slack
- Setup time
- Earliest clock arrival time (next cycle)

Data must be stable
Handling of Across-Chip Variation

• Each gate has a range of delay: \([lb, ub]\)
  • The lower bound is used for early timing
  • The upper bound is used for late timing
• This is called an early/late split
• Static timing obtains bounds on timing slacks
  • Timing is performed as one forward pass and one backward pass

Setup test

Hold test

Capture early path

Capture late path

Launching late path

Launching early path
How is the Early/Late Split Computed?

• The best way is to take known effects into account during characterization of library cells
  • History effect, simultaneous switching, pre-charging of internal nodes, etc.
  • This drives separate characterization for early and late; this is the most accurate method

• Failing that, the most common method is derating factors
  • Example: Late delay = library delay * 1.05
    Early delay = library delay * 0.95

• The IBM way of achieving derating is LCD factors (Linear Combination of Delay) (FC=fast chip, SC=slow chip, see next page)
  • Late delay = $\alpha_L \times FC_{\text{delay}} + \beta_L \times NOM_{\text{delay}} + \gamma_L \times SC_{\text{delay}}$
    Early delay = $\alpha_E \times FC_{\text{delay}} + \beta_E \times NOM_{\text{delay}} + \gamma_E \times SC_{\text{delay}}$
  • Across-chip variation is therefore assumed to be a fixed proportion of chip-to-chip variation for each cell type
IBM Delay Modeling*

At a given corner

late delay = intrinsic + systematic + random
early delay = intrinsic – systematic – random

*P. S. Zuchowski, ICCAD’04
Traditional Timing Corners

Intra-chip variation

Chip-to-chip variation

Intra-chip variation
The Problem with an Early/Late Split

- The early/late split is very useful
  - Allows bounds during delay modeling
  - Any unknown or hard-to-model effect can be swept under the rug of an early/late split
- But, it has problems
  - Additional pessimism (which may be desirable)
  - Unnecessary pessimism (which is never desirable)

![Diagram of setup test and capturing early/late paths]
How to Have Less Pessimism?

• Common path pessimism removal
• Account for correlations
• Credit for statistical averaging of random
Statistical Timing

- Deterministic

- Statistical
Statistical Max Operation

\[ A = a_0 + \sum_{i=1}^{n} a_i \Delta X_i + a_{n+1} \Delta R_a \]
\[ B = b_0 + \sum_{i=1}^{n} b_i \Delta X_i + b_{n+1} \Delta R_b \]
\[ \sigma_A = \sqrt{\sum_{i=1}^{n+1} a_i^2} \]
\[ \sigma_B = \sqrt{\sum_{i=1}^{n+1} b_i^2} \]
\[ \rho = \frac{\sum_{i=1}^{n} a_i b_i}{\sigma_A \sigma_B} \]
\[ \theta = \left( \sigma_A^2 + \sigma_B^2 - 2 \rho \sigma_A \sigma_B \right)^{1/2} \]
\[ t = \Phi \left( \frac{a_0 - b_0}{\theta} \right) \]
\[ E[\max(A, B)] = a_0 t + b_0 (1 - t) + \theta \phi \left( \frac{a_0 - b_0}{\theta} \right) \]
\[ E[\max(A, B)]^2 = (\sigma_A^2 + a_0^2) t + (\sigma_B^2 + b_0^2) (1 - t) + (a_0 + b_0) \theta \phi \left( \frac{a_0 - b_0}{\theta} \right) \]


**M. Cain, “The moment-generating function of the minimum of bivariate normal random variables,” American Statistician, May ’94, 48(2)
Unified View of Correlations

Independently random part

Spatially correlated part: within-chip distance-related correlation

Globally correlated part: chip-to-chip, wafer-to-wafer, batch-to-batch variation

\[ D = a_0 + \sum a_i \Delta X_i + a_r \Delta X_R \]
Spatial Correlation vs. Early/Late Split

Dependence on common virtual variables cancels out at the timing test

ICCAD '07 Tutorial
Chandu Visweswariah
Next Lecture

• Latch-based timing
• Flip-flops