EECS 244
Computer-Aided Design of Integrated Circuits and Systems

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Office Hours: Tu. Th. 3:30-4:30pm

Fall 1997

Administrative Details

❍ Prof. A. Richard Newton
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OH: Tu. Th. 3:30-4:30pm

❍ T.A.: Michael Shilman, michaels@eecs.berkeley.edu

❍ Lecture: Tu. Th. 2-3:30pm, 203 Mc Laughlin

❍ Grading:

Homeworks:	40%
Final Project:	60%

Goals of the Course

- ❍ Introduce fundamental concepts and algorithms used in the physical design of IC's & IC-based systems.
- ❍ Provide a broad and state-of-the-art context for electronic design automation.
- ❍ Identify promising new areas and problems for research, especially:
  - ▲ **Role of the Web and Java in EDA**
  - ▲ **Impact of Deep Sub-Micron (DSM) Technologies**
- ❍ Familiarize you with the Berkeley computing environment and some Berkeley CAD Tools and Systems
- ❍ Partial preparation for the CAD Preliminary Examination.

Design Technology

All software, hardware and infrastructural support aspects of the design of electronic systems

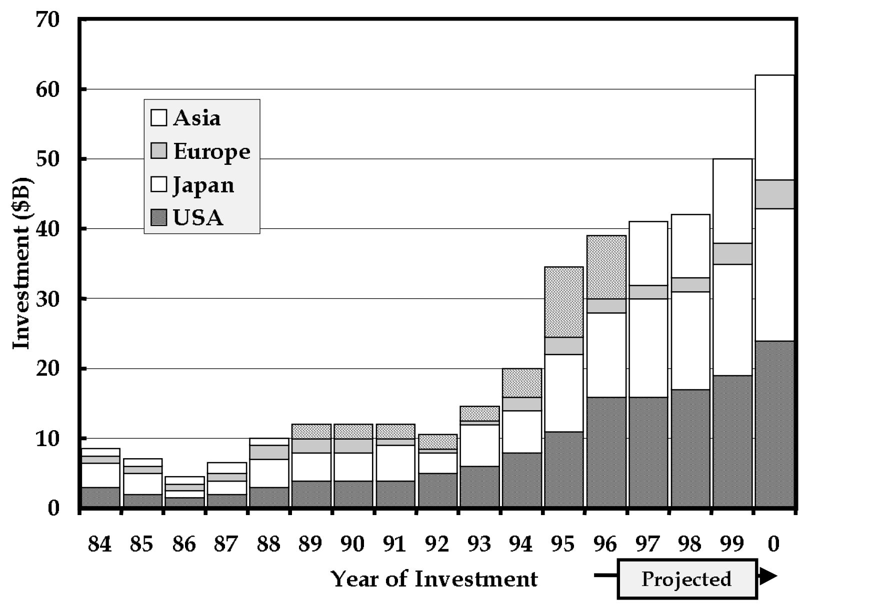
- ◆ CAD tools for verification and synthesis, from software and behavior to chip and board layout.
- ◆ All aspects of the integration and management of such tools with other tools and technologies.
- ◆ User interface technology.
- ◆ Special-purpose hardware emulators, accelerators and interfaces.
- ◆ Design decision support systems, including:
  - ▲ **ASIC gate, megacell and die libraries (simulation, layout, test, formal verification, etc.)**
  - ▲ **Estimators (area, cost, power, speed, etc.)**

Semiconductor Industry Growth

	1995	Steady State? 2030
Semiconductor as % of Electronics	17%	35%
Electronics as % of GWP	4%	8%
Semiconductors as % of GWP	0.7%	3%
CMOS Technology	0.35µm	0.05µm
World Semiconductor Sales	$140B	$12,000B
Annual Growth Rate	16%	8%, same as GWP

Source: Prof. Chenming Hu, UC Berkeley, 1996

Semiconductor Capital Investment



Source: Dataquest

SIA/SRC 1994 National Technology Roadmap

Year of First DRAM Shipment Minimum Feature (µm)	*1995 0.35*	*1998 0.25*	*2001 0.18*	*2004 0.13*	*2007 0.10*	*2010 0.07*	*Driver*
Memory							D
Bits/Chip (DRAM/Flash)	64M	256M	1G	4G	[illegible]	64G	
Cost/Bit @volume (millicents)	0.017	0.007	[illegible]	[illegible]	[illegible]	0.0002	
Logic (High Volume: Microprocessor)							L (µP)
Logic Transistors/cm² (packed)	4M	7M	13M	25M	50M	90M	
Bits/cm² (cache SRAM)	2M	6M	[illegible]	50M	[illegible]	300M	
Cost/Transistor @volume (millicents)	1	0.5	[illegible]	[illegible]	0.05	[illegible]	
Logic (Low Volume: ASIC)							L (A)
Transistors/cm² (auto layout)	2M	4M	7M	12M	25M	40M	
Non-recurring engineering cost/transistor (millicents)	0.3	0.1	0.05	0.03	0.02	0.01	
Number of Chip I/Os							
Chip to package (pads) high perf.	900	1350	2000	2600	3600	4800	L, A
Chip Frequency (MHz)							
On-chip clock, cost-performance	150	200	[illegible]	400	500	625	µP
On-chip clock, high performance	300	450	600	800	[illegible]	1100	
Chip-to-board speed, high performance	150	200	[illegible]	[illegible]	[illegible]	475	L
Chip Size (mm²)							
DRAM	190	280	[illegible]	640	960	1400	D
Microprocessor	250	300	[illegible]	430	[illegible]	620	µP
ASIC	450	660	[illegible]	900	1100	1400	A
Maximum Number Wiring Levels (logic)							
On-chip	4–5	5	5–6	6	6–7	7–8	µP

>0.5G logic gates
>2G bits SRAM

Today's Design Methodologies Will Not Scale Much Further

◆ The Deep Sub-Micron (DSM) Effect ($\leq 0.25\mu$)

$\propto$ DSM

"Microscopic Problems"
- **Wiring Load Management**
- **Noise, Crosstalk**
- **Reliability, Manufacturability**
- **Complexity: LRC, ERC**
- **Accurate Power Prediction**
- **Accurate Delay Prediction**
- **etc.**

Everything Looks a Little Different

?

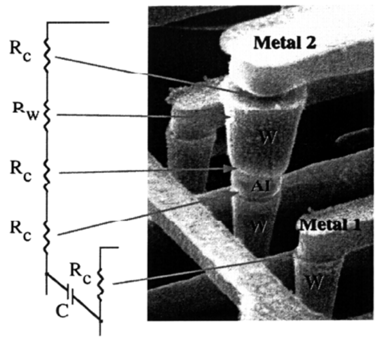
$\propto$ 1/DSM

"Macroscopic Issues"
- **Time-to-Market**
- **Millions of Gates**
- **High-Level Abstractions**
- **Reuse & IP: Portability**
- **Predictability**
- **etc.**

...and There's a Lot of Them!

Adapted from Dr. Kurt Keutzer, Synopsys

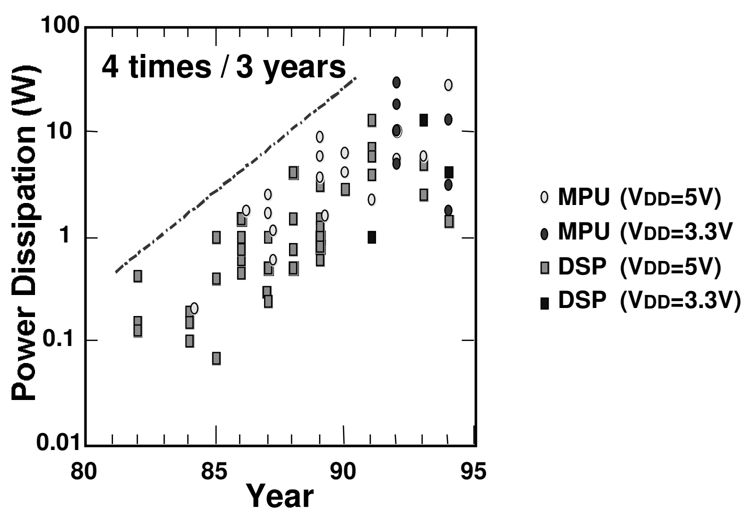
Chip Interconnect Systems



Year	Min. Feature Size [µm]	Interconnect Density [m/cm ^{2}/level]	Interconnect Length [m]
1995	0.40	35	380
1998	0.30	50	840
2001	0.22	70	2100
2004	0.15	105	4100
2007	0.11	125	6300
2010	0.08	155	10,000

Source: Sematech **Source: W. Maly, CMU**

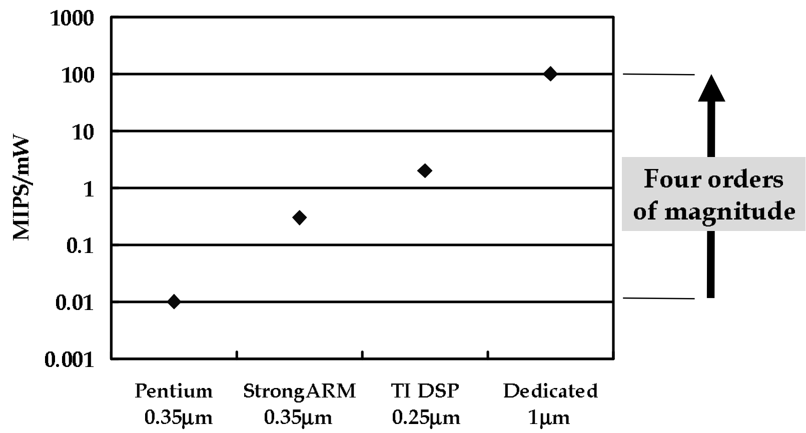
- **Interconnect will eventually dominate all approaches to the design process and will limit the overall effectiveness of any approach.**



Sakurai & Kuroda, Sashimi '96

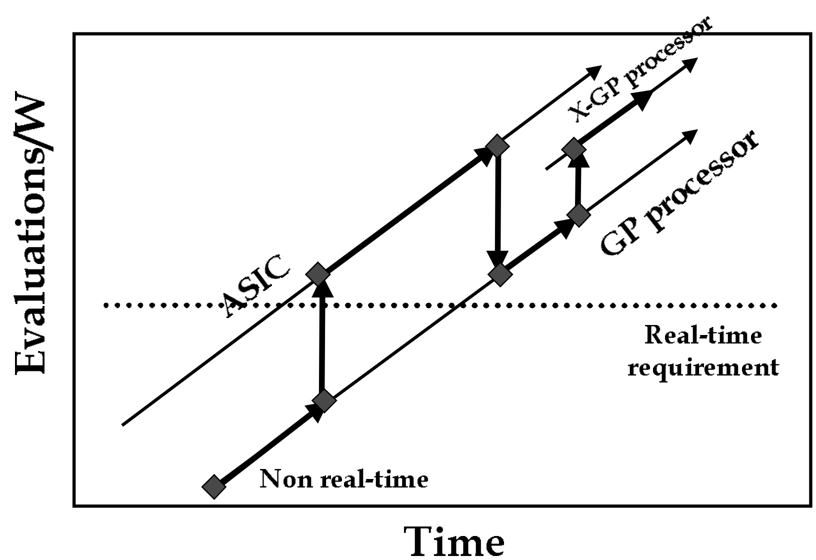
Power as the Driver

We believe power always has been the driver!



Source: R. Brodersen, Berkeley

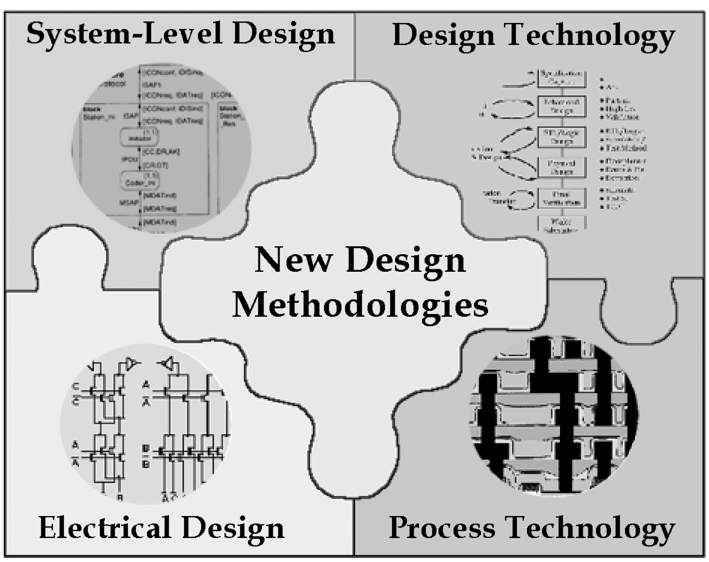
Particular Function (e.g. MPEG)



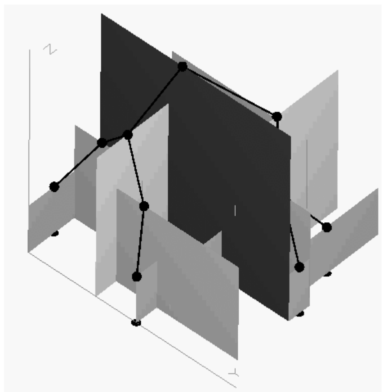
Some Implications

- *"The Full-Chip Bus is Dead!"*
  - Synchronous and asynchronous?
  - Has global architectural implications
- *"Route-then-Place":* Use more transistors, gates, etc. if it helps manage the routing
  - Automatically compiled complex blocks (e.g. memory, datapath, etc.) *"Return of the Silicon Compiler"*
- Complex Synthesized Structures (CSS)
  - More complex basic cells?
  - On-the-fly library generation?
  - Sense-amp latches? Transparent latches?
  - Retiming, retiming, retiming,…?

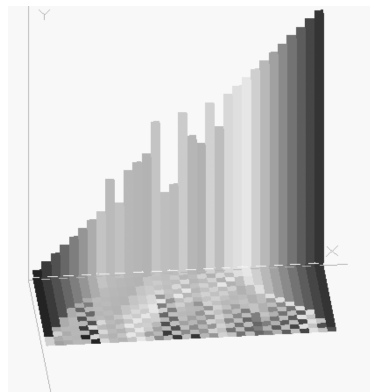
Advanced CMOS Design Methodology



Representation as an Aid in Decision Support



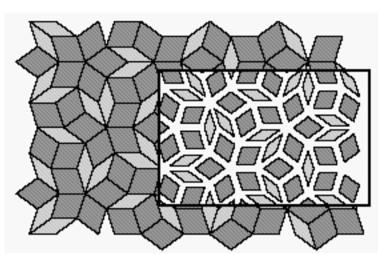
k-D Tree



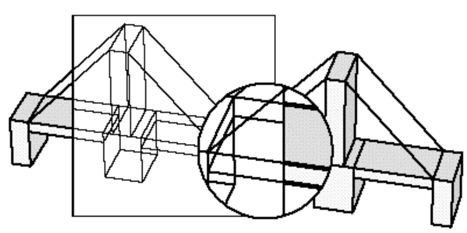
ShakeSort

Beyond Hierarchy

- e.g. Level-of-Detail (VRML 2), Magic Lens (Xerox)



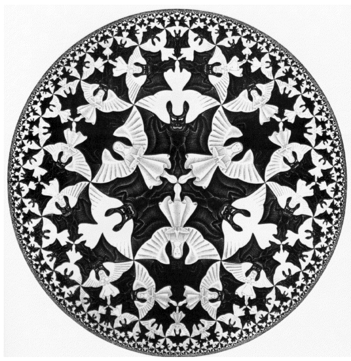
Transformation Lens



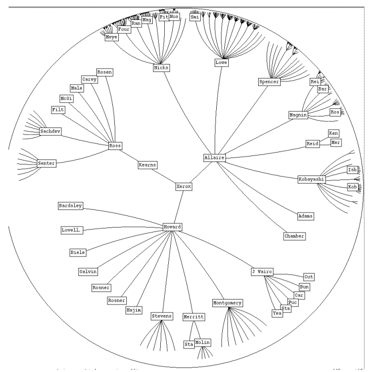
See-through lens, magnifier

Abstractions for Collaboration

- **e.g. "Fisheye Lens" (Hyperbolic Browser; DEC, Xerox)**



Escher



File System

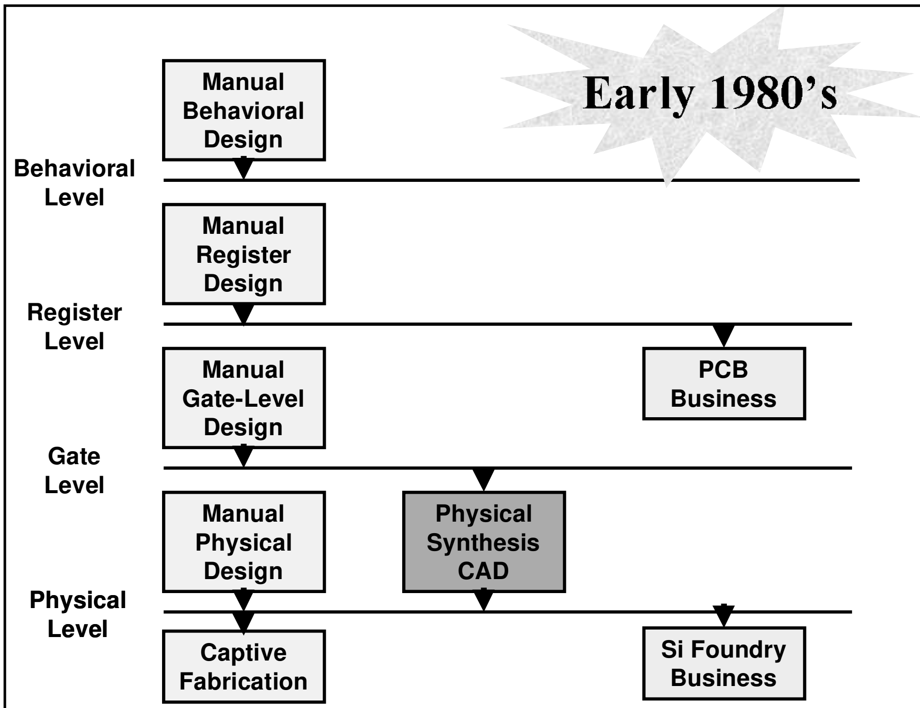
Simplified Model of Design

Behavior
Functions the system must implement
Time, area, power, etc. constraints
Implementation-independent description

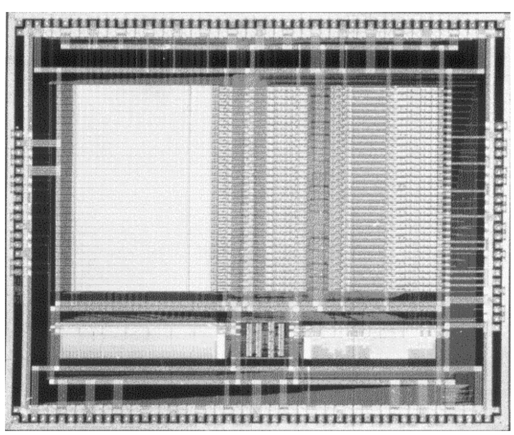
Register
Components and their interconnections
Std. components & ROM, ASIC, PLD
Timing constraints for components

Gate
Low-level components & nets
In terms of ASIC library
EDIF well-suited to this description

Mask
Physical layout of IC or board
EDIF well-suited to this description

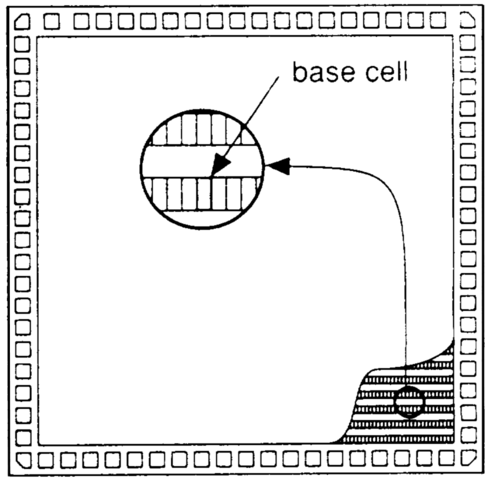


Structured Custom Chip Layout



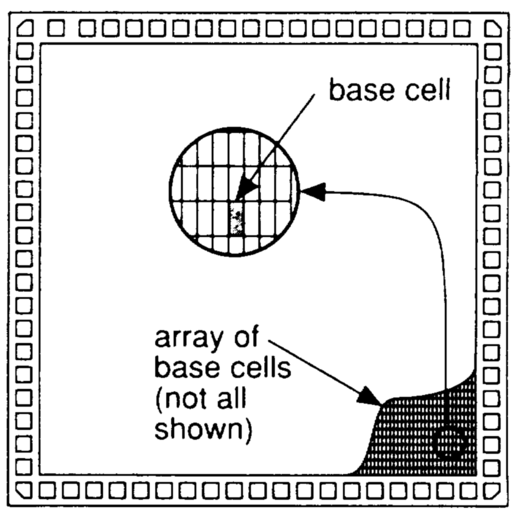
Cell-Based Design Styles

Channeled Gate Array



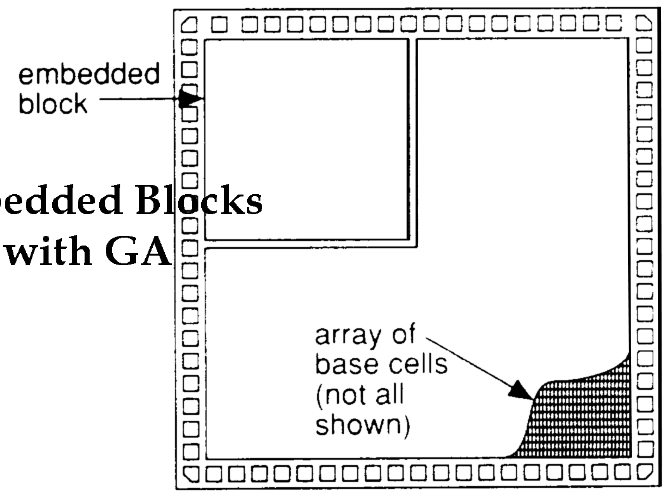
Cell-Based Design Styles

Sea-of-Gates GA



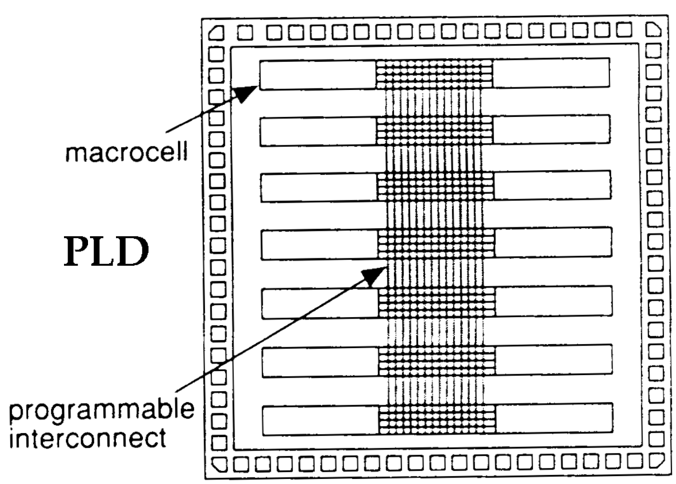
Cell-Based Design Styles

Embedded Blocks with GA



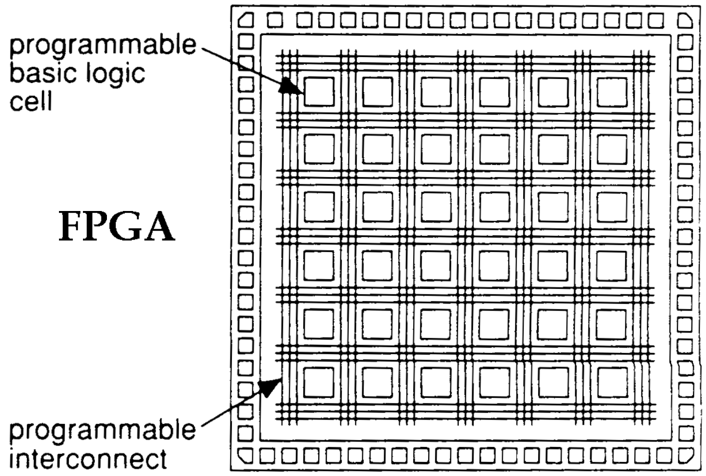
Cell-Based Design Styles

PLD

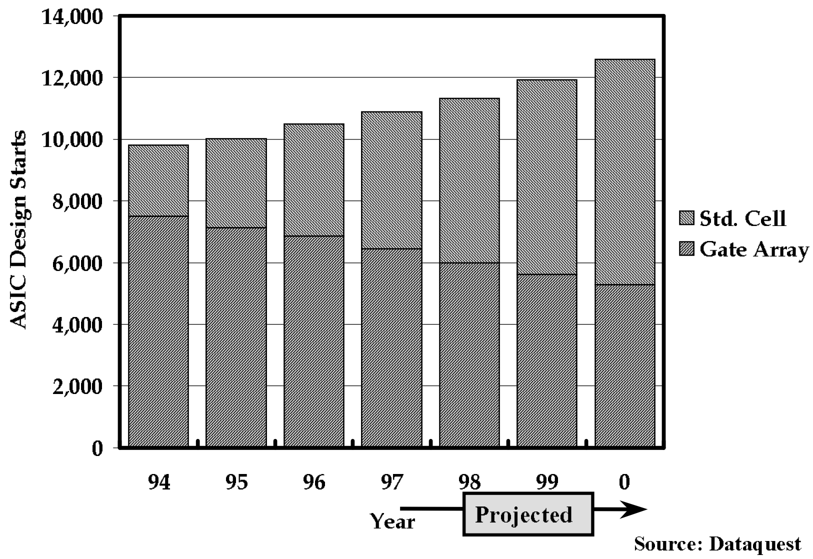


Cell-Based Design Styles

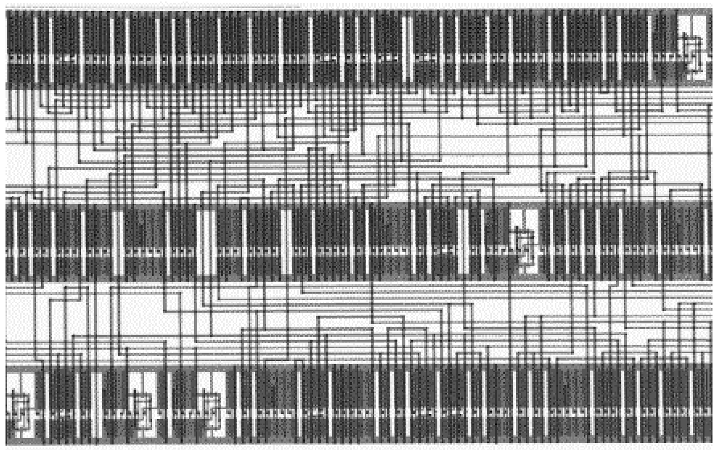
FPGA



ASIC Design Starts



Standard Cell Layout



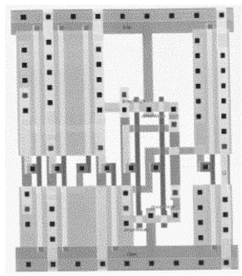
Standard Cells vs. Gate Array

(a) Two tracks required and all connections routed.

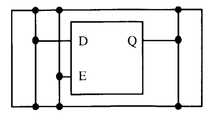
(b) Shorter wire length but three tracks required.

In a Standard Cell design, an additional track could be added while in a Gate-Array, the designer is faced with extra wire length or no connection.

Layout Abstractions for Cell-Based Design

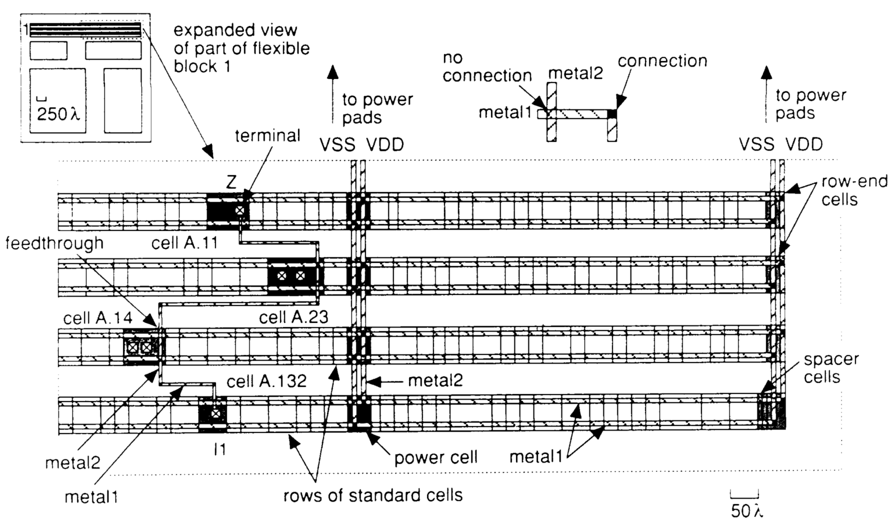


Mask-Level Layout



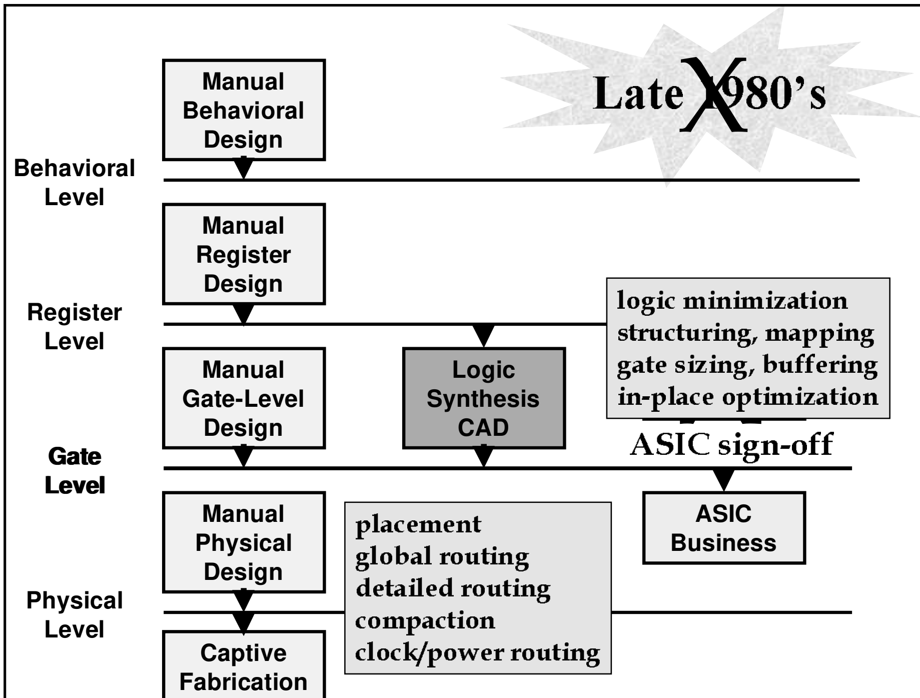
Cell Abstraction for Automatic Placement

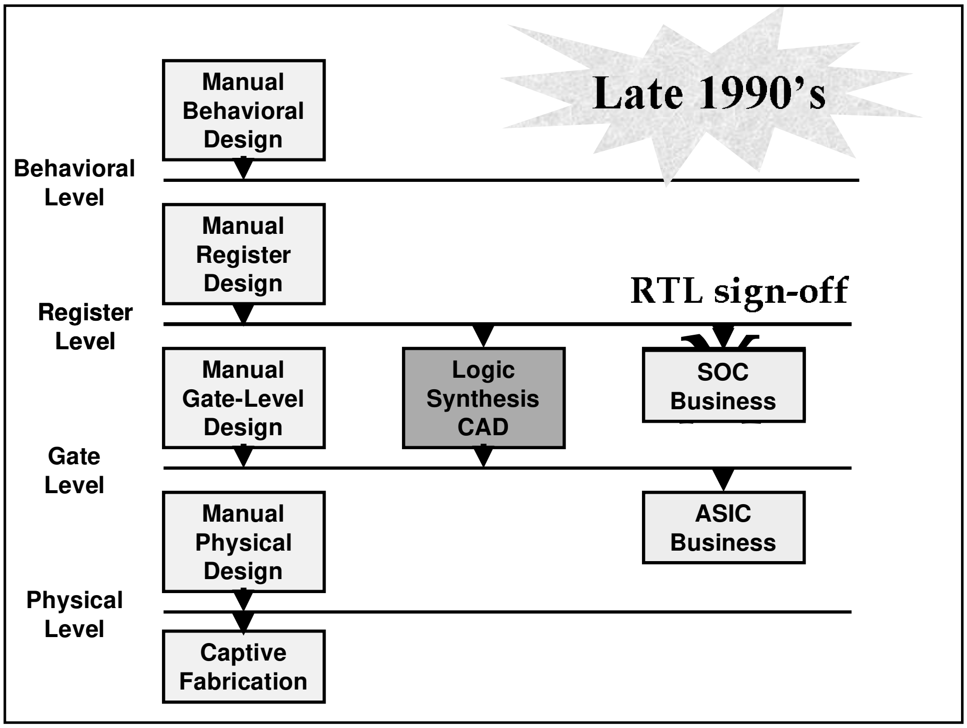
Channeled Gate Array

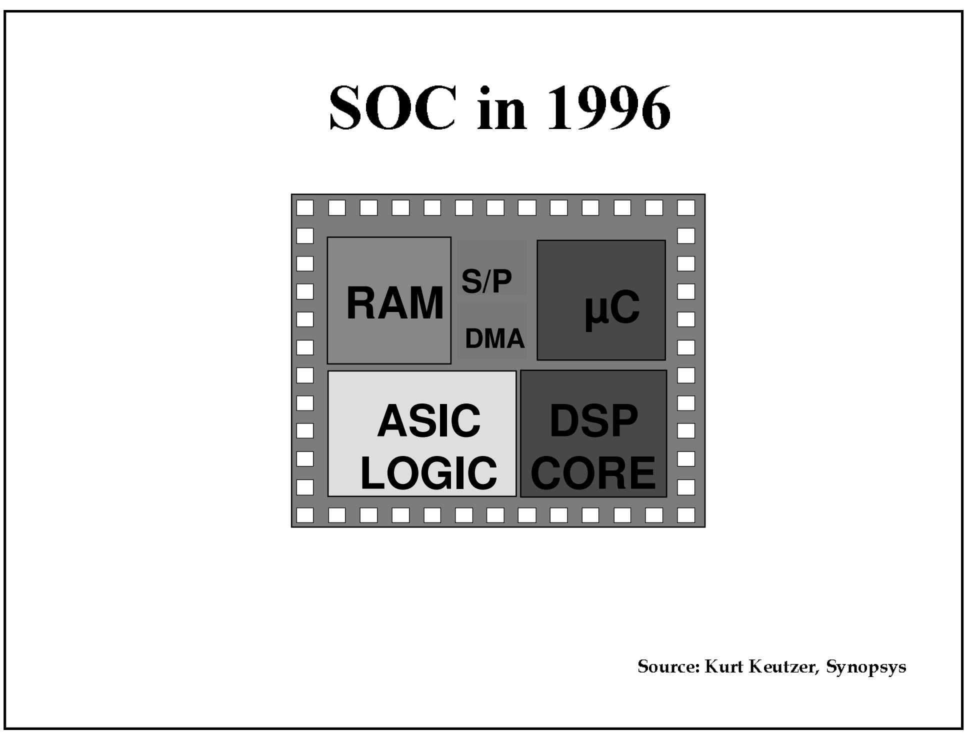


Placement & Routing

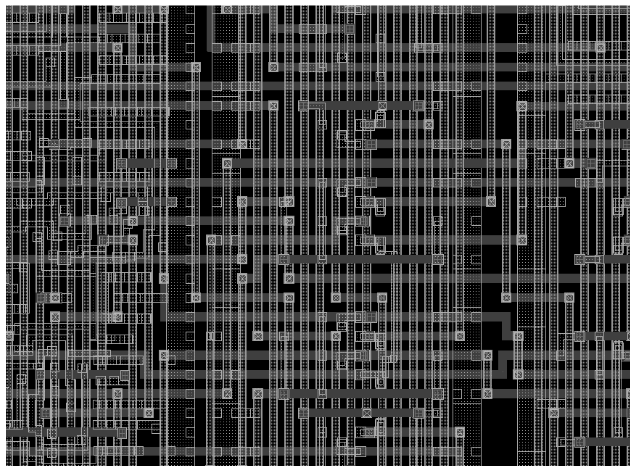
- Placement
  - Initial Placement
    - **Random**
    - **Constructive (top-down)**
    - **Direct (bottom-up)**
  - Placement Improvement
    - ***n*-wise interchange**
  - Gate-assignment (if multiple gates/package)
- Routing
  - Global Routing (e.g. channel assignment)
  - Pin Assignment (assignment of nets to pins)
  - Detailed Routing
  - "Clean-up" (e.g. via-pushing)




Late 1990's
Manual Behavioral Design
Behavioral Level
Manual Register Design
RTL sign-off
Register Level
Manual Gate-Level Design
Logic Synthesis CAD
SOC Business
Gate Level
Manual Physical Design
ASIC Business
Physical Level
Captive Fabrication

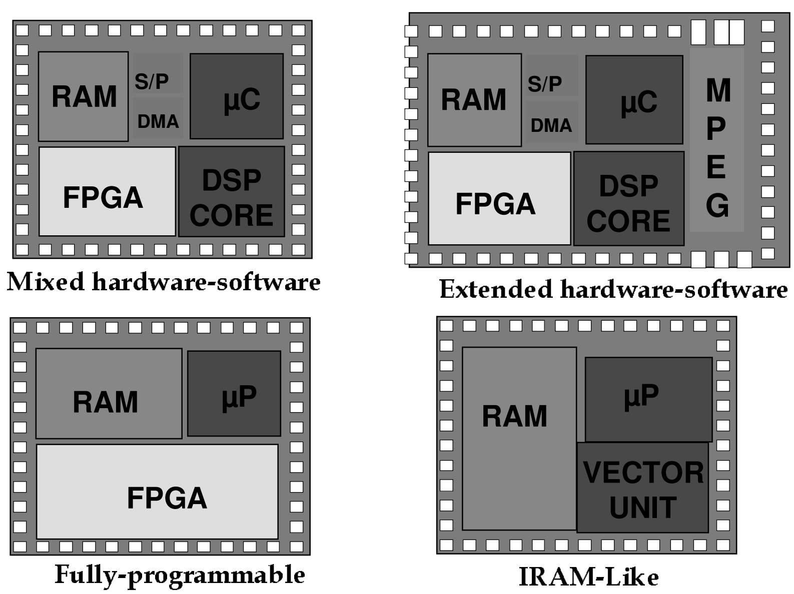

SOC in 1996
RAM
S/P
DMA
µC
ASIC LOGIC
DSP CORE
Source: Kurt Keutzer, Synopsys

Capacitance of Crossing Lines



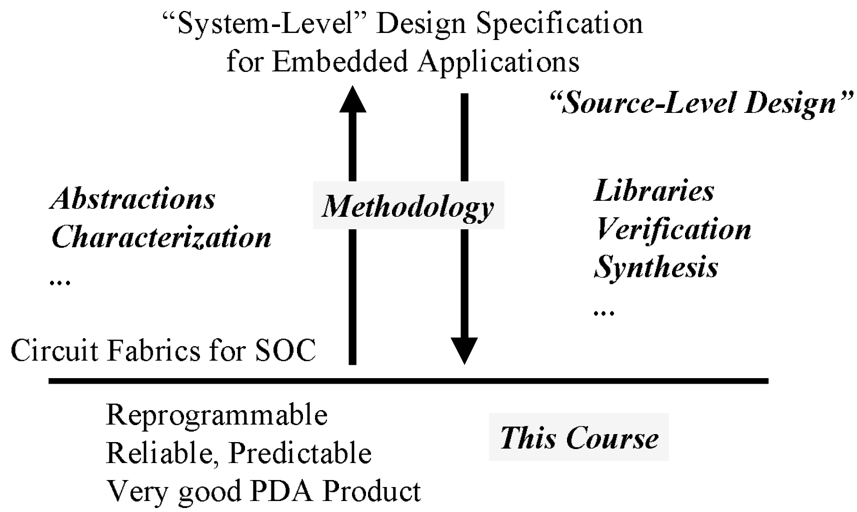
- **70% of interconnections in a DSM chip are parallel crossing lines with 3D effects**

Other Near-Term Micro-Architectures



Source: Kurt Keutzer, Synopsys

SOC Challenge



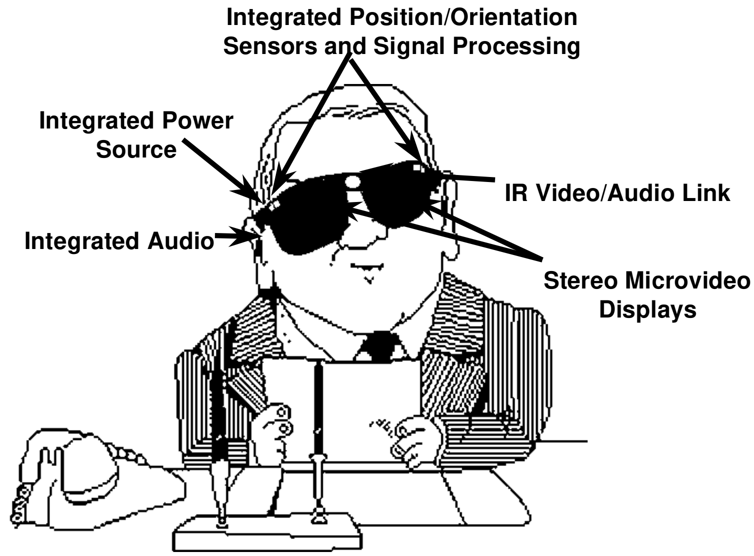
Single-Chip Silicon Implementation Styles

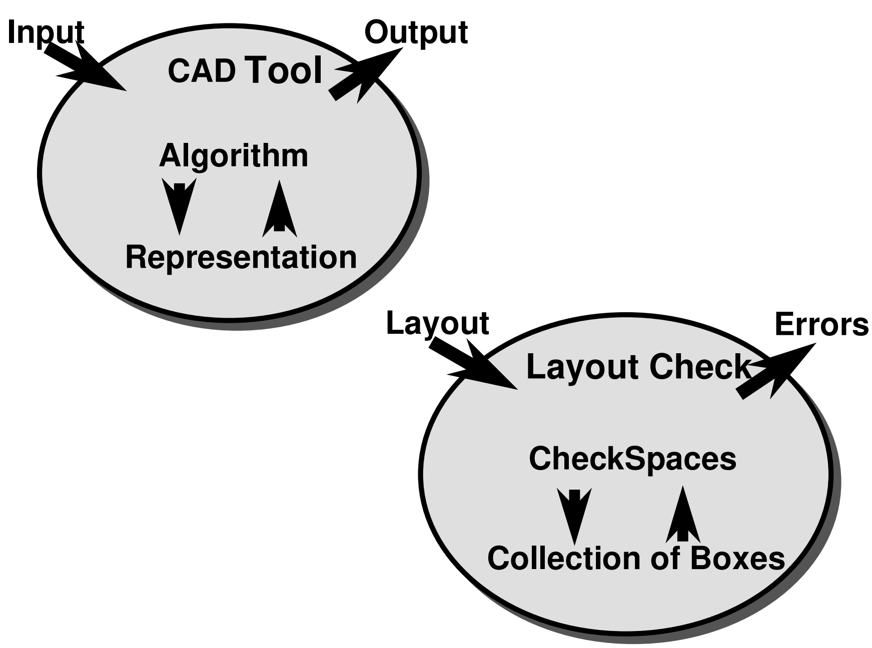
Implementation Fabric

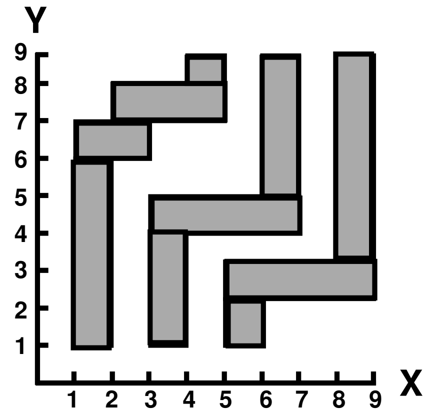
Architectural Style	MEMORY	LOGIC		PROCESSOR		
	SRAM, DRAM, ROM, Flash	Mask Programmed	Electrically Programmed	**General Purpose**	**DSP**	**ASSP**
Microcomputer	✔			✔✔	(✔)	(✔)
RAM/ROM	✔✔✔					
FPGA	✔		✔✔✔			
ASIC	✔	✔✔✔		(✔)	(✔)	(✔)
System-on-Chip (SOC)	✔	✔	✔	✔	✔	✔
Reconfigurable SOC	✔		✔✔✔	(✔)	(✔)	(✔)
Intelligent RAM	✔✔✔			✔		(✔)

✔✔✔ : major emphasis, ✔: present, (✔): option

Integrated Head-Mounted Display

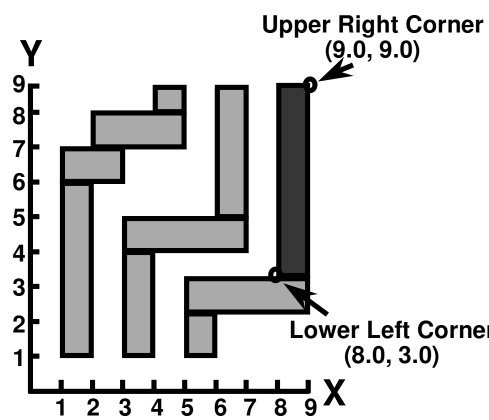




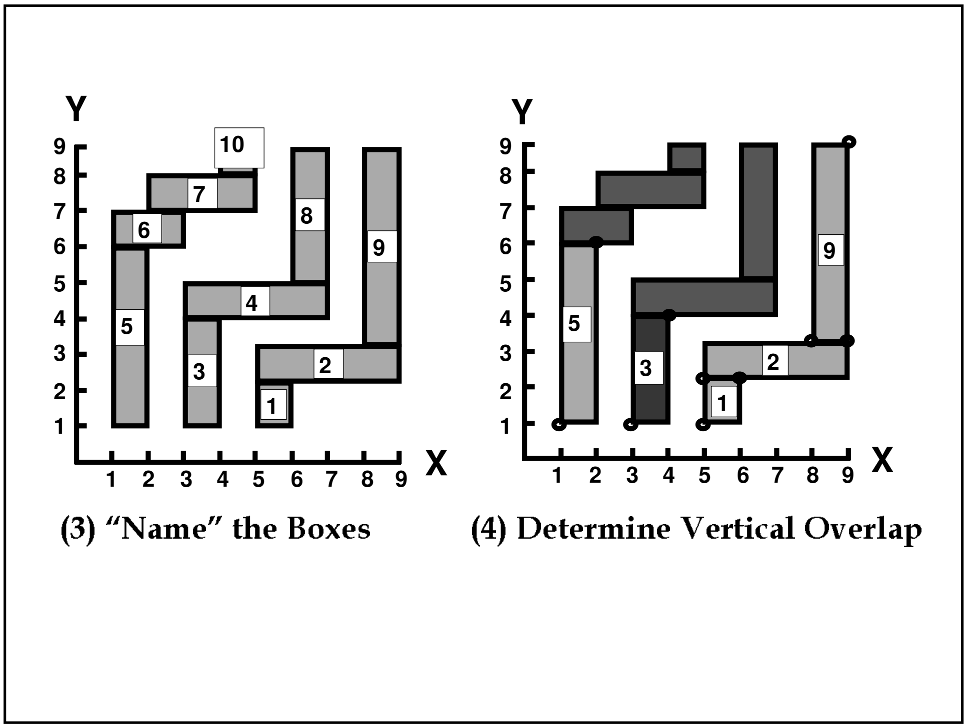


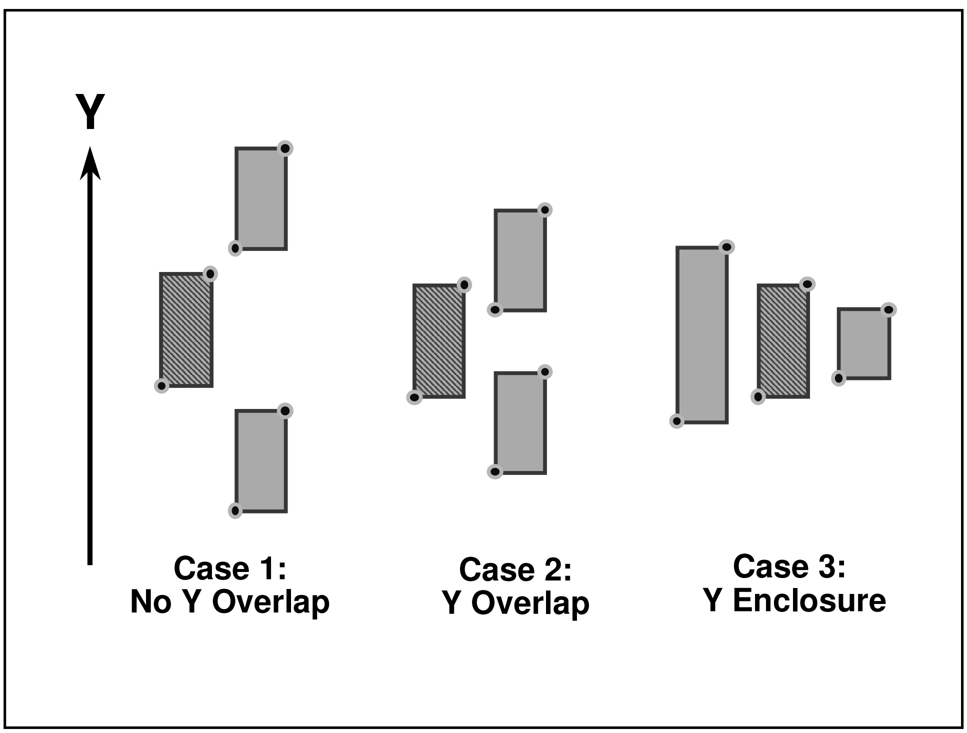
(1) Mask Layout

(2) Break into Boxes



lowerLeftX (LLX)	8.0
lowerLeftY (LLY)	3.0
upperRightX (URX)	9.0
upperRightY (URY)	9.0


Y
9
8
7
6
5
4
3
2
1
10
7
6
8
9
5
4
3
2
1
1 2 3 4 5 6 7 8 9
X
(3) "Name" the Boxes
Y
9
8
7
6
5
4
3
2
1
5
9
3
2
1
1 2 3 4 5 6 7 8 9
X
(4) Determine Vertical Overlap


Y
Case 1:
No Y Overlap
Case 2:
Y Overlap
Case 3:
Y Enclosure

```
checkYOverlap (box1, box2) {
    if(box1.LLY is greater than box2.URY)
        return(No)
    if(box1.URY is less than box2.LLY)
        return(No)
    otherwise, return(Yes)
}
```

```
checkSpaces (layout) {
    breakIntoBoxes (layout)
    forEach(box in layout, box1) {
        forEach(other box in layout, box2) {
            if( checkYOverlap (box1, box2) is Yes)
                checkXSpace (box1, box2)
            if( checkXOverlap (box1, box2) is Yes)
                checkYSpace (box1, box2)
        }}
end program
}
```

Summary

- **We must determine what are the predictable, optimal PDA circuit fabrics and associated architectures**
- **DSM implies many changes in physical design: Verification, "Route-then-Place," "Silicon Compilation," Timing and Power Issues, Communication Dominated Design**
- **Next step is: What are the best ways to represent the physical design problem and what are the metrics of a "good" design?**