EE244: Design Technology for Integrated Circuits and Systems
Outline
Lecture 6.2

◆ Regular Module Structures
  ▲ CMOS Synthetic Libraries
  ▲ Weinberger Arrays
  ▲ Gate Matrix
  ▲ Programmable Logic Array (PLA)
  ▲ Storage Logic Array (SLA)
  ▲ Programmable Path Logic (PPL)
◆ Automating the Design of Regular Structures

Single-Strip Static CMOS Layout
◆ Optimized for combinational strips in static CMOS

VDD
N-Well (pMOS)
P-Well (nMOS)
Polysilicon
GND

VDD
1
2
3
4
5
ρMOS
GND
nMOS
Single-Strip Static CMOS

CMOS Standard-Cell Layout

◆ X+YZ

Single-Strip Static CMOS

Optimized layout with ideal path and drain-source merging
Programmable Logic Array

Symbolic Layout

Single-Strip Static CMOS

X+YZ

CMOS Standard-Cell Layout
Single-Strip Static CMOS

- Dual graphs for P and N sides

Optimization of Static Strip Layout

- Uehara & Van Cleemput, 1981
  - Every gate-drain & gate-source potential is represented by a vertex.
  - Drains or sources at the same potential (connected) are represented by the same vertex.
  - Every transistor is represented by an edge connecting the drain and source vertices of that transistor.
  - “If two edges x and y in the graph are adjacent, then it is possible to place the corresponding transistors in physically adjacent positions of the same row, and hence connect them by a diffusion area. In order to minimize the number of separation areas, it is necessary to find a set of paths, of minimum size, which corresponds to chains of transistors in the row.”
Euler Path

◆ Is a path with no repeating edges that contains all the edges of the graph
◆ If such a path does not exist, the graph can be partitioned into subgraphs with Euler paths.
◆ Must find paths in the dual graphs with the same sequence of edges

Uehara and VanCleemput (1981)

◆ Enumerate all possible decompositions of the graph and find the minimum number of paths that cover the graph
◆ Chain the gates by means of shared diffusion areas according to the order of the edges in each Euler path
◆ If more than two Euler paths are needed to cover the graph model, provide separation between chains.
Heuristic Algorithm

- Relies on the fact that if the number of inputs to every AND/OR element is odd, then the corresponding graph has a single Euler path and there exists a graph such that the sequence of edges on the Euler path corresponds to the order of the inputs on a planar representation of the logic diagram.
- Convert every even number of parallel (series) edges into an odd one by adding pseudo pins.
- Minimize the interlace of pseudo pins and real pins.
- Find the Euler path (input sequence) and lay out the circuit.
- Delete pseudo pins and replace with separation areas.

Single-Strip Static CMOS

N-side Euler path: [1,3,2,4,5]

Dual Euler path: [2,3,1,4,5]
Gate Matrix Layout

- nMOS & pMOS implemented separately
Gate Matrix Layout

◆ Abstract representation, the connection graph and the interval graph