Lecture 27: Noise & Integration
Lecture Outline

• Reading: Senturia, Chpt. 16

• Lecture Topics:
  ➕ Noise
  ➕ MEMS/Transistor Integration
  ➕ Wrap Up
    ➕ Final Exam
    ➕ Next Week
Noise
Noise

• Noise: Random fluctuation of a given parameter \( I(t) \)

• In addition, a noise waveform has a zero average value

\[ I(t) \rightarrow \overline{I_D} \]

Avg. value (e.g. could be DC current)

\( t \)

• We can’t handle noise at instantaneous times

• But we can handle some of the averaged effects of random fluctuations by giving noise a power spectral density representation

• Thus, represent noise by its mean-square value:

Let \( i(t) = I(t) - I_D \)

Then \( i^2 = (I - I_D)^2 = \lim_{T \to \infty} \frac{1}{T} \int_0^T |I - I_D|^2 \, dt \)
Noise Spectral Density

• We can plot the spectral density of this mean-square value:

\[ \frac{i^2}{\Delta f} \] [units²/Hz]

One-sided spectral density → used in circuits → measured by spectrum analyzers

Two-sided spectral density (1/2 the one-sided)

Often used in systems courses

\(\bar{i^2} = \) integrated mean-square noise spectral density over all frequencies (area under the curve)
Circuit Noise Calculations

**Inputs**

- $v_i(j \omega)$
- $S_i(\omega)$

**Outputs**

- $v_o(j \omega)$
- $S_o(\omega)$

**Deterministic**

- $v_o(j \omega) = H(j \omega)v_i(j \omega)$

**Random**

- $S_o(\omega) = \left[H(j \omega)H^*(j \omega)\right]S_i(\omega) = \left|H(j \omega)\right|^2S_i(\omega)$

- $\sqrt{S_o(\omega)} = \left|H(j \omega)\right|\sqrt{S_i(\omega)}$

- How is it we can do this?

Mean square spectral density

**Root mean square amplitudes**

- No $j$ noise has random phase, so $j$ is pointless!
Handling Noise Deterministically

Can do this for noise in a tiny bandwidth (e.g., 1 Hz)

\[ \frac{v_{n1}^2}{\Delta f} = S_1(f) \quad \rightarrow \quad v_{n1} = \sqrt{S_1(f)} \cdot B \]

Can approximate this by a sinusoidal voltage generator (especially for small B, say 1 Hz)

\[ v_o(t) \sim A \cos \omega_o t \]

Why? Neither the amplitude nor the phase of a signal can change appreciably within a time period \(1/B\).

[This is actually the principle by which oscillators work. Oscillators are just noise going through a tiny bandwidth filter]
General Circuit With Several Noise Sources

- Assume noise sources are uncorrelated
  1. For $i_{n1}^2$, replace with a deterministic source of value

\[ i_{n1} = \sqrt{\frac{i_{n1}^2}{\Delta f}} \cdot (1 \text{ Hz}) \]
2. Calculate \( v_{on1}(\omega) = i_{n1}(\omega)H(j\omega) \) (treating it like a deterministic signal)

3. Determine \( v_{on1}^2 = i_{n1}^2 \cdot |H(j\omega)|^2 \)

4. Repeat for each noise source: \( i_{n1}^2, v_{n2}^2, v_{n3}^2 \)

5. Add noise power (mean square values)

\[
v_{onTOT}^2 = v_{on1}^2 + v_{on2}^2 + v_{on3}^2 + v_{on4}^2 + \cdots
\]

\[
v_{onTOT} = \sqrt{v_{on1}^2 + v_{on2}^2 + v_{on3}^2 + v_{on4}^2 + \cdots}
\]

Total rms value
Minimum Detectable Signal (MDS): Input signal level when the signal-to-noise ratio (SNR) is equal to unity

- The sensor scale factor is governed by the sensor type
- The effect of noise is best determined via analysis of the equivalent circuit for the system
LF155/LF156/LF256/LF257/LF355/LF356/LF357
JFET Input Operational Amplifiers

General Description
These are the first monolithic JFET input operational amplifiers to incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors (Bi-FET™ Technology). These amplifiers feature low input bias and offset currents/low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise corner.

Features
Advantages
- Replace expensive hybrid and module FET op amps
- Rugged JFETs allow blow-out free handling compared with MOSFET input devices
- Excellent for low noise applications using either high or low source impedance — very low 1/f corner
- Offset adjust does not degrade drift or common-mode rejection as in most monolithic amplifiers
- New output stage allows use of large capacitive loads (5,000 pF) without stability problems
- Internal compensation and large differential input voltage capability

Applications
- Precision high speed integrators
- Fast D/A and A/D converters
- High impedance buffers
- Wideband, low noise, low drift amplifiers

- Logarithmic amplifiers
- Photocell amplifiers
- Sample and Hold circuits

Common Features
- Low input bias current: 30pA
- Low Input Offset Current: 3pA
- High input impedance: 10^12Ω
- Low input noise current: 0.01 pA/√Hz
- High common-mode rejection ratio: 100 dB
- Large dc voltage gain: 106 dB

Uncommon Features

<table>
<thead>
<tr>
<th>LF155/ LF156/ LF256/ LF257/ LF355/ LF356/ LF357 (AV=5) Units</th>
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<tbody>
<tr>
<td>Extremely fast settling time to 0.01%</td>
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<tr>
<td>Fast slew rate</td>
</tr>
<tr>
<td>Wide gain bandwidth</td>
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<tr>
<td>Low input noise voltage</td>
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\[
\sqrt{\frac{V_{in}}{Af}} = 12 \text{nV/} \sqrt{\text{Hz}}
\]

\[
\sqrt{\frac{V_{in}}{Af}} = 0.01 \text{pA/} \sqrt{\text{Hz}}
\]
Minimum Detectable Signal (MDS)

- Minimum Detectable Signal (MDS): Input signal level when the signal-to-noise ratio (SNR) is equal to unity

- The sensor scale factor is governed by the sensor type
- The effect of noise is best determined via analysis of the equivalent circuit for the system
Move Noise Sources to a Common Point

• Move noise sources so that all sum at the input to the amplifier circuit (i.e., at the output of the sense element)
• Then, can compare the output of the sensed signal directly to the noise at this node to get the MDS
Gyro Readout Equivalent Circuit (for a single tine)

\[ \vec{F}_c = m\vec{a}_c = m \cdot (2\vec{\dot{x}}_d \times \vec{\Omega}) \]

Noise Sources

\[ \eta_e:1 \]

Gyro Sense Element Output Circuit

Signal Conditioning Circuit (Transresistance Amplifier)

* Easiest to analyze if all noise sources are summed at a common node
\[ \vec{F}_c = m \vec{a}_c = m \cdot (2 \ddot{x}_d \times \vec{\Omega}) \]

\[ \eta_e : 1 \]

\[ i_o \rightarrow v_{eq}^2 \]

\[ \eta_e : 1 \]

\[ i_{eq}^2 \]

\[ v_0 \]

\[ C_p \]

\[ R_f \]

\[ F_c \]

\[ l_x \]

\[ c_x \]

\[ f_{r_x}^2 \]

\[ r_x \]

\[ x \]

\[ \text{Gyro Sense Element} \]

\[ \text{Signal Conditioning Circuit (Transresistance Amplifier)} \]

\[ \text{Here, } v_{eq}^2 \text{ and } i_{eq}^2 \text{ are equivalent input-referred voltage and current noise sources} \]
Example: Gyro MDS Calculation (cont)

\[ F_c = m \ddot{a}_c = m \cdot (2 \dddot{x}_d \times \ddot{\Omega}) \]

\[ \begin{align*}
    l_x & \quad c_x & \quad f_{x}^2 & \quad r_x & \quad \eta_e: 1 \\
    \sqrt{ } & \quad \sqrt{ } & \quad \sqrt{ } & \quad \sqrt{ } & \quad \sqrt{ }
\end{align*} \]

Now, find the \( i_{eqTOT} \) entering the amplifier input:

\[ i_{eqTOT}^2 = i_s^2 + i_{eq}^2 \]  

\[ i_{eqTOT}^2 = i_s^2 + i_f^2 + i_{oa}^2 + \frac{N_{oa}^2}{R_f^2} \]  

\[ \frac{f_{rx}^2}{\Delta f} = 4kTf_{rx} \]

Brownian motion noise of the sense element \( \rightarrow \) determined entirely by the noise in \( r_x \rightarrow f_{rx}^2 \) easiest to convert to an all electrical equiv. ckt.
Example: Gyro MDS Calculation (cont)

\[ L_x C_x R_x \rightarrow \frac{i_s^2}{1_s^2} \rightarrow \frac{1_s^2}{1_s^2} \rightarrow \frac{1_s^2}{1_s^2} \rightarrow \frac{1_s^2}{1_s^2} \rightarrow \text{To Amplifier Input} \]

\[ N_{R_x}^2 = 4kT R_x \]

where \( L_x = \frac{\eta_e^2}{\eta_e} \), \( C_x = \eta_e^2 C_x \), \( R_x = \frac{R_x^2}{\eta_e} \)

\[ i_s = N_{R_x} \left( \frac{1}{R_x} \right) \Theta(jw_d) \rightarrow \frac{i_s^2}{\delta f} = 4kT R_x \left( \frac{1}{R_x^2} \right) |\Theta(jw_d)|^2 \]

\[ \Rightarrow \frac{i_s^2}{\delta f} = \frac{4kT}{R_x} |\Theta(jw_d)|^2 \]

Thus:

\[ \frac{i_s^2}{\delta f} = \frac{4kT}{R_x} |\Theta(jw_d)|^2 + \frac{1}{\delta f} + \frac{\overline{V_{ia}}}{\delta f} + \frac{\overline{V_{ia}}}{\delta f} \left( \frac{1}{R_f^2} \right) \]

Learn to get these from EE240, or just get them from a data sheet...
Example: Gyro MDS Calculation (cont)

\[ \ddot{F}_c = m \ddot{a}_c = m \cdot (2 \dot{x}_d \times \dot{\Omega}) \]

\[ F_c \]

\[ l_x \quad c_x \quad f_{rx}^2 \quad r_x \]

\[ \eta_e:1 \]

\[ \eta \]

\[ \dot{x}_s \]

\[ \dot{F}_c \]

\[ R_f \]

\[ C_p \]

\[ v_{eq} \]

\[ i_{eq} \]

\[ \Theta(j\omega) \]

\[ \frac{\omega_s Q}{k_s} \]

\[ \frac{\omega_s Q}{2\omega_d \chi_d \Omega m} \]

\[ \dot{x}_s = \frac{\omega_s Q}{k_s} (\Theta(j\omega)) \]

\[ [F_s = F_c = 2\omega_d \chi_d \Omega m] \]

\[ \dot{x}_s = 2 \frac{\omega_d Q \chi_d \Theta(j\omega)}{\omega_s} \]

Noiseless

• First, find the rotation to \( i_o \) transfer function:

\[ i_o \]

\[ \frac{v_{eq}^2}{i_{eq}^2} \]

\[ v_0 \]

\[ \frac{1}{\omega_s^2} \]
Example: Gyro MDS Calculation (cont)

\[ \dot{i}_0 = \eta e \dot{x}_S = 2 \frac{\omega_d}{\omega_s} Q X_d \eta e \Theta(j \omega_d) \cdot \mathbb{N} \Rightarrow i_0 = A \mathbb{N} \]

Where \( A = 2 \frac{\omega_d}{\omega_s} Q X_d \eta e \Theta(j \omega_d) \)

\[
\text{When } \mathbb{N} = \mathbb{N}_{\text{min}} = \text{MDS}, \ i_0 = i_{\text{eqtot}} \quad \text{input-referred noise current entering the sense amplifier} \rightarrow \text{in } pA/\sqrt{\text{Hz}}
\]

\[ i_{\text{eqtot}} = A \mathbb{N}_{\text{min}} \Rightarrow \mathbb{N}_{\text{min}} = \frac{i_{\text{eqtot}}}{A} \left( \frac{3600 \text{s}}{\text{hr}} \right) \left( \frac{180}{\pi} \right) \left[ \left( \% \text{hr} \right)/\sqrt{\text{Hz}} \right] \]

Angle Random Walk: \( \text{ARW} = \frac{1}{60} \mathbb{N}_{\text{min}} \left[ \% \text{hr} \right] \)

Easier to determine directional error as a function of elapsed time.
Sensing Circuits (cont)
Problems With Pure-C Position Sensing

• To sense position (i.e., displacement), use a capacitive load

\[
\frac{V_o}{V_i} = \frac{C_x/C_D}{1 + C_x/C_D} \cdot \frac{1}{s} \cdot \Theta(s, \omega_0, Q) \cdot \omega_0/\omega
\]

Integration yields displacement.

To maximize gain, minimize \( \omega_0 \).

\( \Rightarrow \) Problem: parasitic capacitance

\[ C_D \rightarrow C_D + C_{pi} + C_{pb} \]

\( \Rightarrow \) DC Gain: \[
\frac{C_x/(C_D + C_{pi} + C_{pb})}{1 + C_x/(C_D + C_{pi} + C_{pb})}
\]

Remedy: Suppress \( C_p \) via use of op amps.
The Op Amp Integrator Advantage

- The virtual ground provided by the ideal op amp eliminates the parasitic capacitance $C_p$

$F_{dl}$

$\begin{align*}
I_0 & = -i_0 \left( R_2 \frac{1}{sC_2} \right) \\
& \approx - \frac{\dot{N}_i}{R_X} \Theta(s) \frac{1}{sC_2}
\end{align*}$

$\frac{N_o(s)}{N_i} = -\frac{1}{R_X C_2 s}$

Can drive next stage’s $R_1$ w/o interference to transfer function!

$R_0 = 0 \Omega$
Integration of MEMS and Transistors
Merged MEMS/Transistor Technologies (Process Philosophy)

MEMS-Last:
- Circuits
- Pass./Prot.
- μMechanics

Mixed:
- Circuits
- Pass./Prot.
- μMechanics
- Pass./Prot.

MEMS-First:
- μMechanics
- Pass./Prot.
- Circuits

**Mixed:**
- **Problem:** multiple passivation/protection steps ⇒ large number of masks required
- **Problem:** custom process for each product

**MEMS-first or MEMS-last:**
- **Adv.:** modularity ⇒ flexibility ⇒ less development time
- **Adv.:** low pass./protection complexity ⇒ fewer masks
Analog Devices BiMEMS Process

- Interleaved MEMS and 4 μm BiMOS processes (28 masks)
- Diffused n+ runners used to interconnect MEMS & CMOS
- Relatively deep junctions allow for MEMS poly stress anneal
- Used to manufacture the ADXL-50 accelerometer and Analog Devices family of accelerometers

![Diagram of BiMEMS process](image)
Analog Devices BiMEMS Process (cont)

• Examples:

![Analog Devices ADXL 78](image1)

Old → New

![Analog Devices ADXL-202 Multi-Axis Accelerometer](image2)

• Can you list the advances in the process from old to new?
250 nm CMOS Cross-Section

2nd Level Metal Interconnect (e.g., Cu)

1st Level Metal Interconnect (e.g., Al)

LPCVD SiO$_2$

CVD Tungsten

TiN Local Interconnect

Lightly Doped Drain (LDD)

28 masks and a lot more complicated than MEMS!
Merged MEMS/Transistor Technologies (Process Philosophy)

- **Mixed:**
  - **problem:** multiple passivation/protection steps \(\Rightarrow\) large number of masks required
  - **problem:** custom process for each product

- **MEMS-first or MEMS-last:**
  - **adv.** modularity \(\Rightarrow\) flexibility \(\Rightarrow\) less development time
  - **adv.** low pass./protection complexity \(\Rightarrow\) fewer masks
MEMS-First Integration

• **Problem:** μstructural topography interferes with lithography
difficult to apply photoresist for submicron circuits

  - Photoresist Wellng
  - 6-10μm
  - Structural Poly-si
  - Sacrificial Oxide
  - Nitride
  - Thinning Due to Streaking While Spinning
  - Silicon Substrate

• **Soln.:** build μmechanics in a trench, then planarize before circuit processing [Smith et al, IEDM'95]

  - Silicon for Circuits
  - Contact to Circuits Made Here
  - Micromechanics Trench
  - Surface and Structures Planarized Via CMP
  - Epitaxial Layer
  - Polysilicon Stud
  - Structural Poly-si
  - Sacrificial Oxide
  - Silicon Substrate
MEMS-First Ex: Sandia's iMEMS

- Used to demonstrate functional fully integrated oscillators

- **Issues:**
  - Lithography and etching may be difficult in trench → may limit dimensions (not good for RF MEMS)
  - μmechanical material must stand up to IC temperatures (>1000°C) → problem for some metal materials
  - Might be contamination issues for foundry IC's

[Smith et al, IEDM’95]
Bosch/Stanford MEMS-First Process

- Single-crystal silicon microstructures sealed under epi-poly encapsulation covers
- Many masking steps needed, but very stable structures

[Image of MEMS design with labels: Epi-Poly Seal, Epi-Poly Cap, Contact, Substrate, Transistor Circuits, Vacuum Chamber, μMechanical Device, Epi-silicon for CMOS, Resonator, [Kim, Kenny Trans'05]]

[Diagram showing layers and components of MEMS design: Silicon, Oxide, Sensor Structure, Silicon, p-plus, Nonconformal LTO, Monocrystalline Silicon, Polycrystalline Silicon, Vent, Nonconformal LTO, Aluminum Pad]
Merged MEMS/Transistor Technologies (Process Philosophy)

Post-Circuits: Circuits → Pass./Prot. → μMechanics

Mixed: Circuits → Pass./Prot. → μMechanics → Pass./Prot.

Pre-Circuits: μMechanics → Pass./Prot. → Circuits

• **Mixed:**
  - **problem**: multiple passivation/protection steps ⇒ large number of masks required
  - **problem**: custom process for each product

• **MEMS-first or MEMS-last:**
  - **adv.**: modularity ⇒ flexibility ⇒ less development time
  - **adv.**: low pass./protection complexity ⇒ fewer masks
Berkeley Polysilicon MICS Process

- Uses surface-micromachined polysilicon microstructures with silicon nitride layer between transistors & MEMS
  - Polysilicon dep. $T \approx 600^\circ C$; nitride dep. $T \approx 835^\circ C$
  - $1100^\circ C$ RTA stress anneal for 1 min.
  - Metal and junctions must withstand temperatures $\approx 835^\circ C$
  - Tungsten metallization used with TiSi$_2$ contact barriers
  - *in situ* doped structural polySi; rapid thermal annealing

**Diagram:**
- Ground Plane Polysilicon
- Structural Polysilicon (Suspended Beams)
- Poly-to-Poly Capacitor
- Si$_3$N$_4$
- TiSi$_2$ Contact Barrier
- Tungsten Interconnect
- Thermal SiO$_2$
- n-substrate
- pwell
Single-Chip Ckt/MEMS Integration

- Completely monolithic, low phase noise, high-Q oscillator (effectively, an integrated crystal oscillator)

To allow the use of >600°C processing temperatures, tungsten (instead of aluminum) is used for metallization

[Nguyen, Howe 1993]
**Problem**: tungsten is not an accepted primary interconnect metal

**Challenge**: retain conventional metallization

- minimize post-CMOS processing temperatures
- explore alternative structural materials (e.g., plated nickel, SiGe [Franke, Howe et al, MEMS'99])

Limited set of usable structural materials → not the best situation, but workable
UCB Poly-SiGe MICS Process

- 2 μm standard CMOS process w/ Al metallization
- P-type poly-Si$_{0.35}$Ge$_{0.65}$ structural material; poly-Ge sacrificial material

Process:
- Passivate CMOS w/ LTO @ 400°C
- Open vias to interconnect runners
- Deposit & pattern ground plane
- RTA anneal to lower resistivity (550°C, 30s)
Wrap Up