UC Berkeley

EE C245 – ME C218
Introduction to MEMS Design
Fall 2008

Prof. Clark T.-C. Nguyen

Dept. of Electrical Engineering & Computer Sciences
University of California at Berkeley
Berkeley, CA 94720

Lecture 27: Noise & Integration

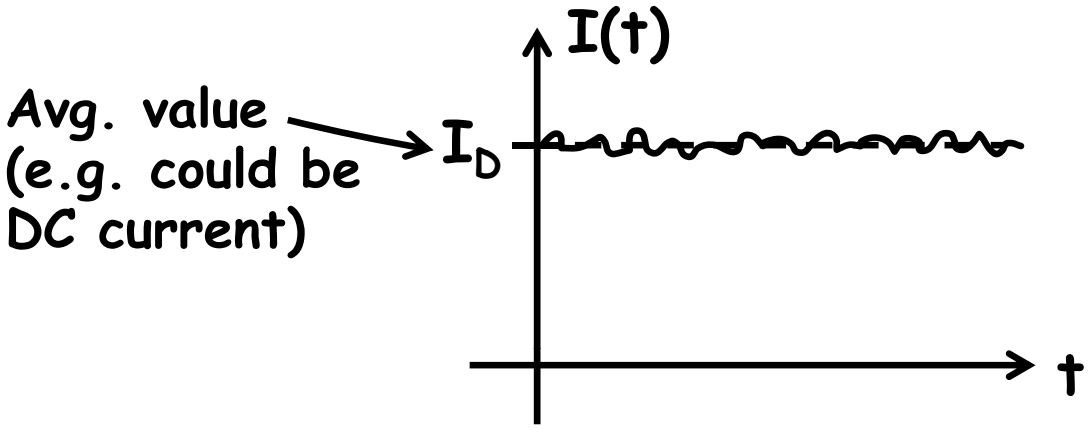
Lecture Outline

- Reading: Senturia, Chpt. 16
- Lecture Topics:
  - Noise
  - MEMS/Transistor Integration
  - Wrap Up
    - Final Exam
    - Next Week

Noise

Noise

- Noise: Random fluctuation of a given parameter I(t)
- In addition, a noise waveform has a zero average value



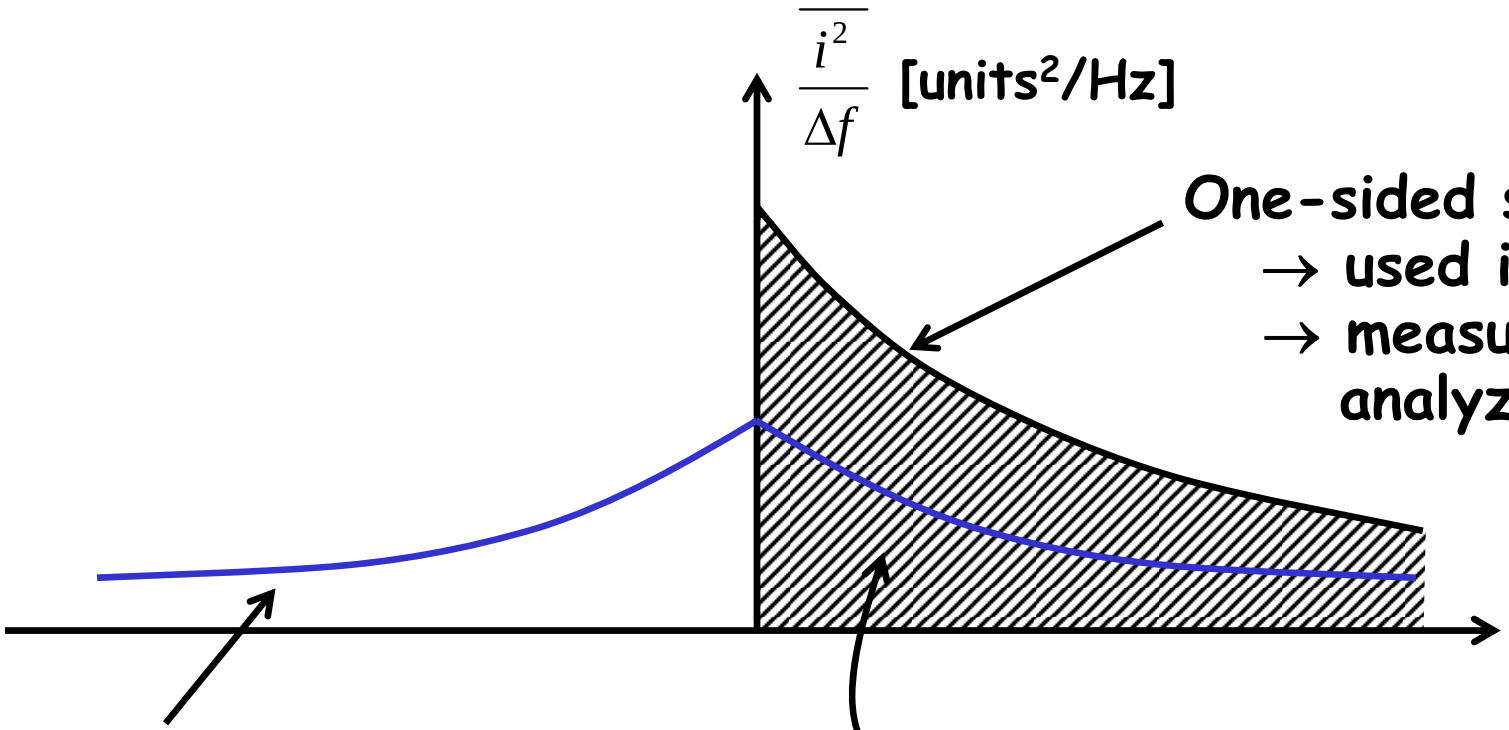
- We can't handle noise at instantaneous times
- But we can handle some of the averaged effects of random fluctuations by giving noise a power spectral density representation
- Thus, represent noise by its mean-square value:

Let $i(t) = I(t) - I_D$

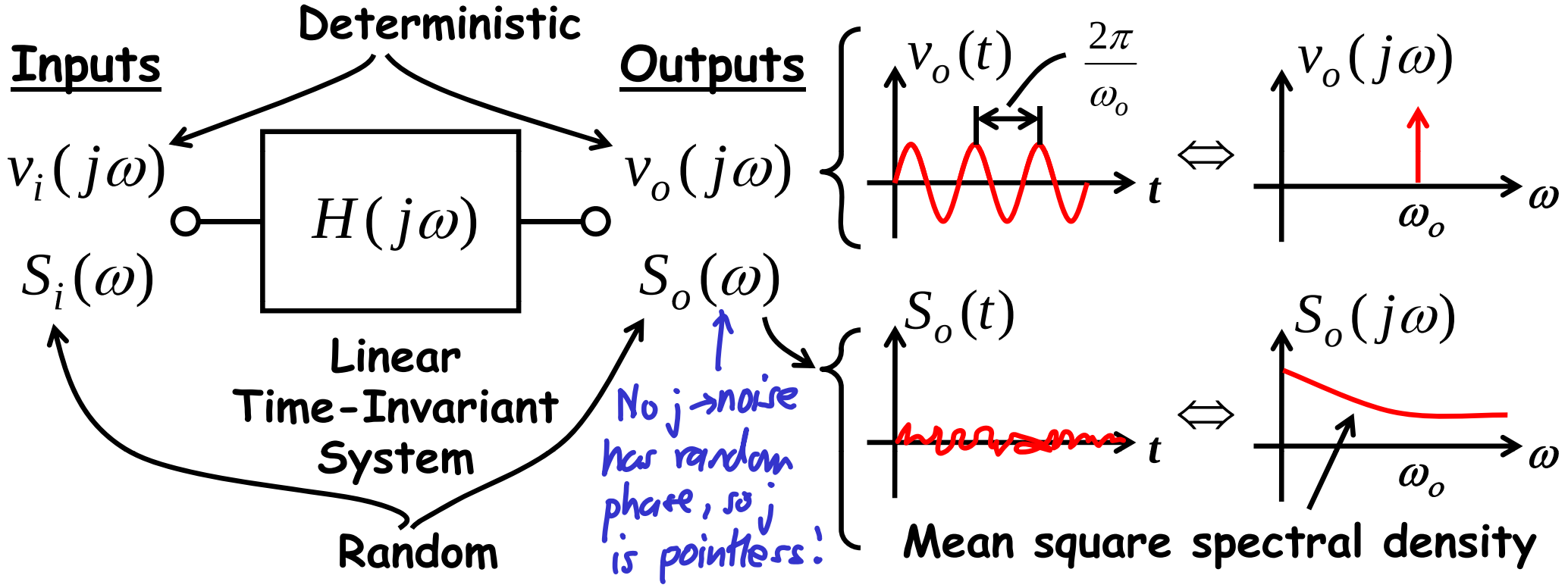
Then $\overline{i^2} = \overline{(I - I_D)^2} = \lim_{T\to\infty} \frac{1}{T} \int_0^T |I - I_D|^2 \, dt$

Noise Spectral Density

- We can plot the spectral density of this mean-square value:



Circuit Noise Calculations



- **Deterministic:** $v_o(j\omega) = H(j\omega)v_i(j\omega)$

- **Random:** $S_o(\omega) = \left[H(j\omega)H^*(j\omega)\right]S_i(\omega) = \left|H(j\omega)\right|^2 S_i(\omega)$

$$\sqrt{S_o(\omega)} = \left|H(j\omega)\right|\sqrt{S_i(\omega)}$$

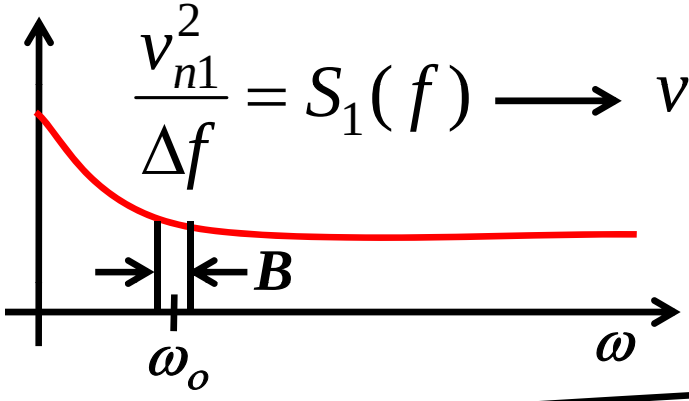
How is it we can do this?

Root mean square amplitudes

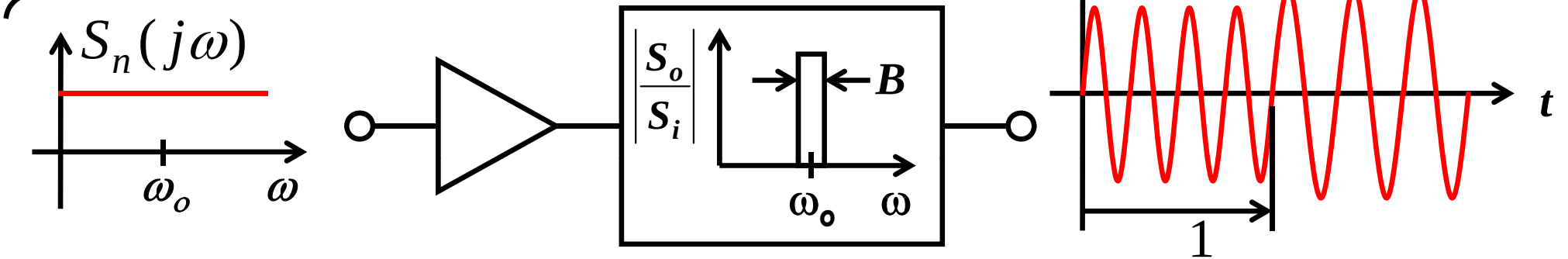
Handling Noise Deterministically

- Can do this for noise in a tiny bandwidth (e.g., 1 Hz)

$$\frac{\overline{v_{n1}^2}}{\Delta f} = S_1(f) \longrightarrow v_{n1} = \sqrt{S_1(f) \cdot B}$$



→ Can approximate this by a sinusoidal voltage generator (especially for small B, say 1 Hz)

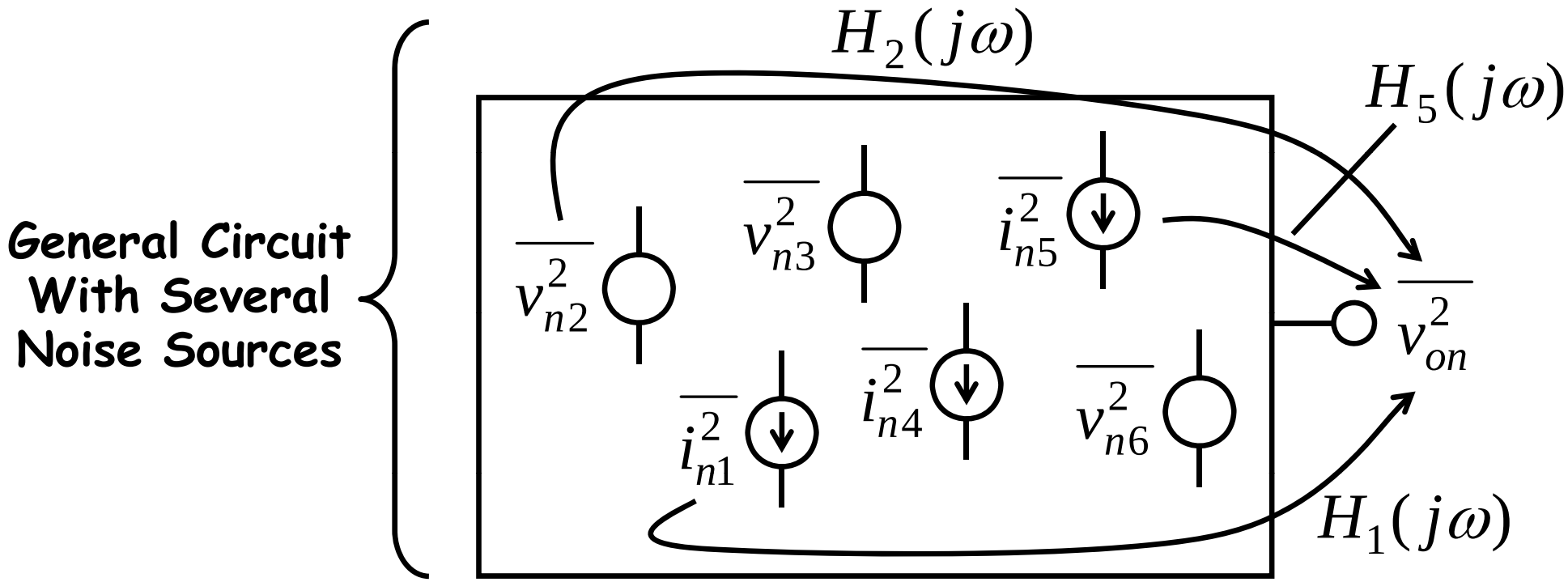


$$\tau \sim \frac{1}{B}$$

[This is actually the principle by which oscillators work → oscillators are just noise going through a tiny bandwidth filter]

Why? Neither the amplitude nor the phase of a signal can change appreciably within a time period 1/B.

Systematic Noise Calculation Procedure



- Assume noise sources are uncorrelated
  1. For $\overline{i_{n1}^2}$, replace w/ a deterministic source of value

$$i_{n1} = \sqrt{\frac{\overline{i_{n1}^2}}{\Delta f} \cdot (1\,\text{Hz})}$$

Systematic Noise Calculation Procedure

UC Berkeley

2. Calculate $v_{on1}(\omega) = i_{n1}(\omega)H(j\omega)$ (treating it like a deterministic signal)
3. Determine $\overline{v_{on1}^2} = \overline{i_{n1}^2} \cdot \left|H(j\omega)\right|^2$
4. Repeat for each noise source: $\overline{i_{n1}^2}, \overline{v_{n2}^2}, \overline{v_{n3}^2}$
5. Add noise power (mean square values)

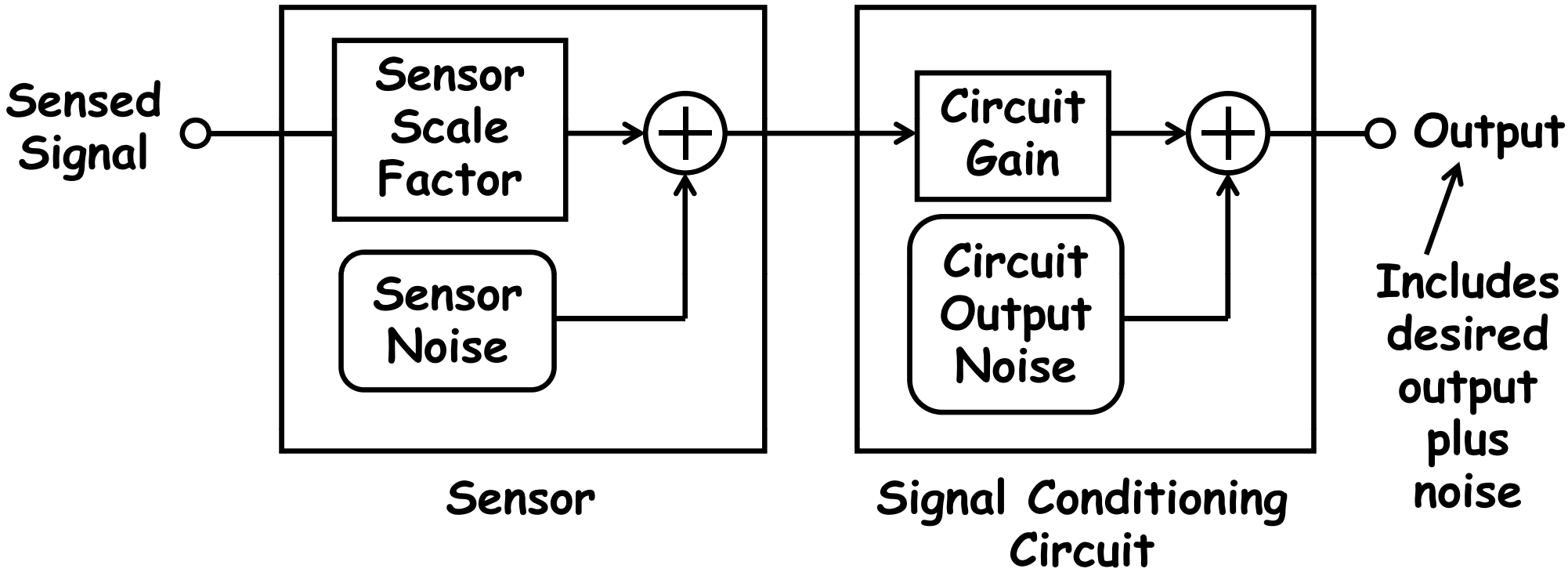
$$\overline{v_{onTOT}^2} = \overline{v_{on1}^2} + \overline{v_{on2}^2} + \overline{v_{on3}^2} + \overline{v_{on4}^2} + \cdots$$

$$v_{onTOT} = \sqrt{\overline{v_{on1}^2} + \overline{v_{on2}^2} + \overline{v_{on3}^2} + \overline{v_{on4}^2} + \cdots}$$

Total rms value

Minimum Detectable Signal (MDS)

- Minimum Detectable Signal (MDS): Input signal level when the signal-to-noise ratio (SNR) is equal to unity



- The sensor scale factor is governed by the sensor type
- The effect of noise is best determined via analysis of the equivalent circuit for the system

LF356 Op Amp Data Sheet

UC Berkeley

LF155/LF156/LF256/LF257/LF355/LF356/LF357
JFET Input Operational Amplifiers

General Description

These are the first monolithic JFET input operational amplifiers to incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors (BI-FET™ Technology). These amplifiers feature low input bias and offset currents/low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise corner.

Features

Advantages

- Replace expensive hybrid and module FET op amps
- Rugged JFETs allow blow-out free handling compared with MOSFET input devices
- Excellent for low noise applications using either high or low source impedance—very low 1/f corner
- Offset adjust does not degrade drift or common-mode rejection as in most monolithic amplifiers
- New output stage allows use of large capacitive loads (5,000 pF) without stability problems
- Internal compensation and large differential input voltage capability

Applications

- Precision high speed integrators
- Fast D/A and A/D converters
- High impedance buffers
- Wideband, low noise, low drift amplifiers
- Logarithmic amplifiers
- Photocell amplifiers
- Sample and Hold circuits

Common Features

- Low input bias current: 30pA
- Low Input Offset Current: 3pA
- High input impedance: $10^{12}\Omega$
- Low input noise current: 0.01 pA/√Hz
- High common-mode rejection ratio: 100 dB
- Large dc voltage gain: 106 dB

$\sqrt{\frac{\overline{i_{na}^2}}{\Delta f}} = 0.01\ \text{pA}/\sqrt{\text{Hz}}$

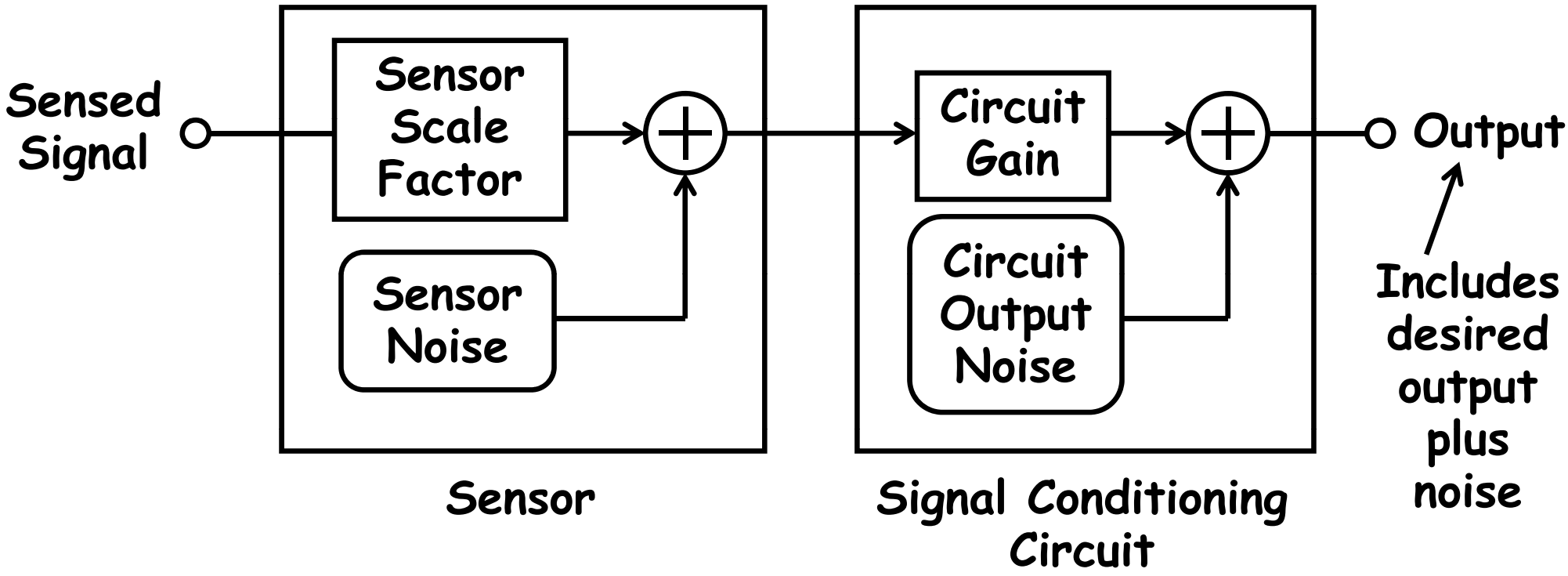
Uncommon Features

	LF155/ LF355	LF156/ LF256/ LF356	LF257/ LF357 (A_V=5)	Units
■ Extremely fast settling time to 0.01%	4	1.5	1.5	µs
■ Fast slew rate	5	12	50	V/µs
■ Wide gain bandwidth	2.5	5	20	MHz
■ Low input noise voltage	20	12	12	nV/√Hz

$\sqrt{\frac{\overline{v_{na}^2}}{\Delta f}} = 12\ \text{nV}/\sqrt{\text{Hz}}$

Minimum Detectable Signal (MDS)

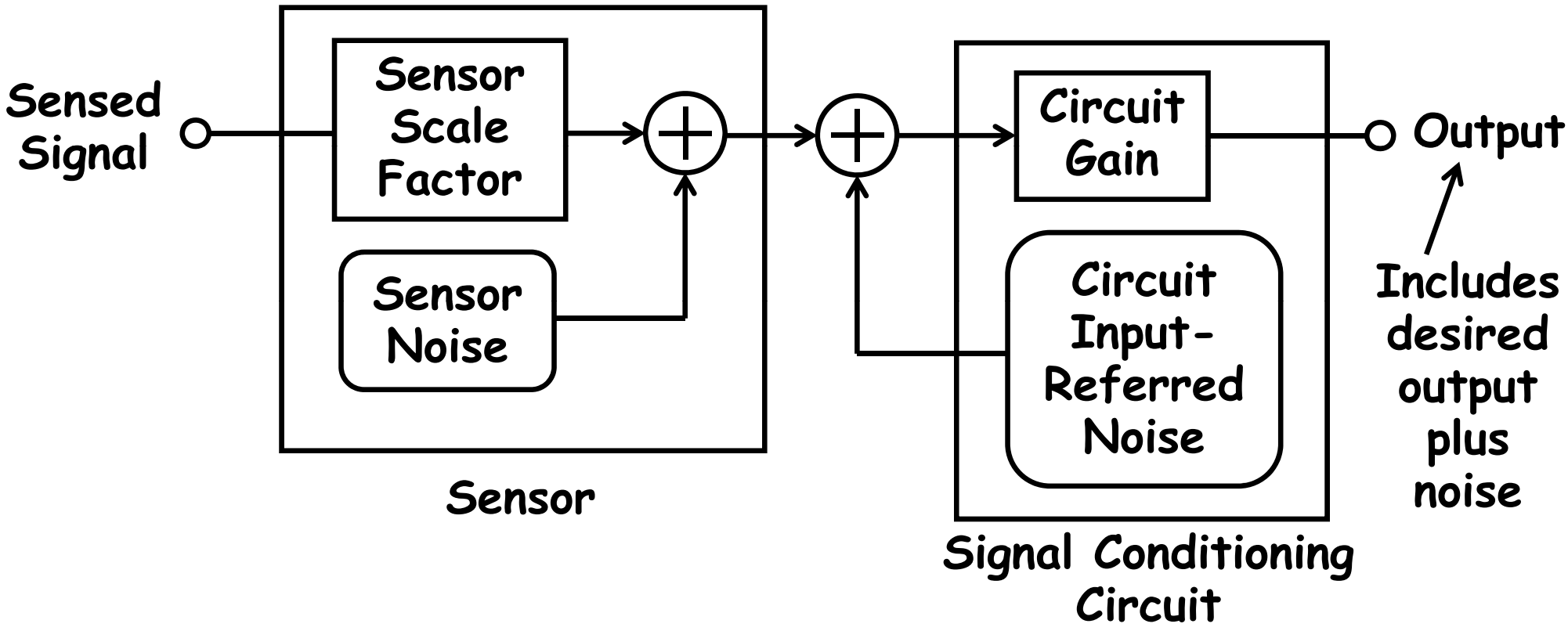
- Minimum Detectable Signal (MDS): Input signal level when the signal-to-noise ratio (SNR) is equal to unity



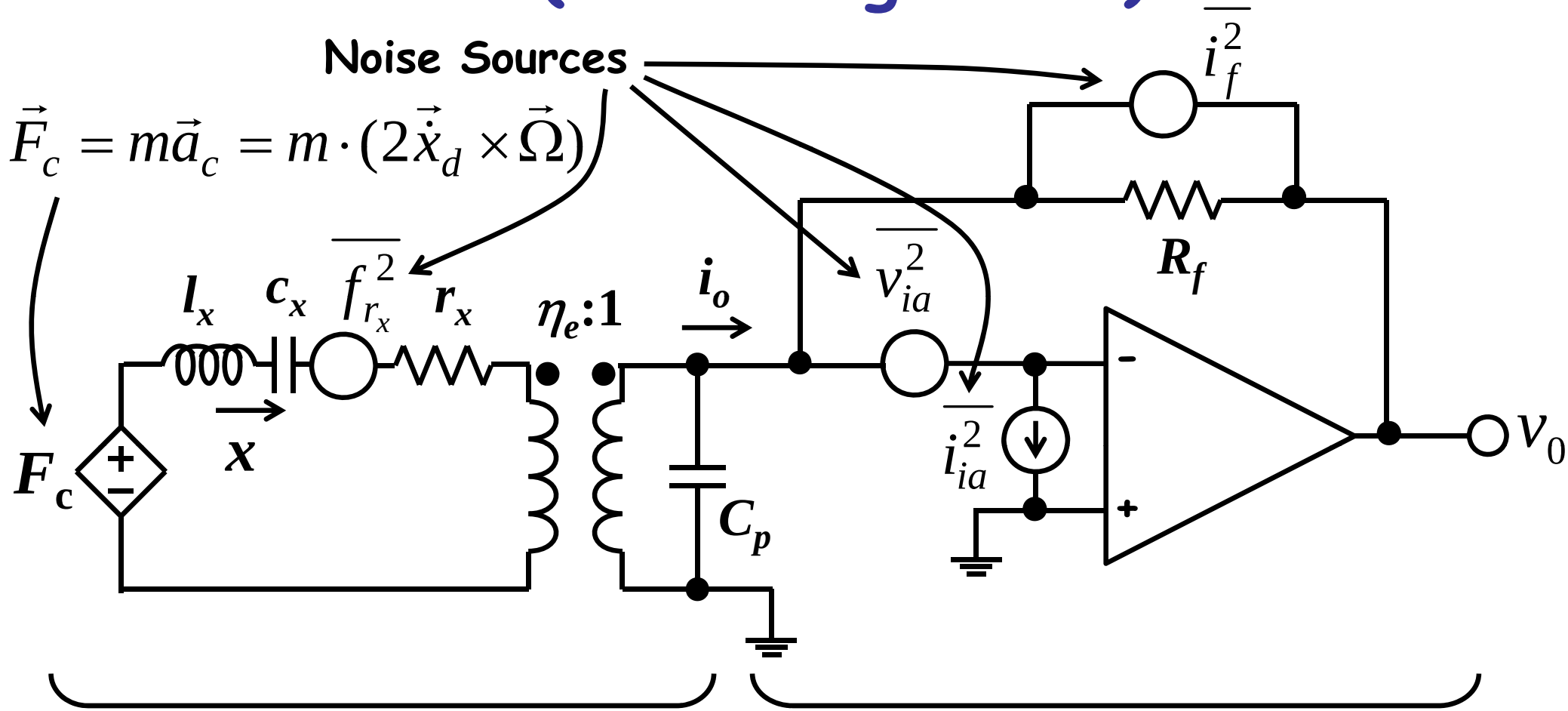
- The sensor scale factor is governed by the sensor type
- The effect of noise is best determined via analysis of the equivalent circuit for the system

Move Noise Sources to a Common Point

- Move noise sources so that all sum at the input to the amplifier circuit (i.e., at the output of the sense element)
- Then, can compare the output of the sensed signal directly to the noise at this node to get the MDS

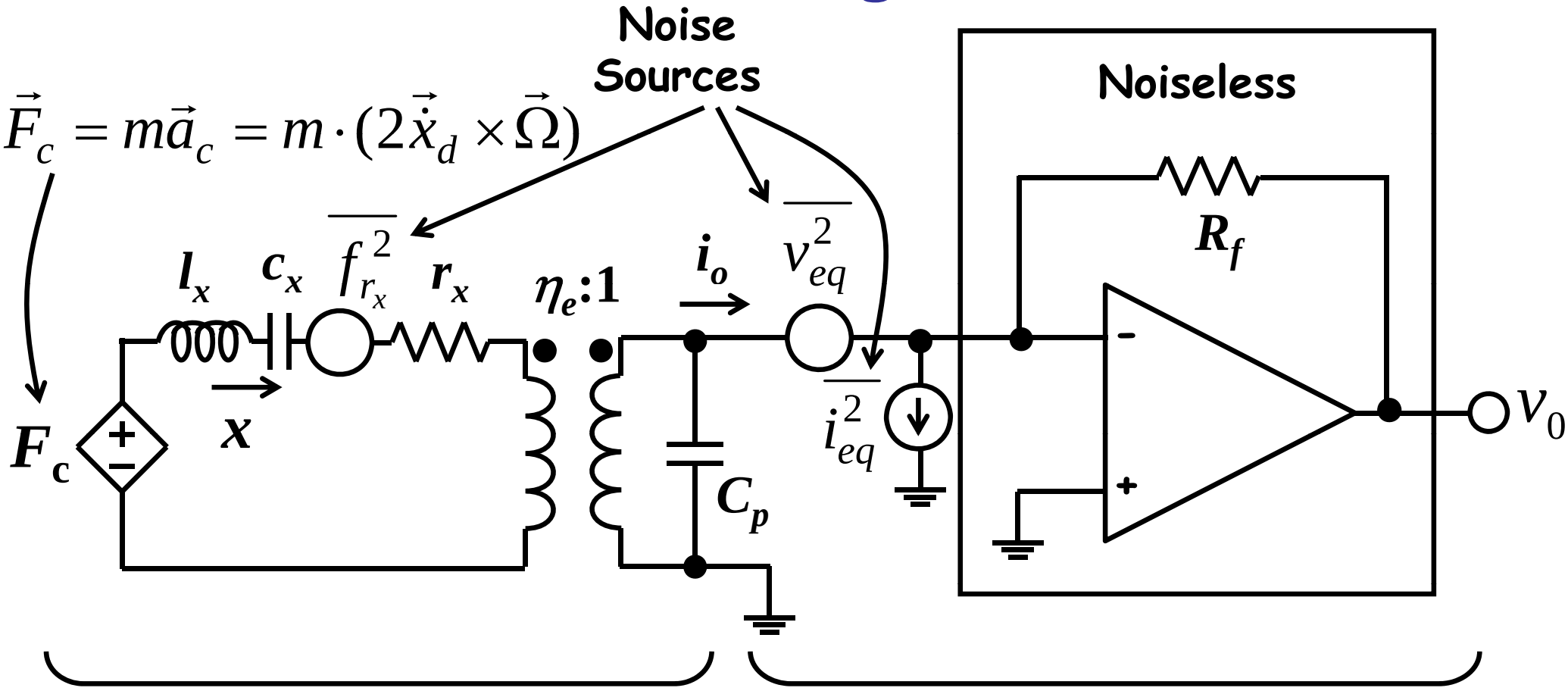


Gyro Readout Equivalent Circuit (for a single tine)



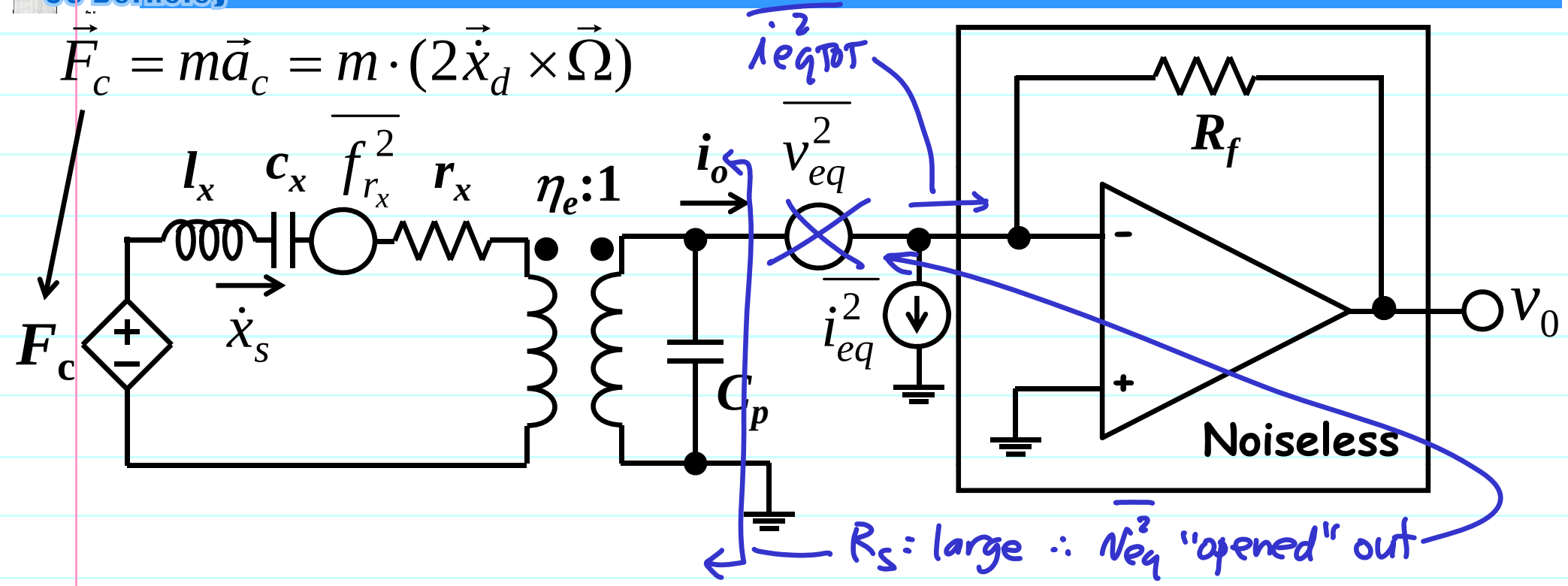
- Easiest to analyze if all noise sources are summed at a common node

Gyro Readout Equivalent Circuit (for a single tine)



- Here, $\overline{v_{eq}^2}$ and $\overline{i_{eq}^2}$ are equivalent input-referred voltage and current noise sources

Example: Gyro MDS Calculation (cont)



- Now, find the i_{eqTOT} entering the amplifier input:

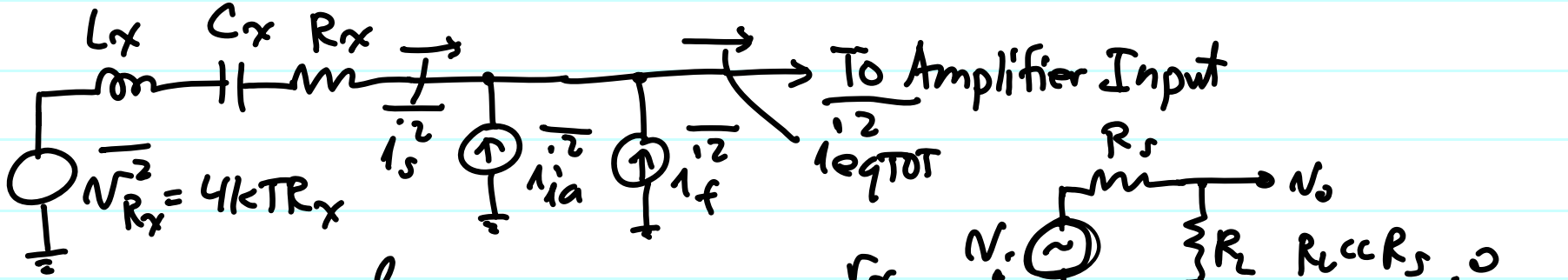
$$\overline{i_{eqTOT}^2} = \overline{i_S^2} + \overline{i_{eqA}^2} \rightarrow \overline{i_{eqTOT}^2} = \overline{i_S^2} + \overline{i_f^2} + \overline{i_{ia}^2} + \frac{\overline{v_{ia}^2}}{R_f^2}$$

$$\frac{\overline{f_{r_x}^2}}{\Delta f} = 4kTr_x$$

↑ Brownian motion noise of the sense element → determined entirely by the noise in r_x → $\overline{f_{r_x}^2}$

↳ easiest to convert to an all electrical equiv. ckt.

Example: Gyro MDS Calculation (cont)



where $L_x = \frac{L_x}{\eta_e^2}$, $C_x = \eta_e^2 C_x$, $R_x = \frac{r_x}{\eta_e^2}$

$$\therefore \; i_s = v_{R_x}\left(\frac{1}{R_x}\right)\mathcal{H}(j\omega_d) \rightarrow \frac{\overline{i_s^2}}{\Delta f} = 4kTR_x\left(\frac{1}{R_x^2}\right)|\mathcal{H}(j\omega_d)|^2$$

$$\Rightarrow \boxed{\frac{\overline{i_s^2}}{\Delta f} = \frac{4kT}{R_x}|\mathcal{H}(j\omega_d)|^2}$$

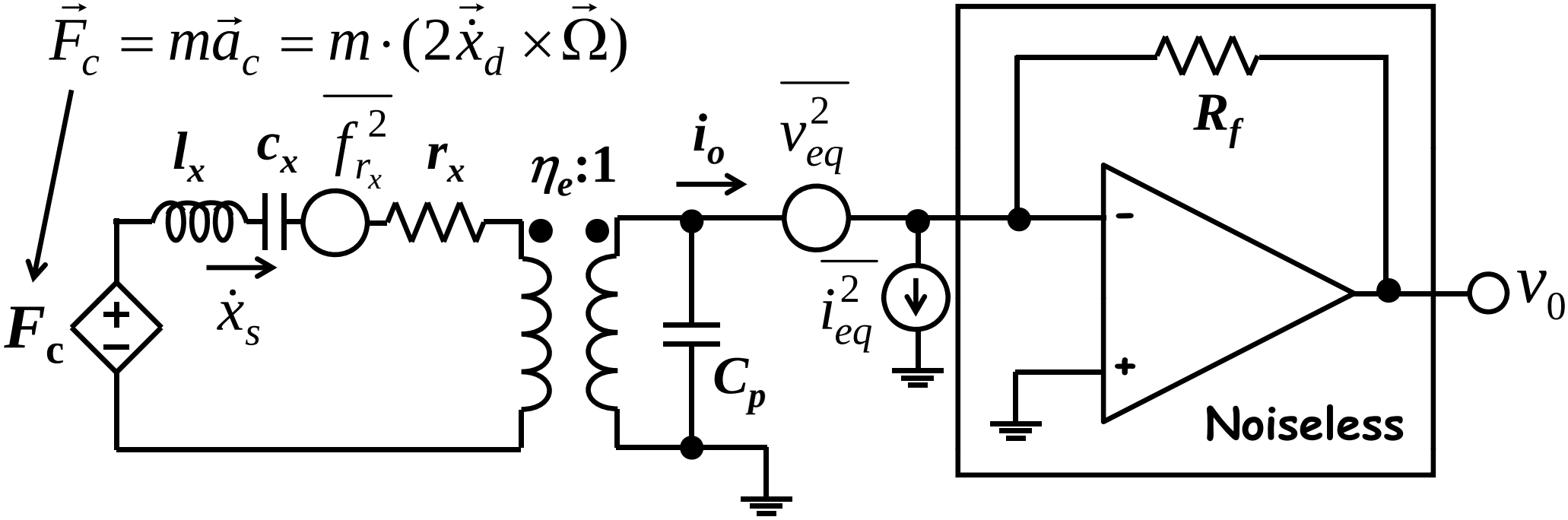
Thus:

$$\boxed{\frac{\overline{i_{eqTOT}^2}}{\Delta f} = \frac{4kT}{R_x}|\mathcal{H}(j\omega_d)|^2 + \frac{4kT}{R_f} + \frac{\overline{i_{ia}^2}}{\Delta f} + \frac{\overline{v_{ia}^2}}{\Delta f}\left(\frac{1}{R_f^2}\right)}$$

$\overline{i_{eqA}^2}$

Learn to get these from EE240.
↳ or just get them from a data sheet ...

Example: Gyro MDS Calculation (cont)



- First, find the rotation to i_o transfer function:

$$\dot{x}_s = \frac{\omega_s Q}{k_s} H_s(j\omega_d) F_s = \frac{\omega_s Q}{k_s} \cdot 2\omega_d x_d \Omega m \cdot H(j\omega_d)$$

$$\left[F_s = F_c = 2\omega_d x_d \Omega m\right]$$

$$\frac{1}{\omega_s^2}$$

$$\dot{x}_s = 2\frac{\omega_d}{\omega_s} Q x_d H(j\omega_d)\cdot\Omega$$

Example: Gyro MDS Calculation (cont)

UC Berkeley

$$i_o = \eta_e \dot{x}_s = \underbrace{2\frac{\omega_d}{\omega_s} Q x_d \eta_e \mathcal{H}(j\omega_d)}_{A \triangleq \text{scale factor}} \cdot \Omega \quad \rightarrow \quad \boxed{i_o = A\Omega \quad \text{where } A = 2\frac{\omega_d}{\omega_s} Q x_d \eta_e \mathcal{H}(j\omega_d)}$$

When $\Omega = \Omega_{min} \triangleq MDS$, $i_o = i_{eqTOT}$ ← input-referred noise current entering the sense amplifier → in $pA/\sqrt{Hz}$

$$\therefore \; i_{eqTOT} = A\Omega_{min} \rightarrow \boxed{\Omega_{min} = \frac{i_{eqTOT}}{A}\left(\frac{360^\circ s}{hr}\right)\left(\frac{180^\circ}{\pi}\right) \left[(^\circ/hr)/\sqrt{Hz}\right]}$$

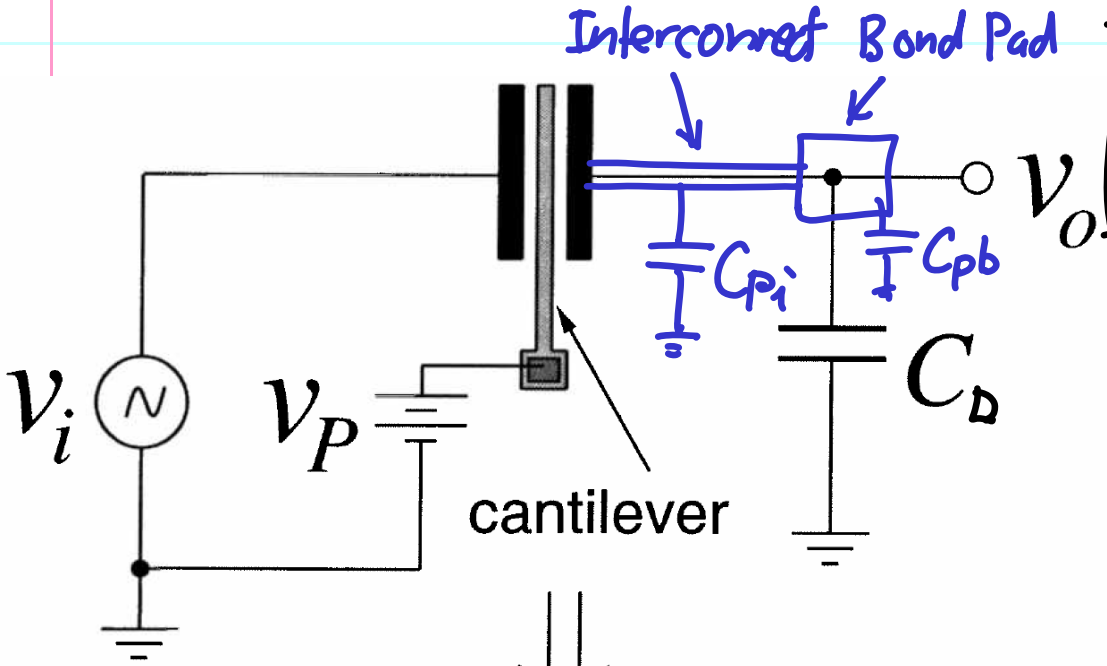
$$\boxed{\text{Angle Random Walk} = ARW = \frac{1}{60}\Omega_{min} \left[^\circ/\sqrt{hr}\right]}$$

↳ Easier to determine directional error as a function of elapsed time.

Sensing Circuits (cont)

Problems With Pure-C Position Sensing

- To sense position (i.e., displacement), use a capacitive load



$$\frac{V_o}{V_i}(s) = \frac{C_x/C_D}{1+C_x/C_D} \cdot \frac{1}{s} \cdot H(s, \omega_o', Q') \cdot \omega_o' Q'$$

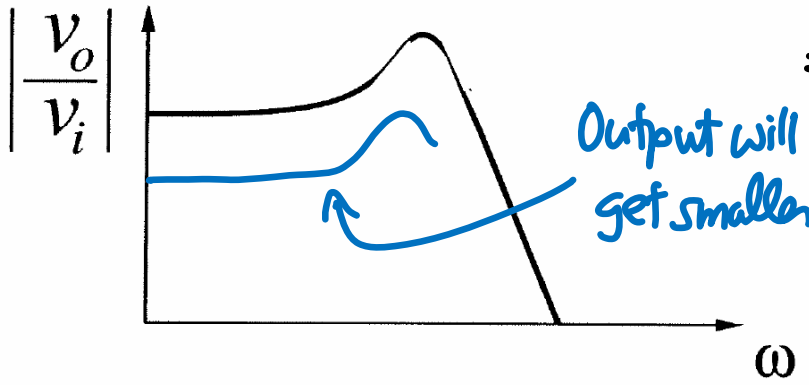
Integration yields displacement.

To maximize gain, minimize f_L.

⇒ Problem: parasitic capacitance

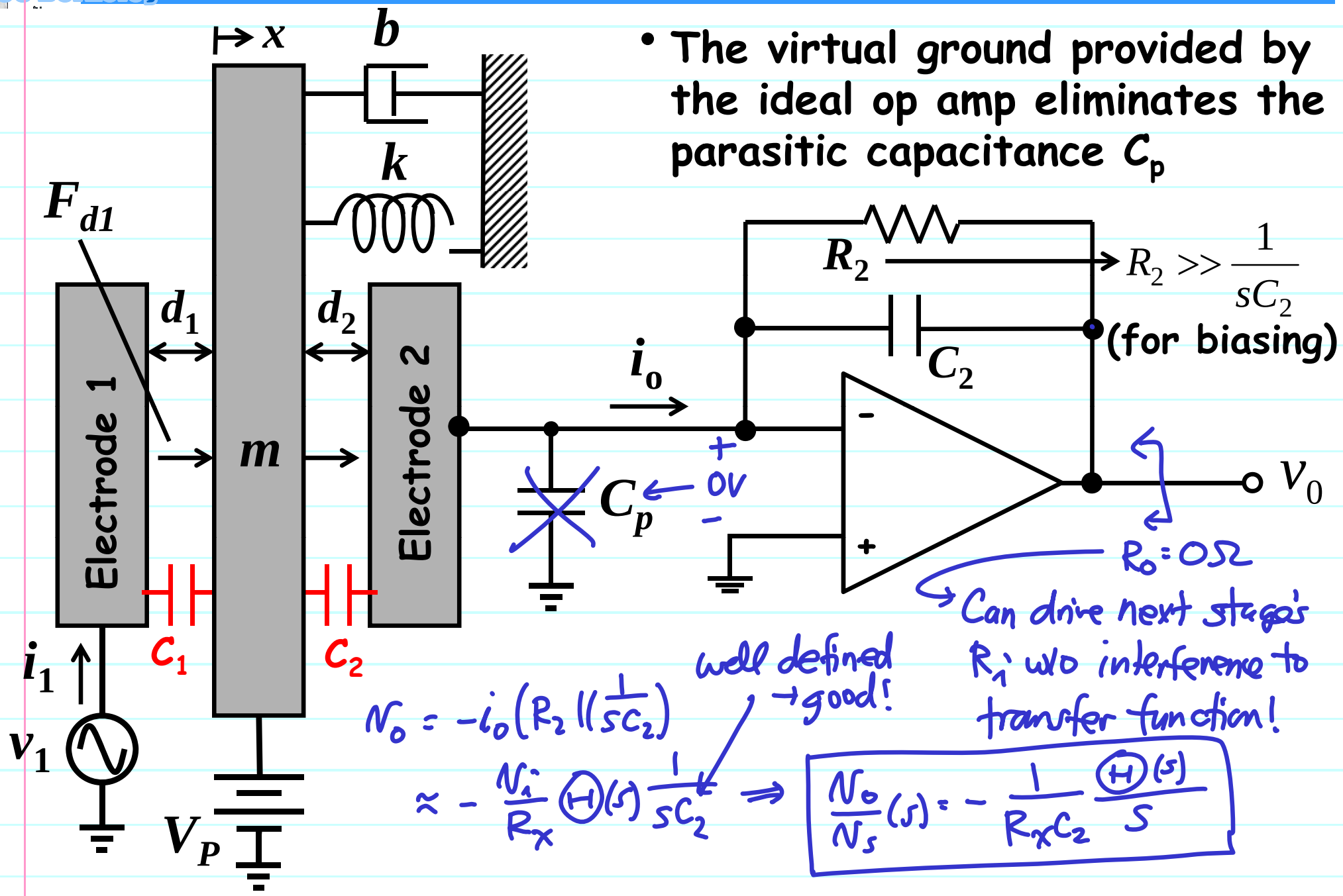
$$C_D \rightarrow C_D + C_{pi} + C_{pb}$$

⇒ DC Gain: $\dfrac{C_x/(C_D+C_{pi}+C_{pb})}{1+C_x/(C_D+C_{pi}+C_{pb})}$



Remedy: Suppress C_p via use of op amps.

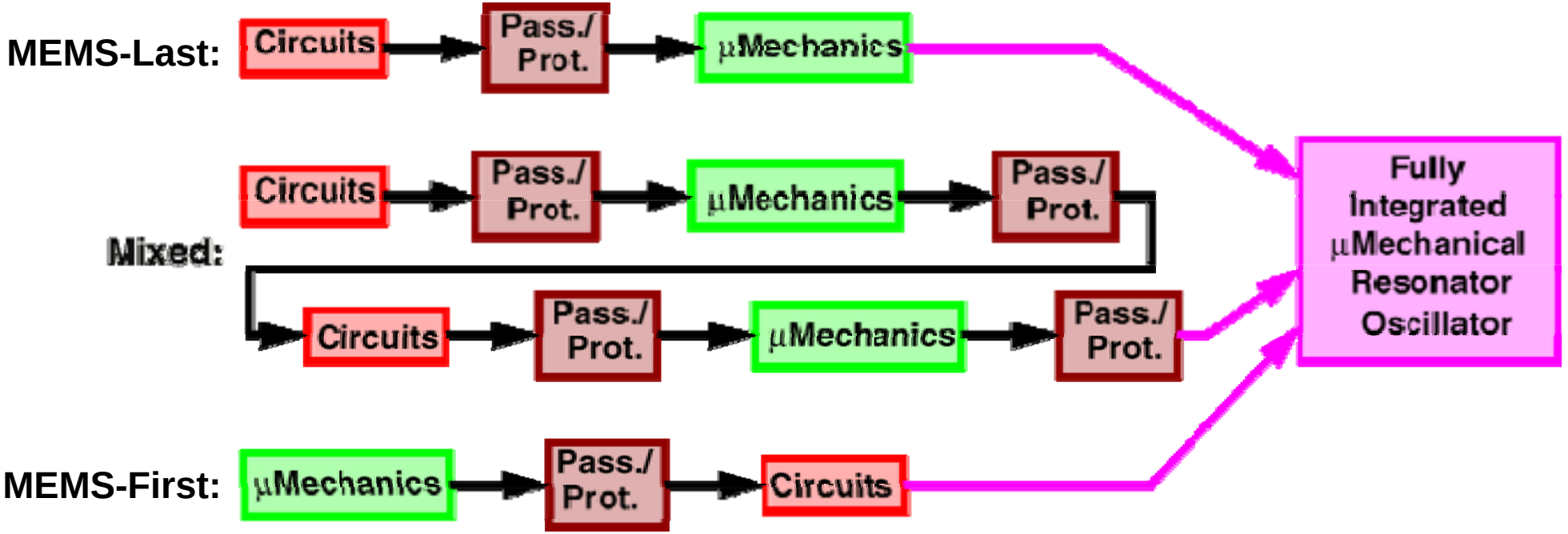
The Op Amp Integrator Advantage



- The virtual ground provided by the ideal op amp eliminates the parasitic capacitance C_p

Integration of MEMS and Transistors

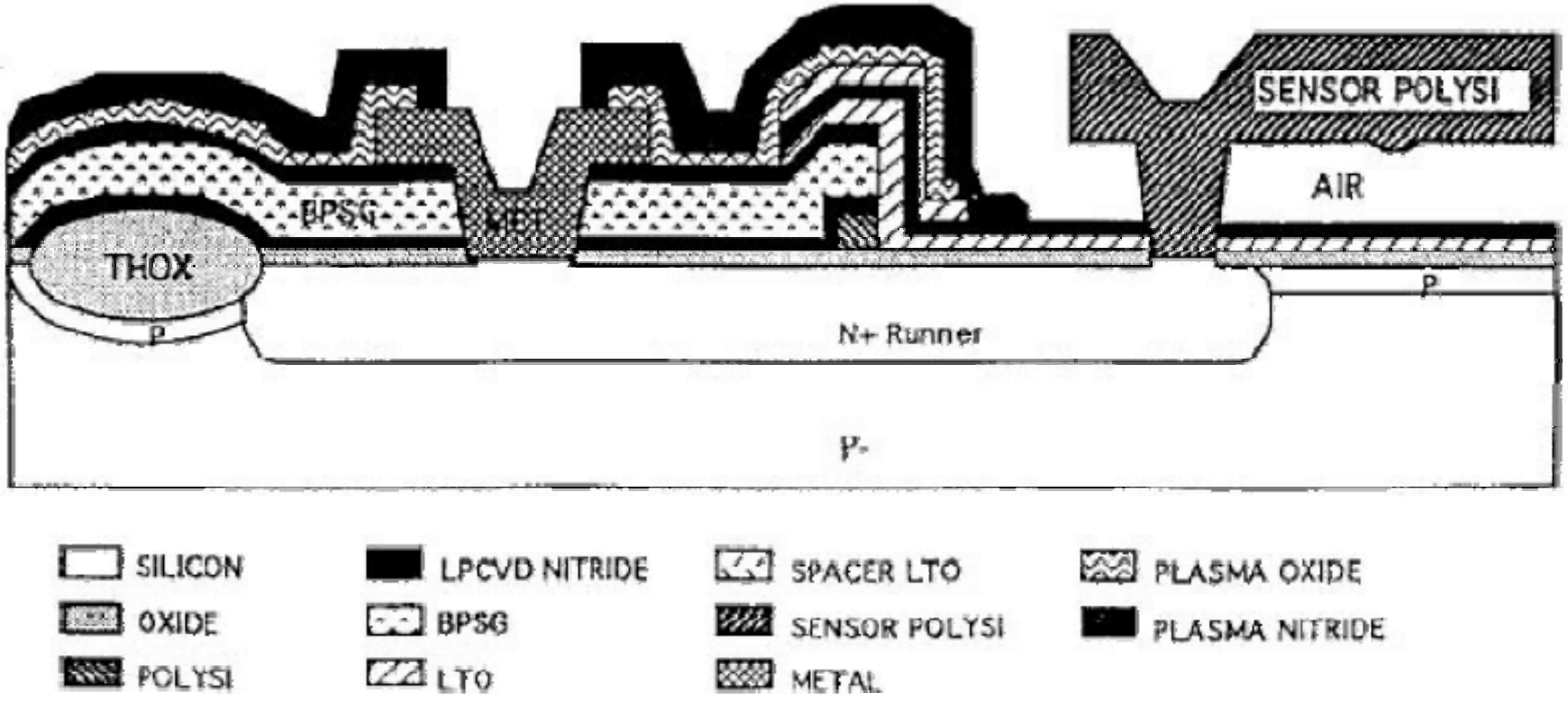
Merged MEMS/Transistor Technologies (Process Philosophy)



- Mixed:
  - problem: multiple passivation/protection steps ⇒ large number of masks required
  - problem: custom process for each product
- MEMS-first or MEMS-last:
  - adv.: modularity ⇒ flexibility ⇒ less development time
  - adv.: low pass./protection complexity ⇒ fewer masks

Analog Devices BiMEMS Process

- Interleaved MEMS and 4 μm BiMOS processes (28 masks)
- Diffused n+ runners used to interconnect MEMS & CMOS
- Relatively deep junctions allow for MEMS poly stress anneal
- Used to manufacture the ADXL-50 accelerometer and Analog Devices family of accelerometers

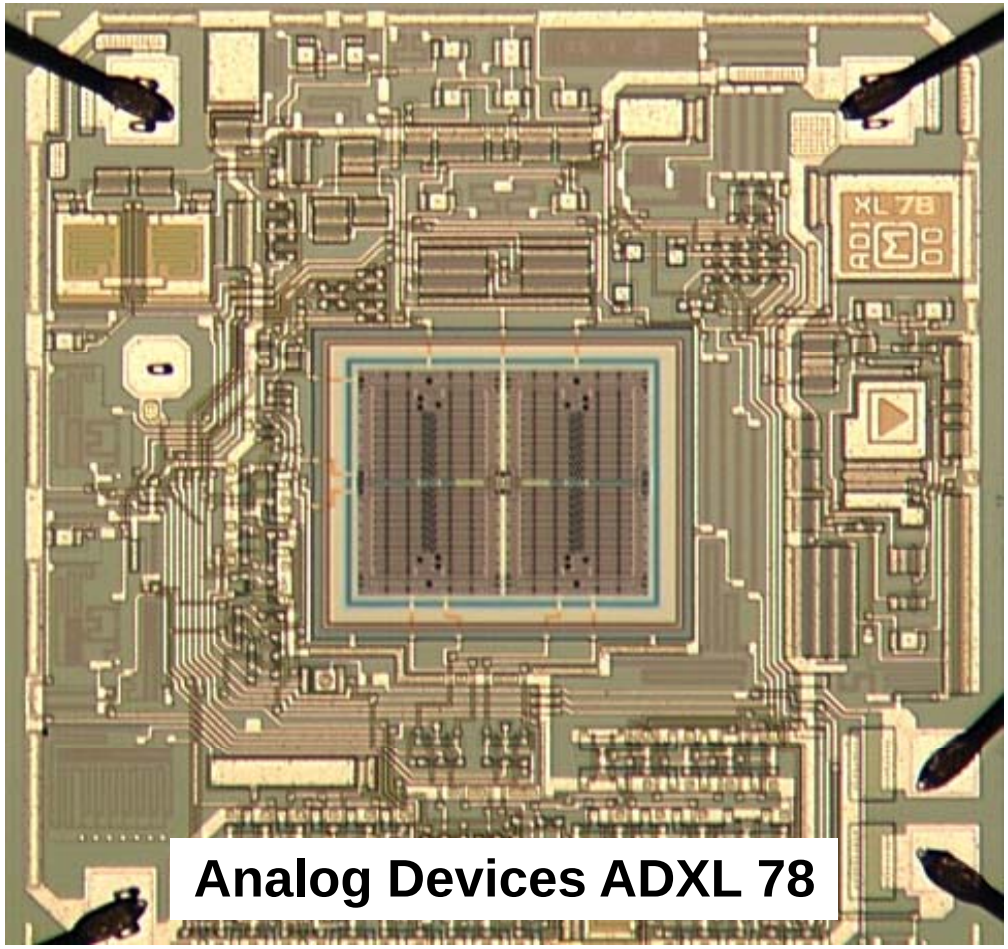


Analog Devices BiMEMS Process (cont)

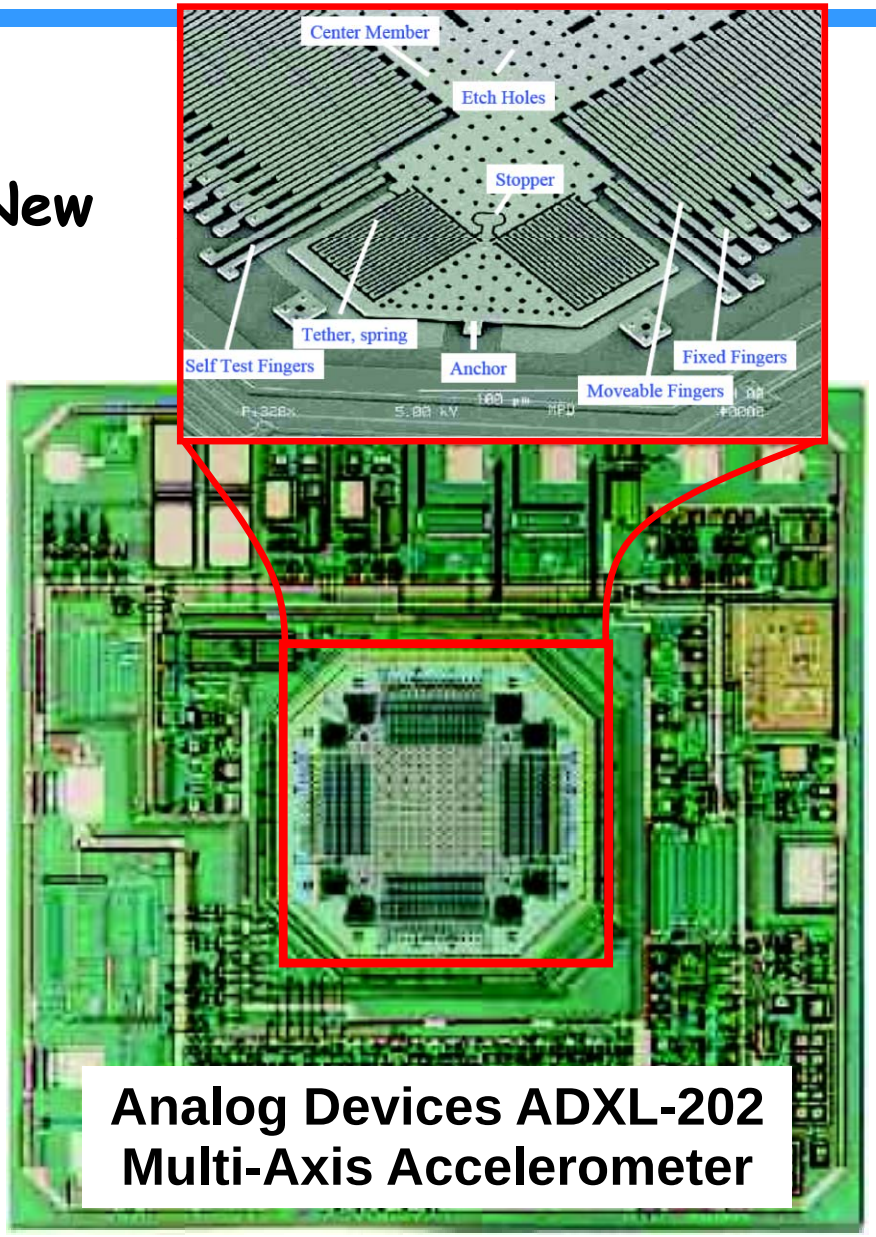
UC Berkeley

- **Examples**:

Old ⟶ New



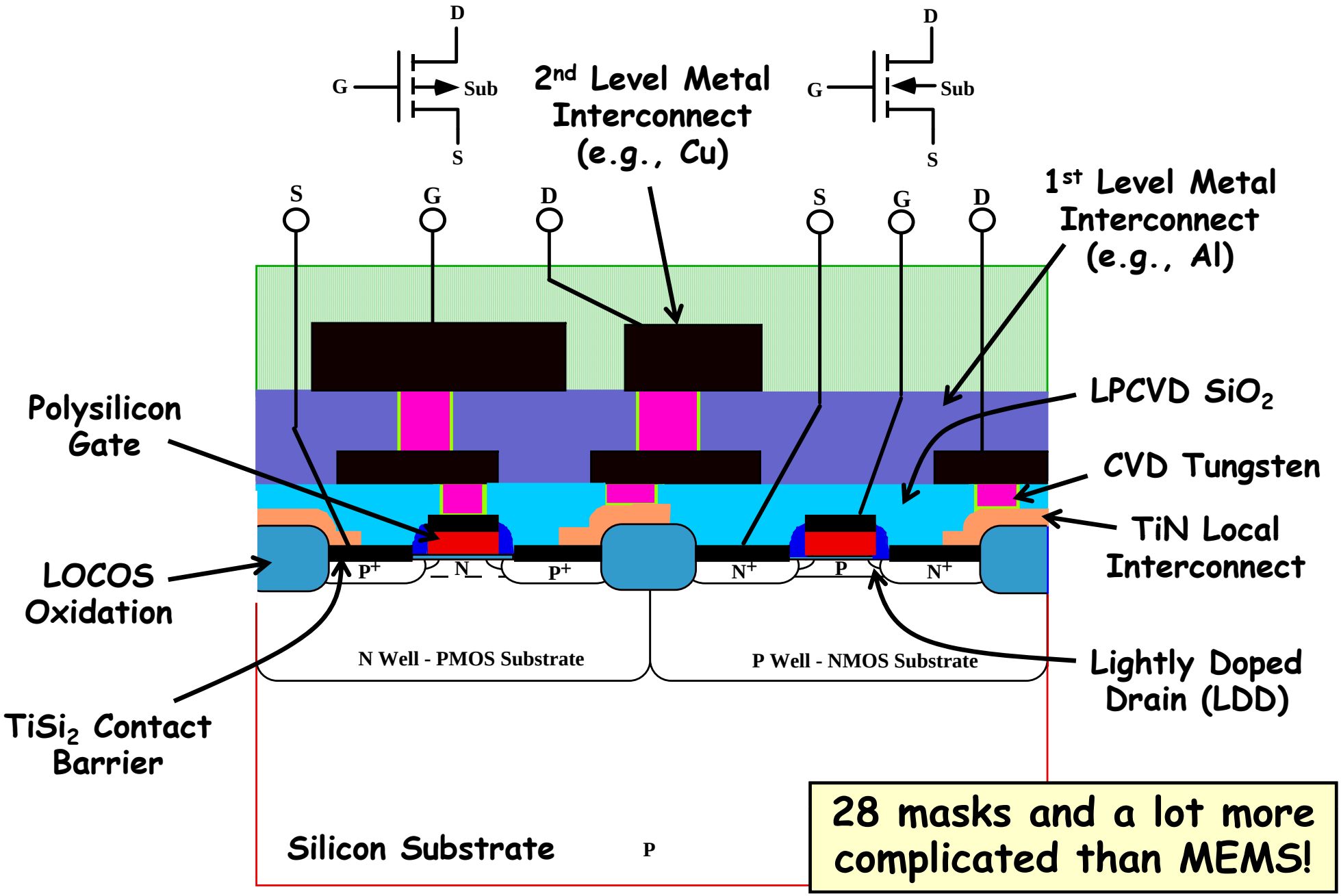
Analog Devices ADXL 78



Analog Devices ADXL-202
Multi-Axis Accelerometer

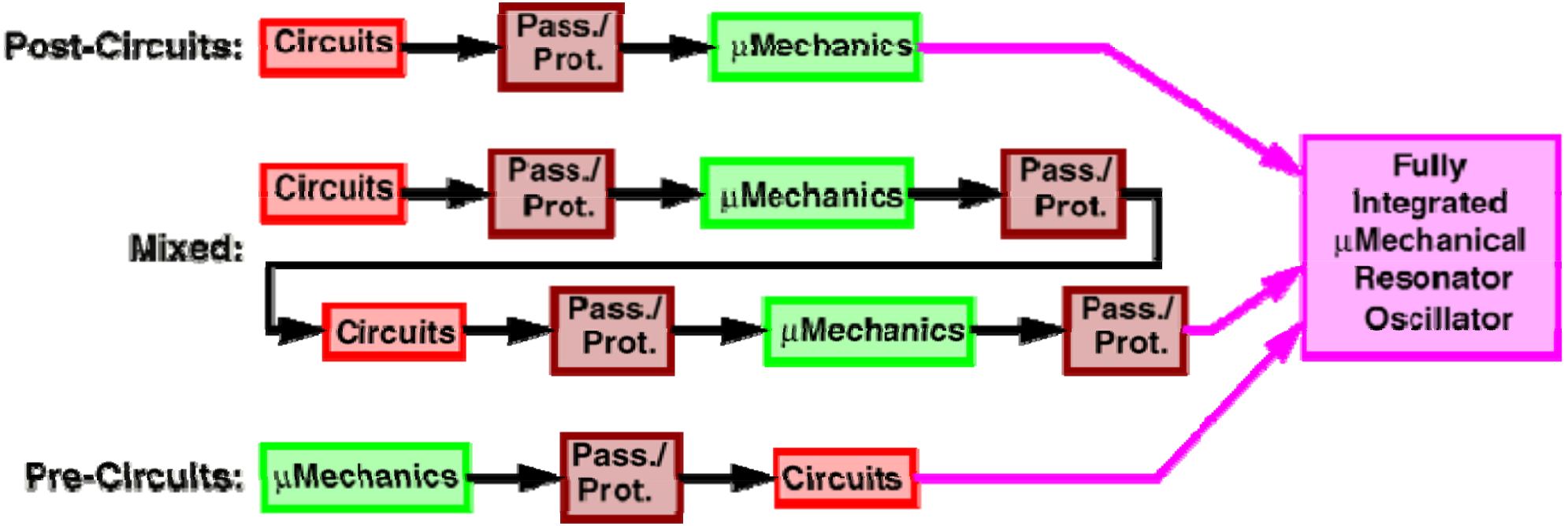
- Can you list the advances in the process from old to new?

250 nm CMOS Cross-Section



28 masks and a lot more complicated than MEMS!

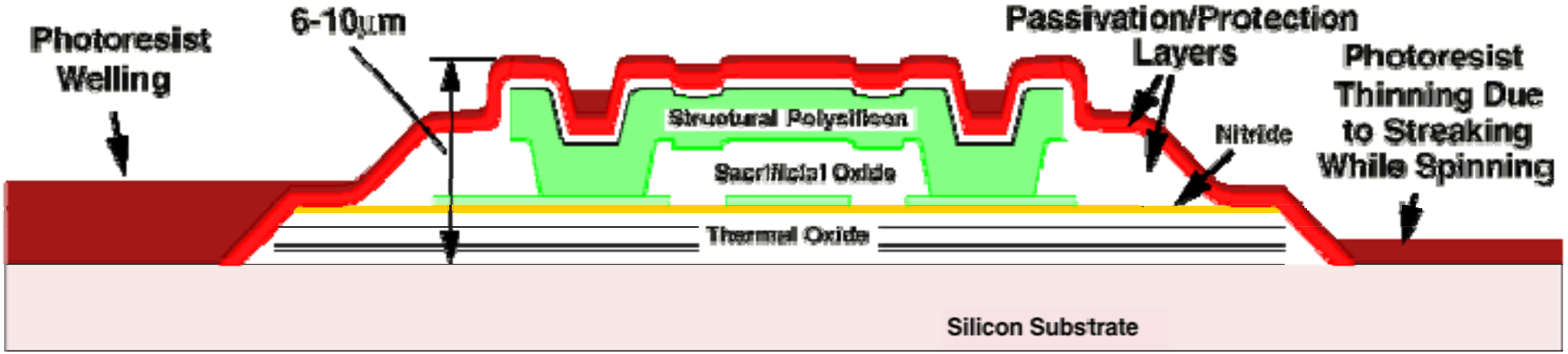
Merged MEMS/Transistor Technologies (Process Philosophy)



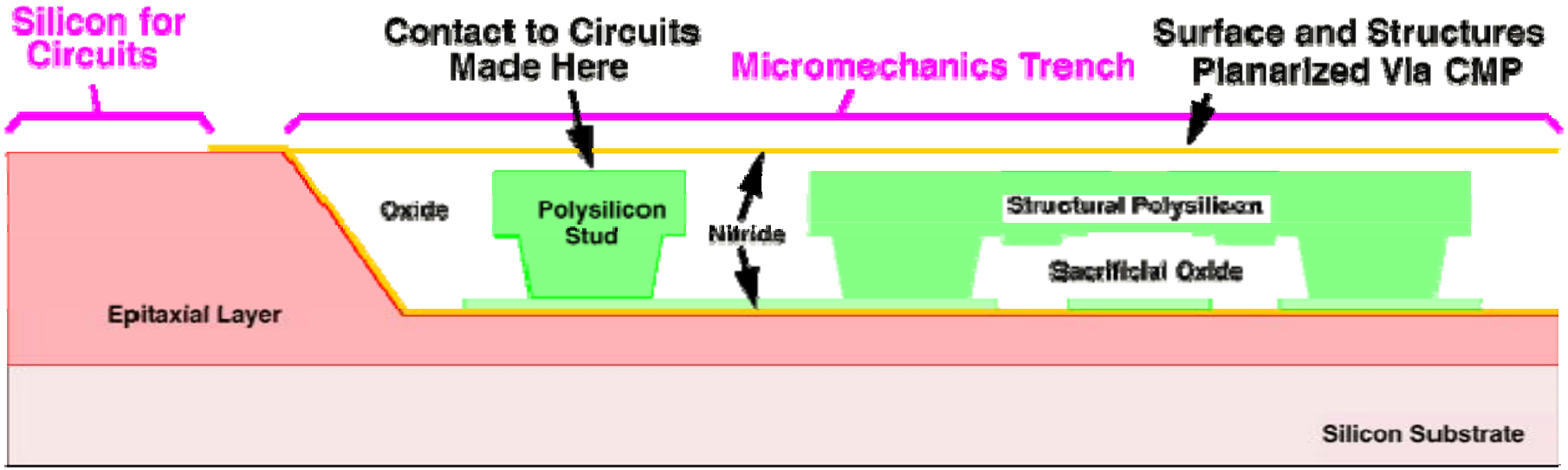
- Mixed:
  - problem: multiple passivation/protection steps ⇒ large number of masks required
  - problem: custom process for each product
- MEMS-first or MEMS-last:
  - adv.: modularity ⇒ flexibility ⇒ less development time
  - adv.: low pass./protection complexity ⇒ fewer masks

MEMS-First Integration

- Problem: μstructural topography interferes with lithography
  - ↳ difficult to apply photoresist for submicron circuits



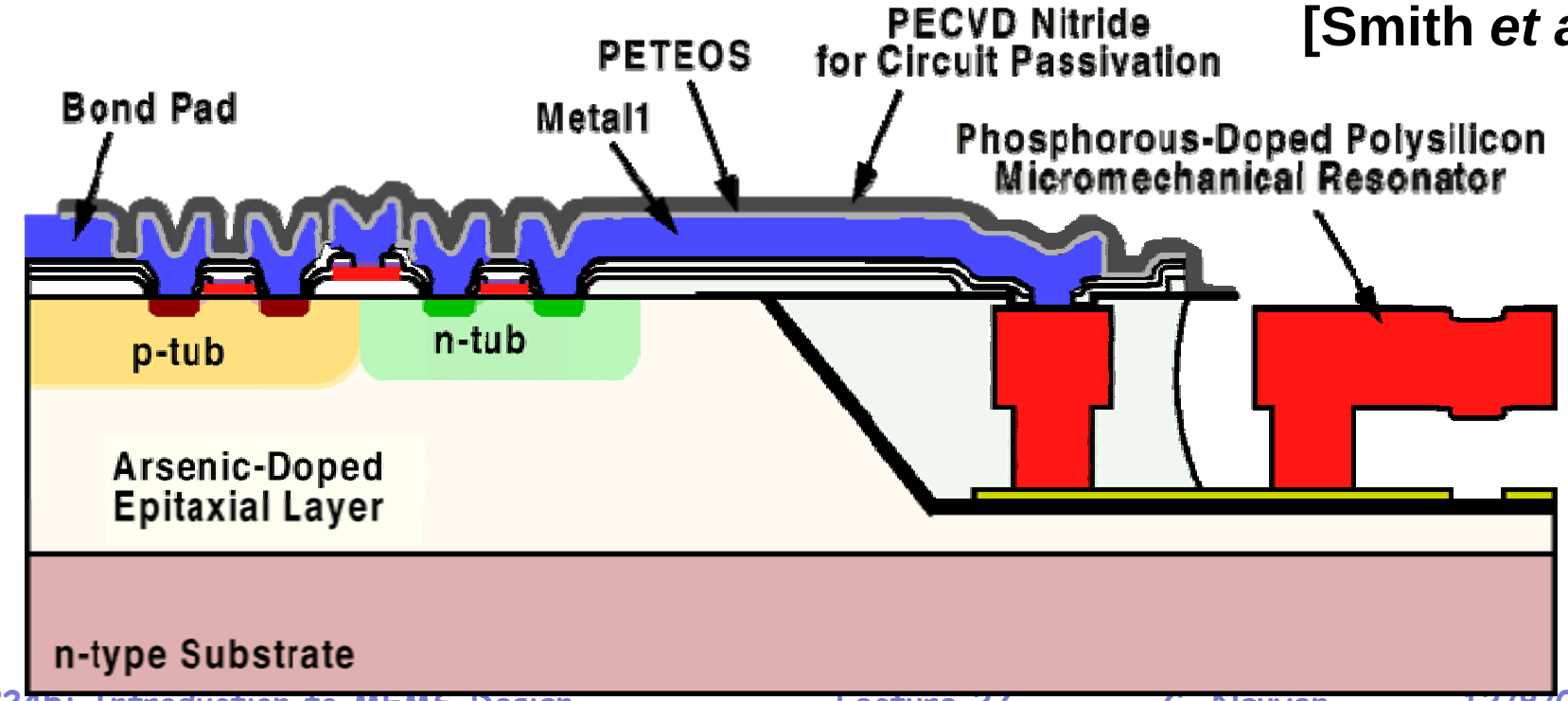
- Soln.: build μmechanics in a trench, then planarize before circuit processing [Smith *et al*, IEDM'95]



MEMS-First Ex: Sandia's iMEMS

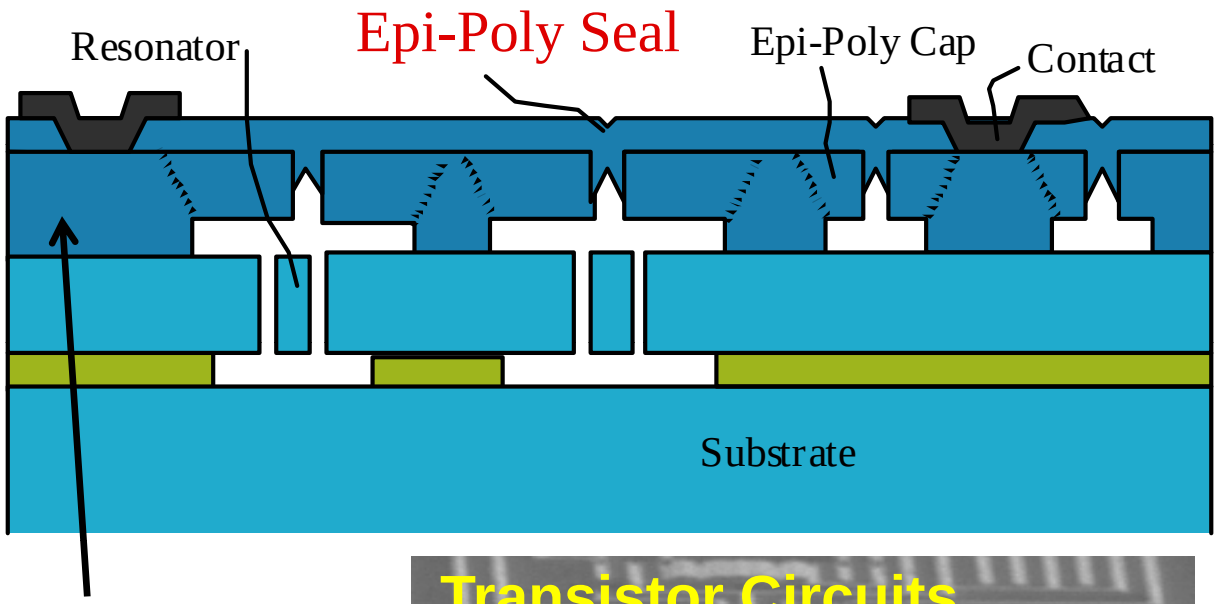
- Used to demonstrate functional fully integrated oscillators
- Issues:
  - lithography and etching may be difficult in trench → may limit dimensions (not good for RF MEMS)
  - μmechanical material must stand up to IC temperatures (>1000°C) → problem for some metal materials
  - might be contamination issues for foundry IC's

[Smith *et al*, IEDM'95]

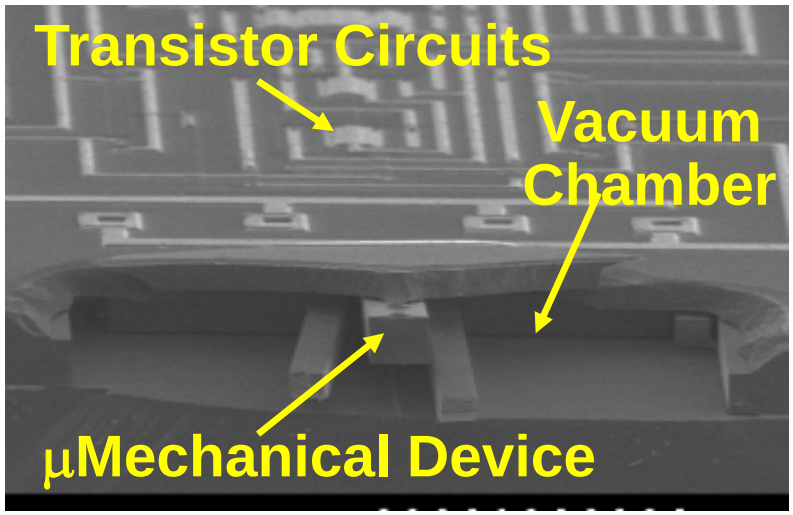


Bosch/Stanford MEMS-First Process

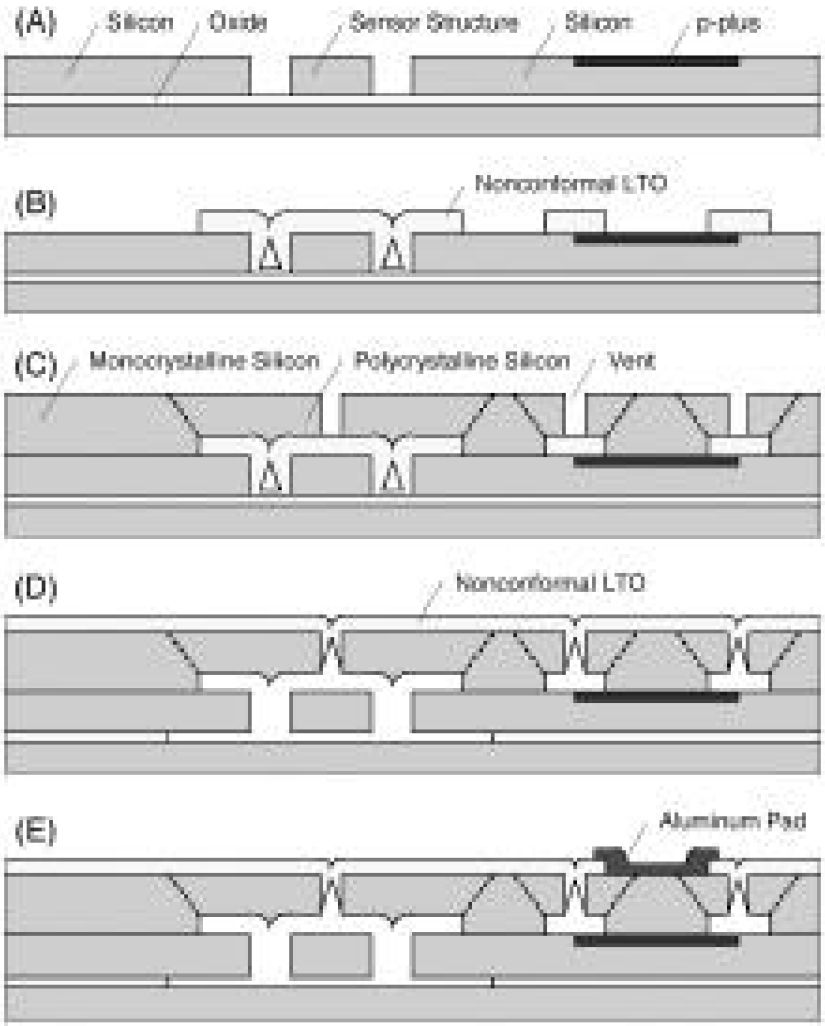
- Single-crystal silicon microstructures sealed under epi-poly encapsulation covers
- Many masking steps needed, but very stable structures



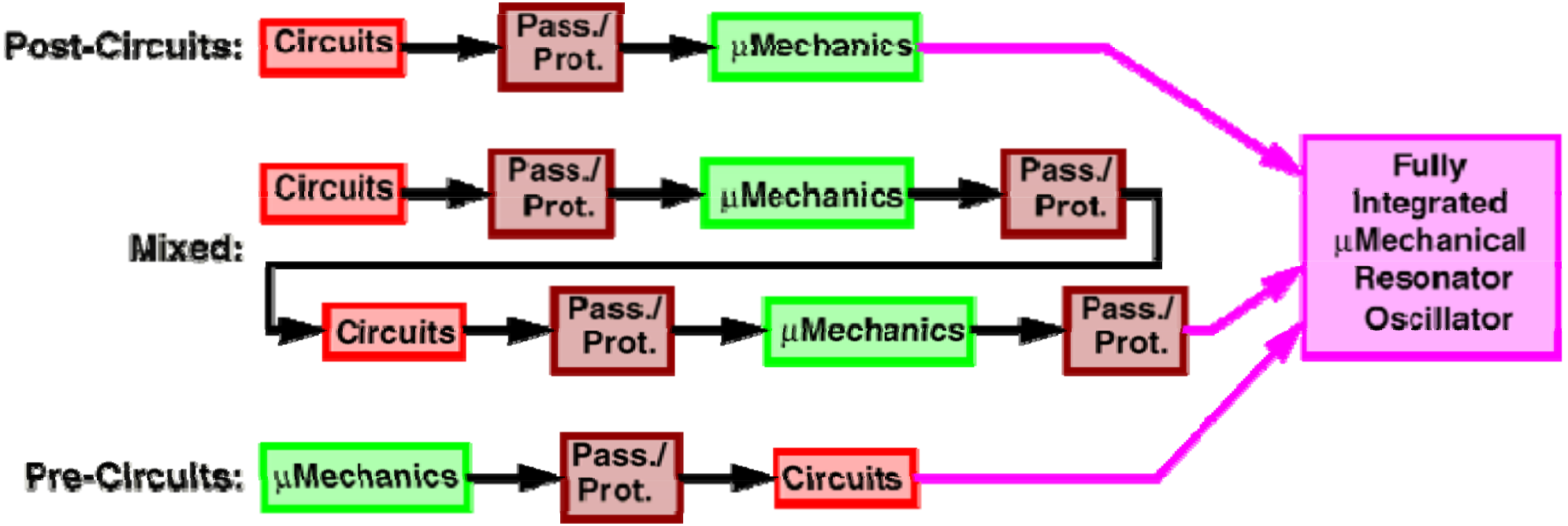
Epi-silicon for CMOS



[Kim, Kenny Trans'05]



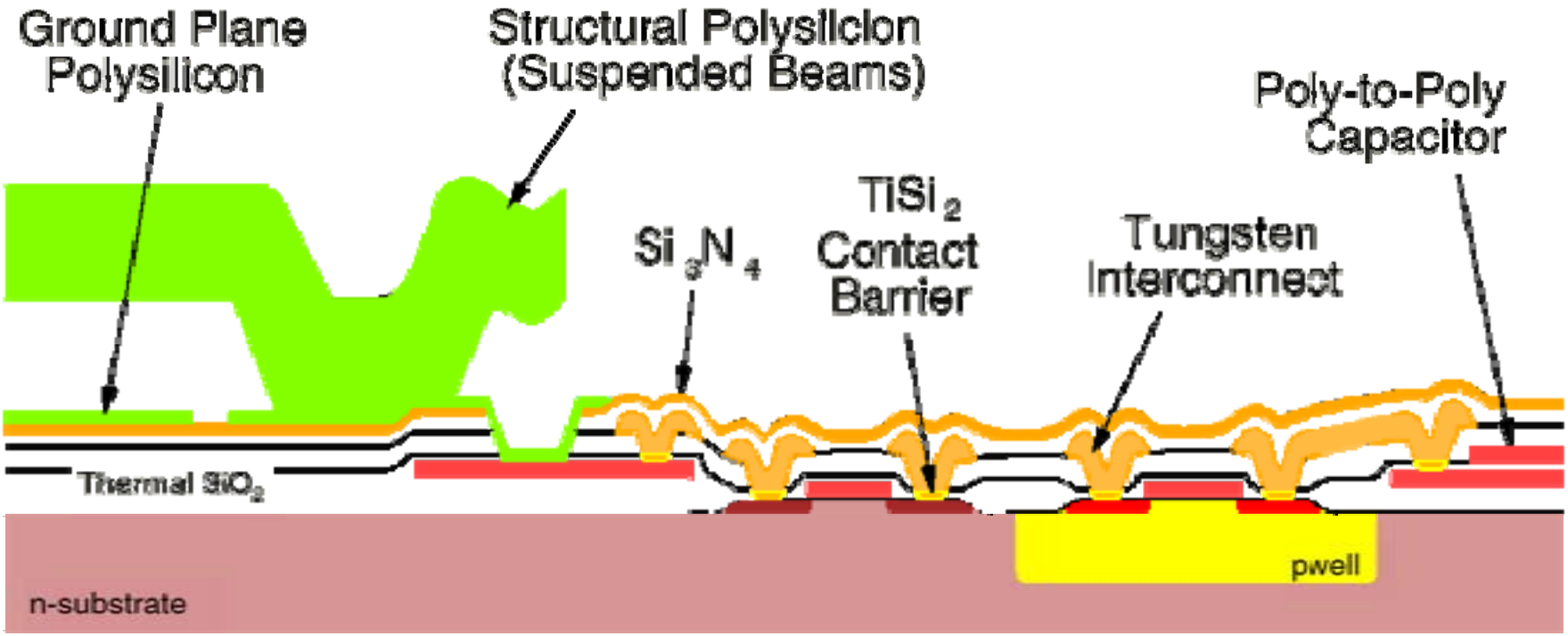
Merged MEMS/Transistor Technologies (Process Philosophy)



- Mixed:
  - problem: multiple passivation/protection steps ⇒ large number of masks required
  - problem: custom process for each product
- MEMS-first or MEMS-last:
  - adv.: modularity ⇒ flexibility ⇒ less development time
  - adv.: low pass./protection complexity ⇒ fewer masks

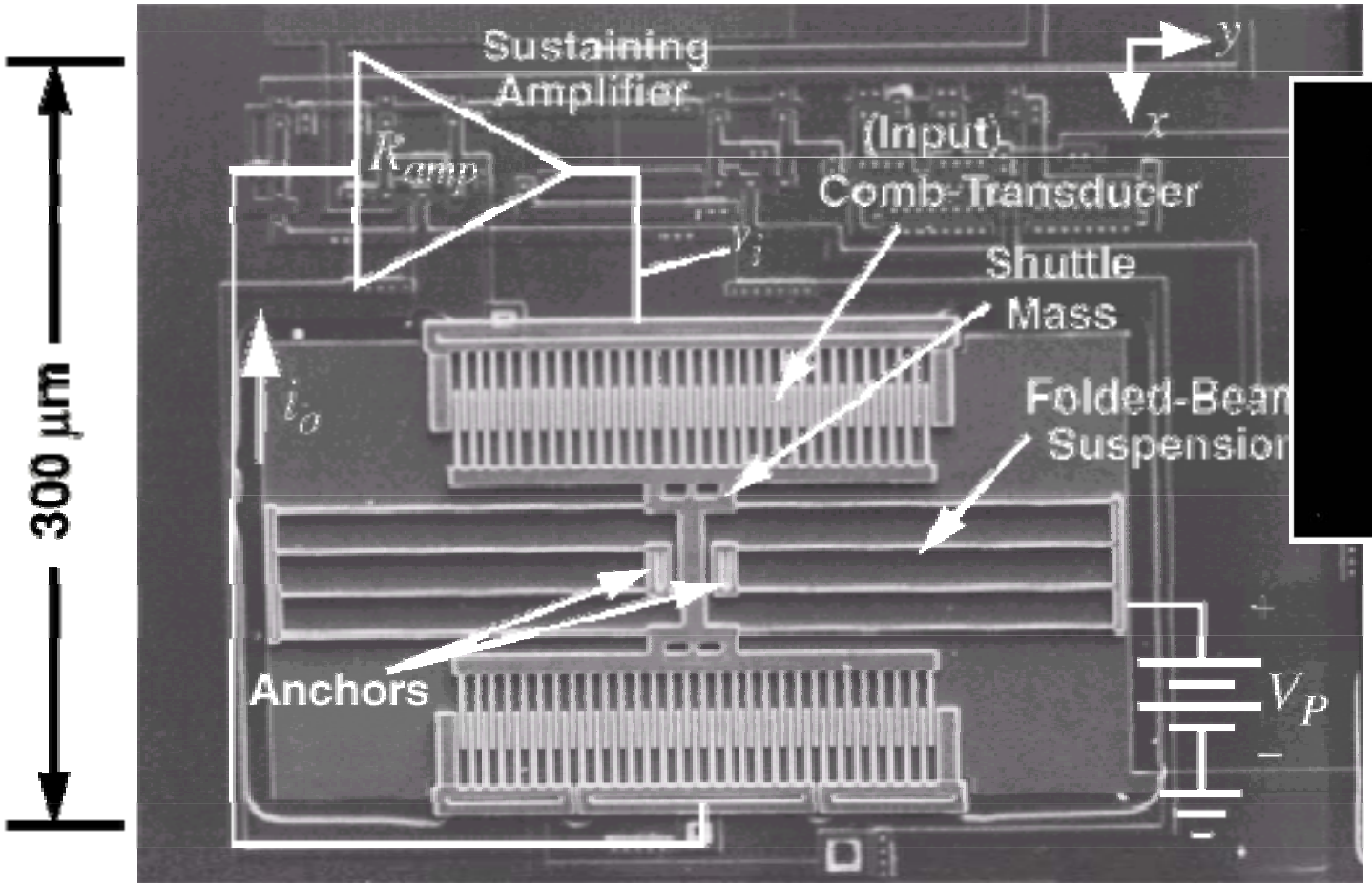
Berkeley Polysilicon MICS Process

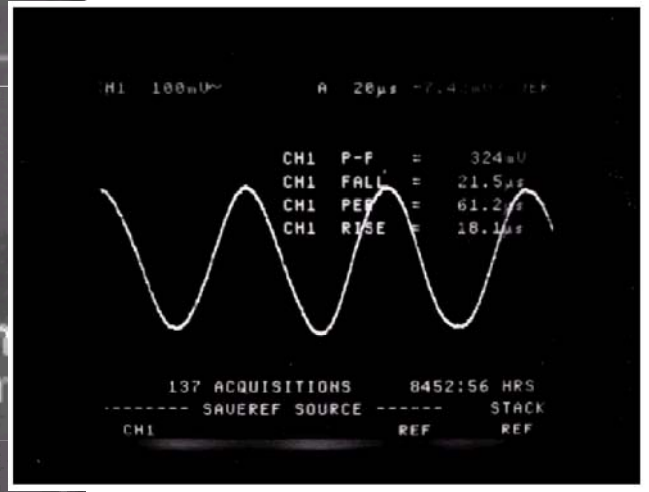
- Uses surface-micromachinedpolysilicon microstructures with silicon nitride layer between transistors & MEMS
  - Polysilicon dep. T~600°C; nitride dep. T~835°C
  - 1100°C RTA stress anneal for 1 min.
  - metal and junctions must withstand temperatures ~835°C
  - tungsten metallization used with $TiSi_2$ contact barriers
  - *in situ* doped structural polySi; rapid thermal annealing



Single-Chip Ckt/MEMS Integration

- Completely monolithic, low phase noise, high-Q oscillator (effectively, an integrated crystal oscillator)





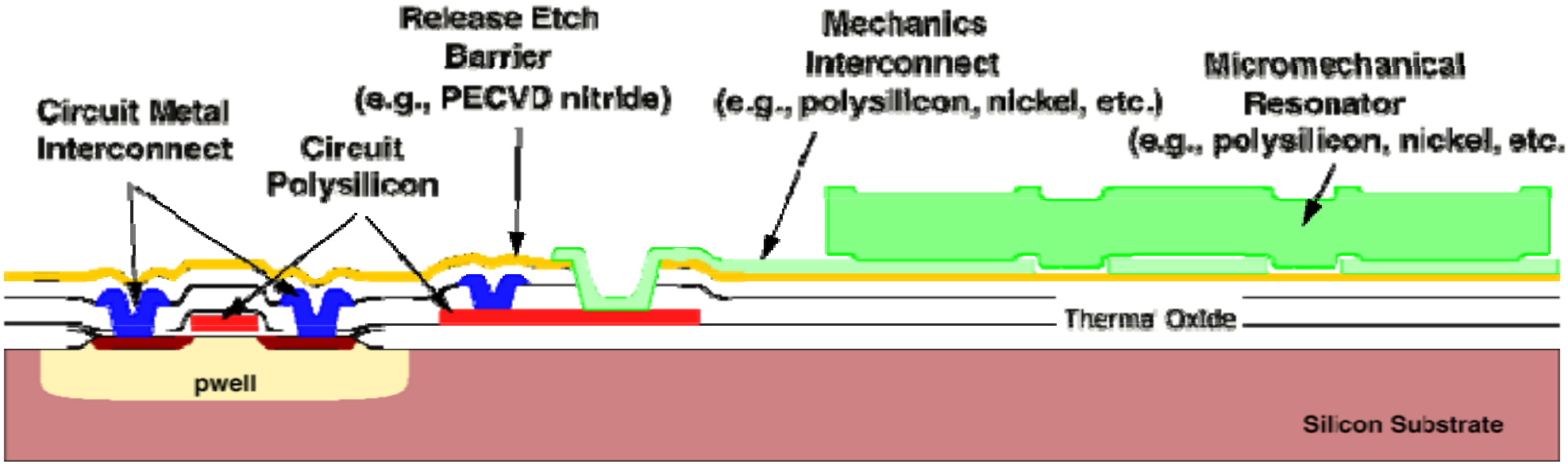
Oscilloscope Output Waveform

[Nguyen, Howe 1993]

- To allow the use of >600°C processing temperatures, tungsten (instead of aluminum) is used for metallization

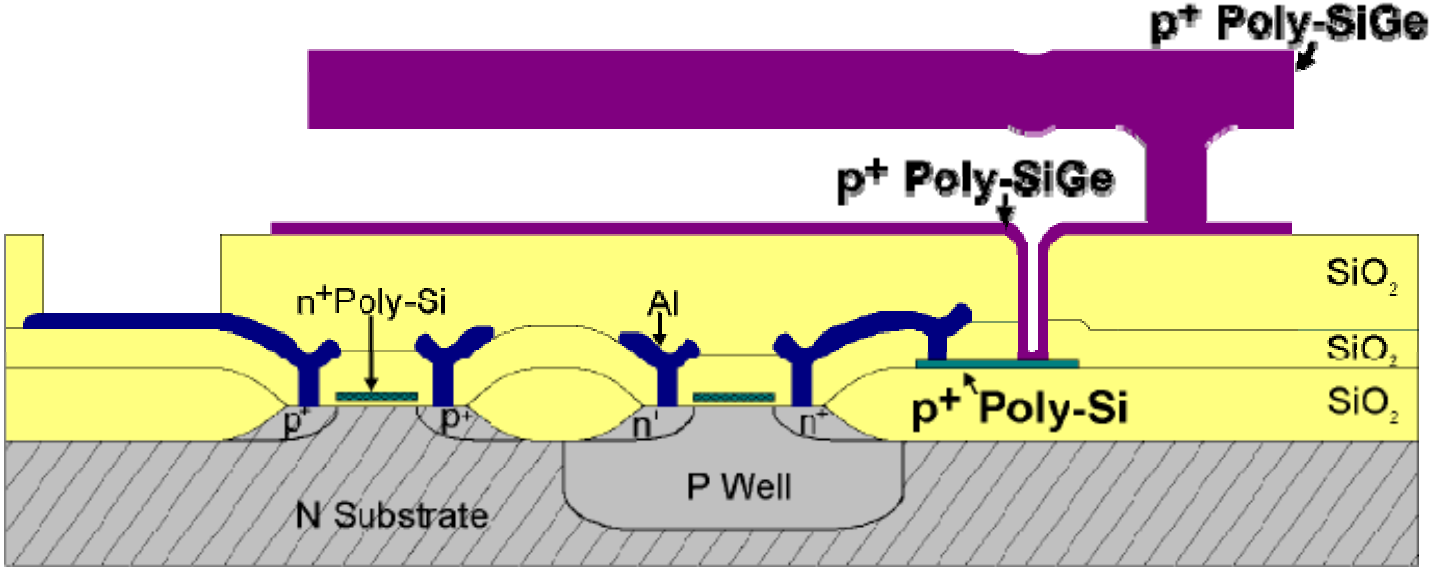
Usable MEMS-Last Integration

- Problem: tungsten is not an accepted primary interconnect metal
- Challenge: retain conventional metallization
  - minimize post-CMOS processing temperatures
  - explore alternative structural materials (e.g., plated nickel, SiGe [Franke, Howe *et al*, MEMS'99])
  - Limited set of usable structural materials → not the best situation, but workable

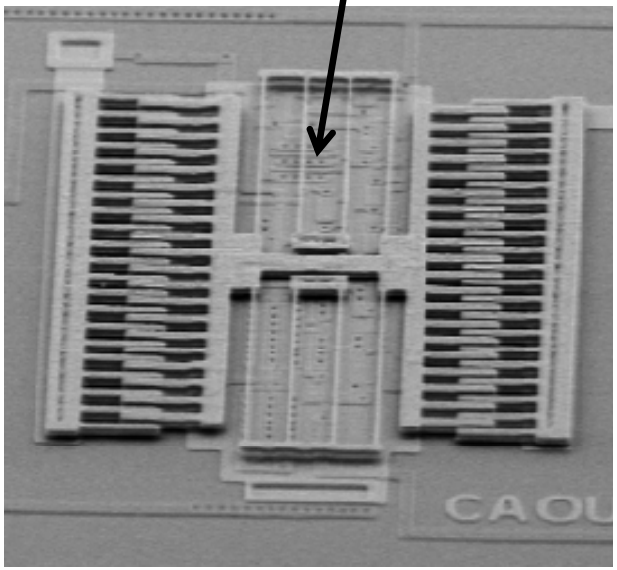


UCB Poly-SiGe MICS Process

- 2 μm standard CMOS process w/ Al metallization
- P-type poly-$Si_{0.35}Ge_{0.65}$ structural material; poly-Ge sacrificial material
- Process:
  - Passivate CMOS w/ LTO @ 400°C
  - Open vias to interconnect runners
  - Deposit & pattern ground plane
  - RTA anneal to lower resistivity (550°C, 30s)



Transistor Circuits



Wrap Up