

# EE C245 - ME C218

## Introduction to MEMS Design


### Fall 2012

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**Lecture Module 6: Bulk Micromachining**


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## Lecture Outline





- Reading: Senturia Chpt. 3, Jaeger Chpt. 11, Handouts: "Bulk Micromachining of Silicon"
- Lecture Topics:
  - ↗ Bulk Micromachining
  - ↗ Anisotropic Etching of Silicon
  - ↗ Boron-Doped Etch Stop
  - ↗ Electrochemical Etch Stop
  - ↗ Isotropic Etching of Silicon
  - ↗ Deep Reactive Ion Etching (DRIE)
  - ↗ Wafer Bonding

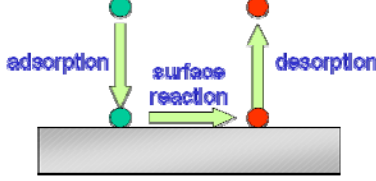
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## Bulk Micromachining


- Basically, etching the substrate (usually silicon) to achieve microstructures
- Etching modes:
  - ↗ Isotropic vs. anisotropic
  - ↗ Reaction-limited
    - Etch rate dep. on temp.
  - ↗ Diffusion-limited
    - Etch rate dep. on mixing
    - Also dependent on layout & geometry, i.e., on loading
- Choose etch mode based on
  - ↗ Desired shape
  - ↗ Etch depth and uniformity
  - ↗ Surface roughness (e.g., sidewall roughness after etching)
  - ↗ Process compatibility (w/ existing layers)
  - ↗ Safety, cost, availability, environmental impact

	Wet etch	Plasma (dry) etch
Isotropic		
Anisotropic		



slowest step controls rate of reaction


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## Mechanical Properties of Silicon

- Crystalline silicon is a hard and brittle material that deforms elastically until it reaches its yield strength, at which point it breaks.
  - ↗ Tensile yield strength = 7 GPa (~1500 lb suspended from 1 mm<sup>2</sup>)
  - ↗ Young's Modulus near that of stainless steel
  - ↗ {100} = 130 GPa; {110} = 169 GPa; {111} = 188 GPa
  - ↗ Mechanical properties uniform, no intrinsic stress
  - ↗ Mechanical integrity up to 500°C
  - ↗ Good thermal conductor
  - ↗ Low thermal expansion coefficient
  - ↗ High piezoresistivity

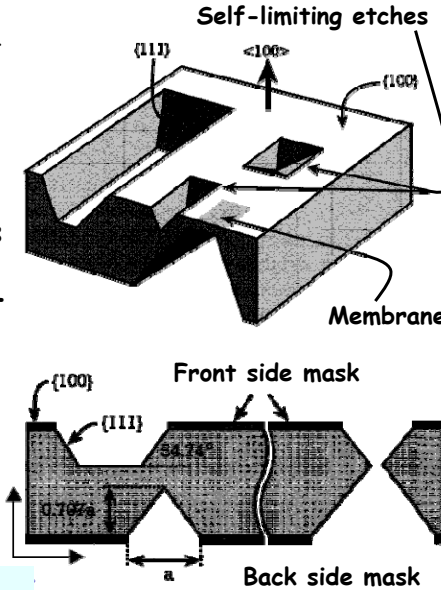
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## Anisotropic Etching of Silicon

- Etching of Si w/ KOH
 
$$\text{Si} + 2\text{OH}^- \rightarrow \text{Si}(\text{OH})_2^{2+} + 4e^-$$

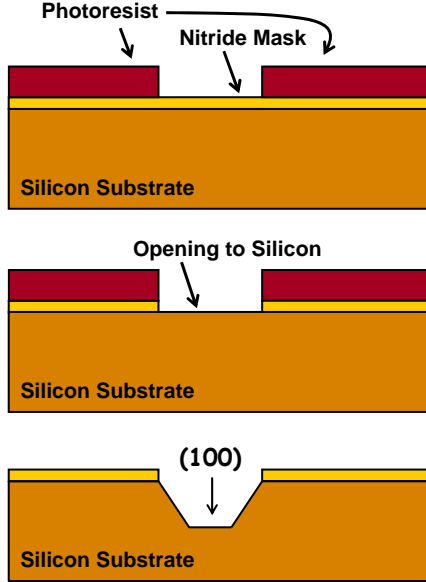
$$4\text{H}_2\text{O} + 4e^- \rightarrow 4(\text{OH})^- + 2\text{H}_2$$
- Crystal orientation dependent etch rates
  - $\{110\}:\{100\}:\{111\}=600:400:1$
  - $\{100\}$  and  $\{110\}$  have 2 bonds below the surface & 2 dangling bonds that can react
  - $\{111\}$  plane has three of its bonds below the surface & only one dangling bond to react  $\rightarrow$  much slower E.R.
  - $\{111\}$  forms protective oxide
  - $\{111\}$  smoother than other crystal planes  $\rightarrow$  good for optical MEMS (mirrors)



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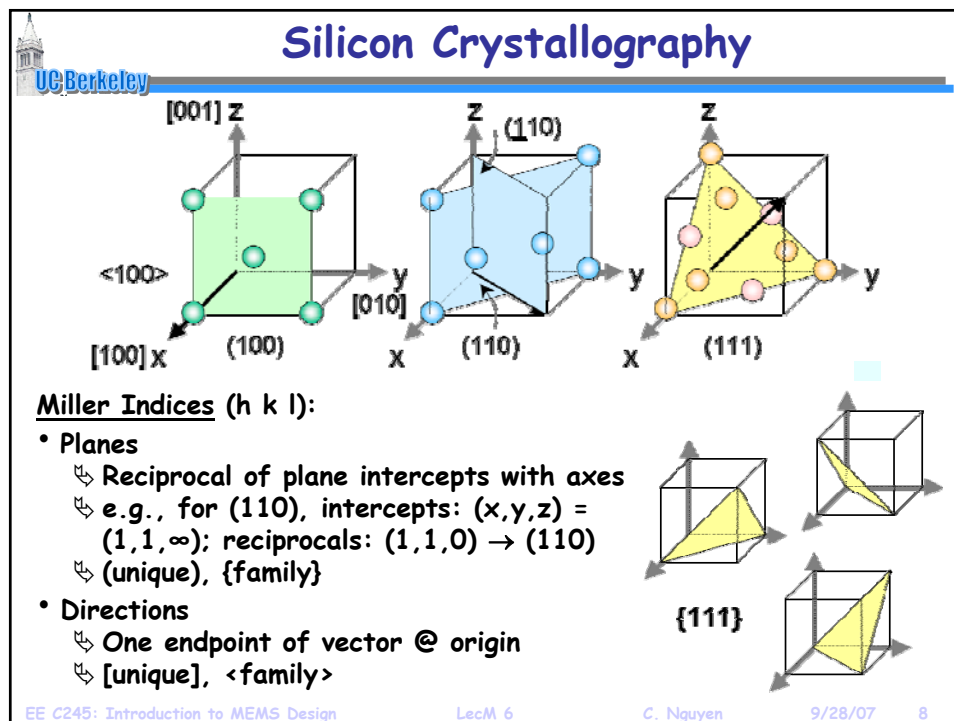
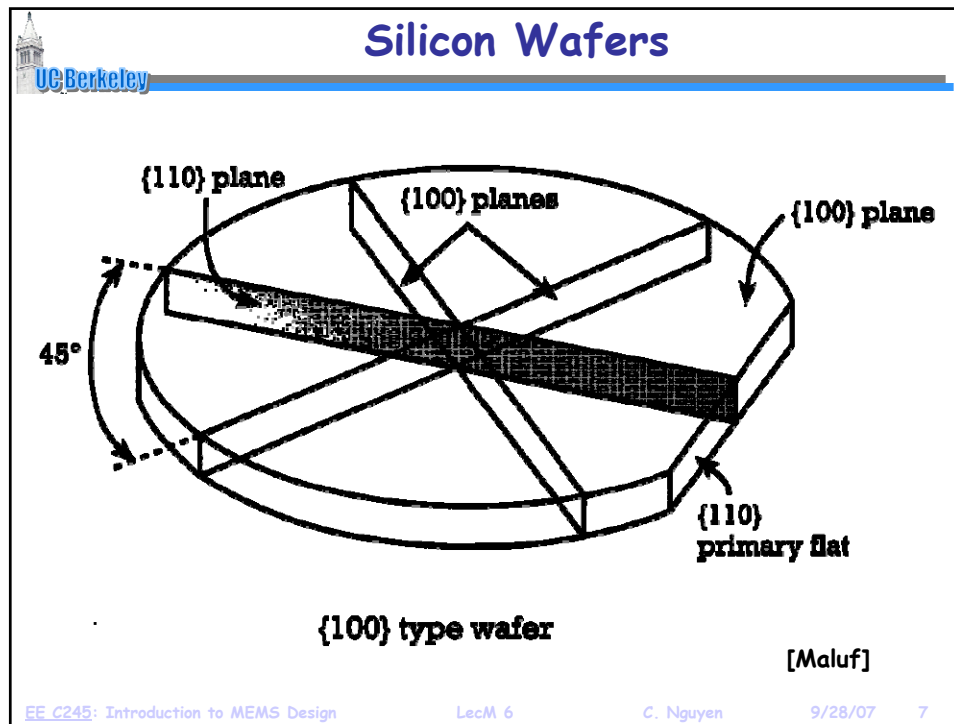


## Anisotropic Etching of Silicon

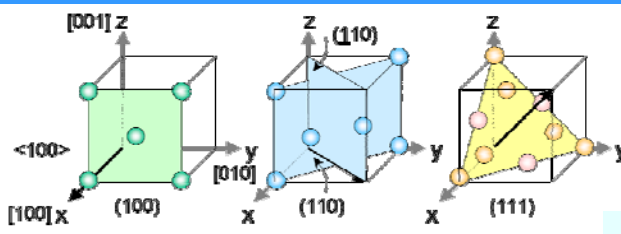


- Deposit nitride:
  - Target = 100nm
  - 22 min. LPCVD @800°C
- Lithography to define areas of silicon to be etched
- Etch/pattern nitride mask
  - RIE using  $\text{SF}_6$
  - Remove PR in PRS2000
- Etch the silicon
  - Use 1:2 KOH:H<sub>2</sub>O (wt.), stirred bath @ 80°C
  - Etch Rates:
    - (100) Si  $\rightarrow$  1.4  $\mu\text{m}/\text{min}$
    - $\text{Si}_3\text{N}_4 \rightarrow \sim 0 \text{ nm}/\text{min}$
    - $\text{SiO}_2 \rightarrow 1\text{-}10 \text{ nm}/\text{min}$
    - Photoresist, Al  $\rightarrow$  fast
- Micromasking by H<sub>2</sub> bubbles leads to roughness
  - Stir well to displace bubbles
  - Can also use oxidizer for (111) surfaces
  - Or surfactant additives to suppress bubble formation

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**Determining Angles Between Planes**




- The angle between vectors  $[abc]$  and  $[xyz]$  is given by:
$$ax + by + cz = |(a, b, c)| \cdot |(x, y, z)| \cdot \cos \theta$$

$$\theta_{(a,b,c),(x,y,z)} = \cos^{-1} \left[ \frac{ax + by + cz}{|(a, b, c)| \cdot |(x, y, z)|} \right]$$
- For  $\{100\}$  and  $\{110\} \rightarrow 45^\circ$
- For  $\{100\}$  and  $\{111\} \rightarrow 54.74^\circ$
- For  $\{110\}$  and  $\{111\} \rightarrow 35.26^\circ, 90^\circ, \text{ and } 144.74^\circ$

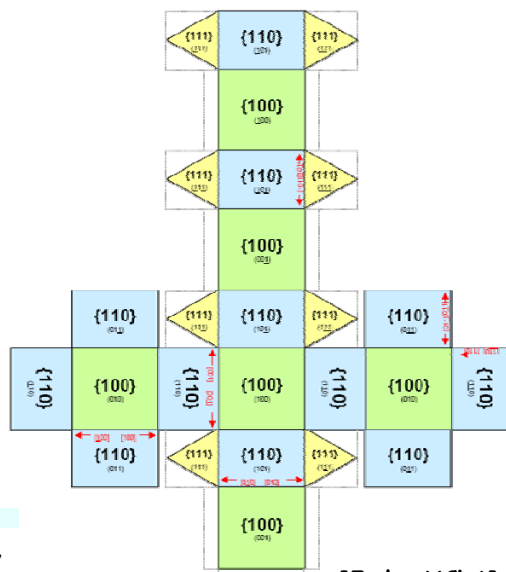
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**Silicon Crystal Origami**



*Judy*

- Silicon fold-up cube
- Adapted from Profs. Kris Pister and Jack Judy
- Print onto transparency
- Assemble inside out
- Visualize crystal plane orientations, intersections, and directions



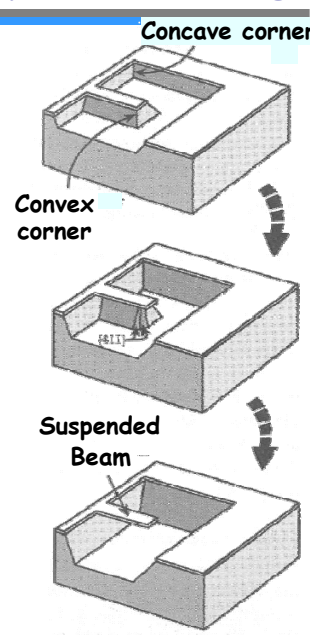
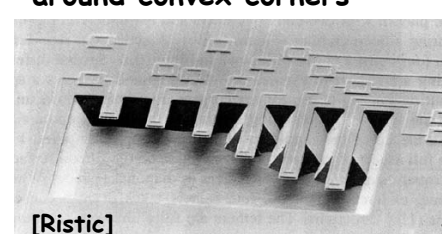
[Judy, UCLA]

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### Undercutting Via Anisotropic Si Etching

**UC Berkeley**

- Concave corners bounded by  $\{111\}$  are not attacked
- ... but convex corners bounded by  $\{111\}$  are attacked
  - ↳ Two  $\{111\}$  planes intersecting now present two dangling bonds → no longer have just one dangling bond → etch rate fast
  - ↳ **Result:** can undercut regions around convex corners

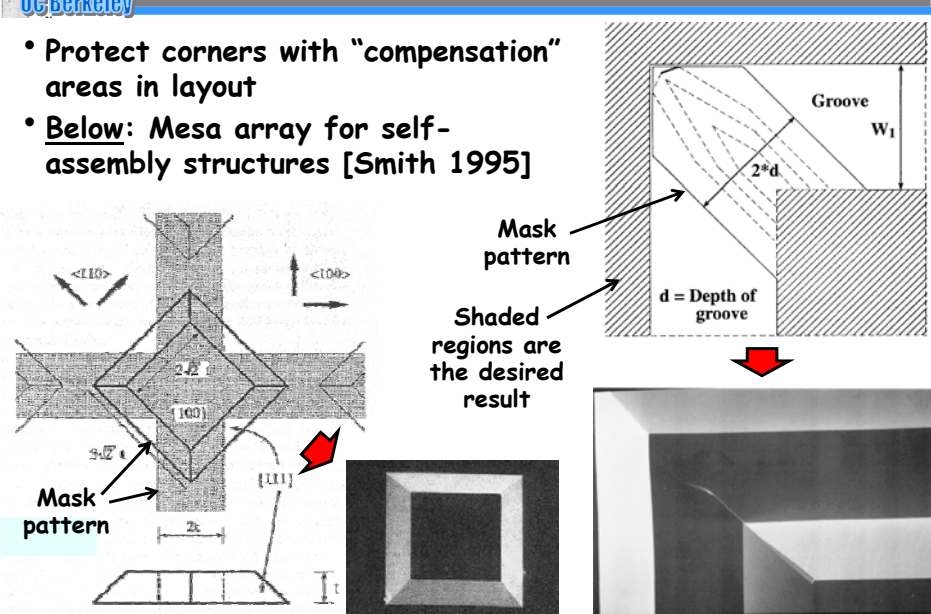
[Ristic]

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### Corner Compensation

**UC Berkeley**

- Protect corners with "compensation" areas in layout
- Below: Mesa array for self-assembly structures [Smith 1995]



Mask pattern


Shaded regions are the desired result

Groove  $W_1$

$2*d$

$d$  = Depth of groove


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## Other Anisotropic Silicon Etchants

- TMAH, Tetramethyl ammonium hydroxide, 10-40 wt.% (90°C)
  - ↗ Etch rate (100) = 0.5-1.5  $\mu\text{m}/\text{min}$
  - ↗ Al safe, IC compatible
  - ↗ Etch ratio (100)/(111) = 10-35
  - ↗ Etch masks:  $\text{SiO}_2$ ,  $\text{Si}_3\text{N}_4$  ~ 0.05-0.25 nm/min
  - ↗ Boron doped etch stop, up to 40× slower
- EDP (115°C)
  - ↗ Carcinogenic, corrosive
  - ↗ Etch rate (100) = 0.75  $\mu\text{m}/\text{min}$
  - ↗ Al may be etched
  - ↗  $R(100) > R(110) > R(111)$
  - ↗ Etch ratio (100)/(111) = 35
  - ↗ Etch masks:  $\text{SiO}_2$  ~ 0.2 nm/min,  $\text{Si}_3\text{N}_4$  ~ 0.1 nm/min
  - ↗ Boron doped etch stop, 50× slower


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## Boron-Doped Etch Stop

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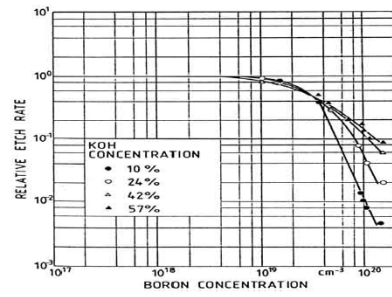
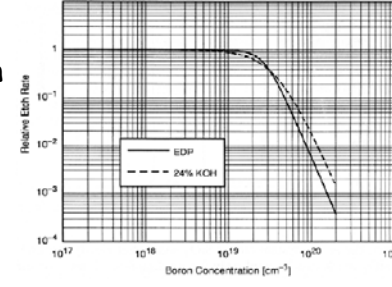





## Boron-Doped Etch Stop

- Control etch depth precisely with boron doping (p++)
  - ↳  $[B] > 10^{20} \text{ cm}^{-3}$  reduces KOH etch rate by 20-100×
  - ↳ Can use gaseous or solid boron diffusion
  - ↳ Recall etch chemistry:
 
$$\text{Si} + 2\text{OH}^- \rightarrow \text{Si}(\text{OH})_2^{2-} + 4\text{e}^-$$

$$4\text{H}_2\text{O} + 4\text{e}^- \rightarrow 4(\text{OH})^- + 2\text{H}_2$$
  - ↳ At high dopant levels, injected electrons recombine with holes in valence band and are unavailable for reactions to give  $\text{OH}^-$
- **Result:**
  - ↳ Beams, suspended films
  - ↳ 1-20  $\mu\text{m}$  layers possible

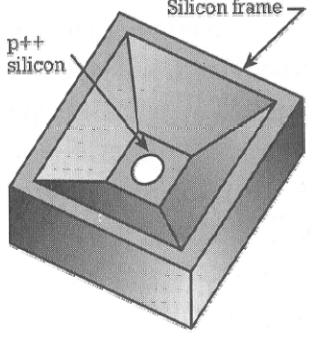



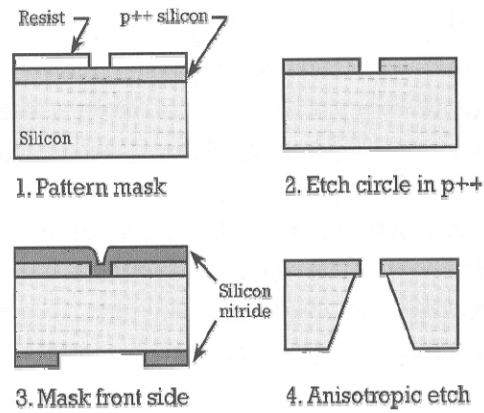
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## Ex: Micronozzle

- Micronozzle using anisotropic etch-based fabrication
- Used for inkjet printer heads






[Maluf]

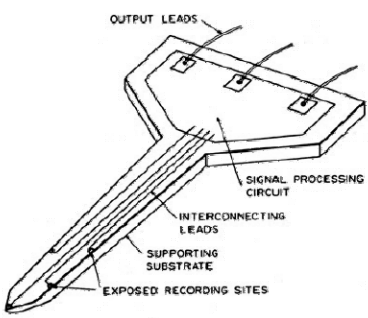
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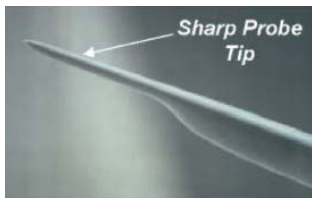


## Ex: Microneedle

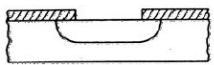
- **Below:** micro-neurostimulator
  - ↳ Used to access central nervous system tissue (e.g., brain) and record electrical signals on a cellular scale
- Wise Group, Univ. of Michigan



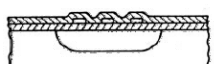
**Multi-Channel Recording Array Structure**



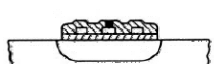
Sharp Probe Tip



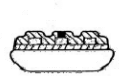
Selectively diffuse p++ into substrate



Deposit interconnect pattern and insulate conductors




Pattern dielectric and metallize recording sites

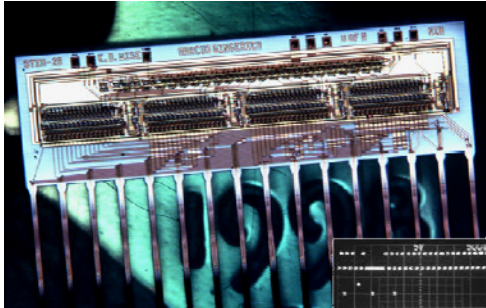


Dissolve away the wafer (no mask needed)

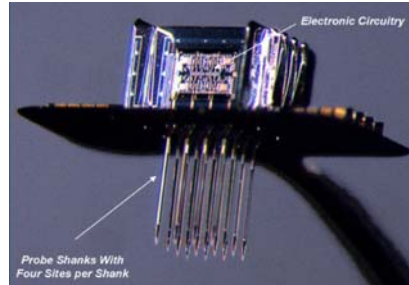
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## Ex: Microneedles (cont.)



**64-Site Multiplexed Stimulating Array**




Electronic Circuitry

Probe Shanks With Four Sites per Shank

[Wise, U. of Michigan]


- Micromachined with on-chip CMOS electronics
- Both stimulation and recording modes
- 400  $\mu\text{m}$  site separations, extendable to 3D arrays
- Could be key to neural prosthesis systems focusing on the central nervous system

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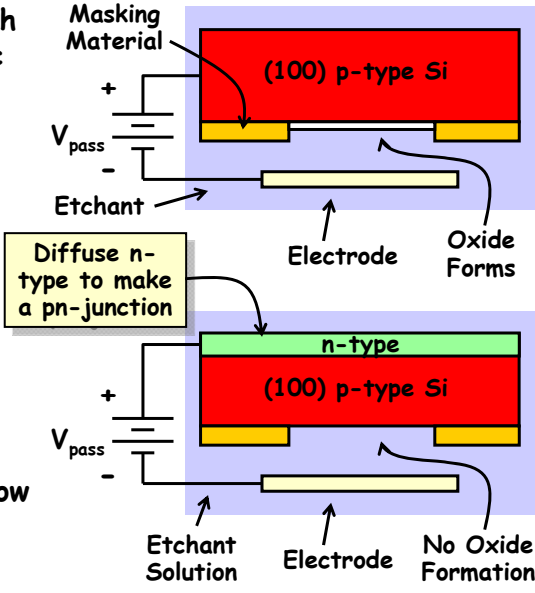
## Electrochemical Etch Stop

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## Electrochemical Etch Stop

- When silicon is biased with a sufficiently large anodic potential relative to the etchant → get oxidation (i.e., electrochemical passivation), which then prevents etching
- For passivation to occur, current flow is required
- If current flow can be prevented → no oxide growth, and etching can proceed
  - ↳ Can prevent current flow by adding a reverse-biased diode structure

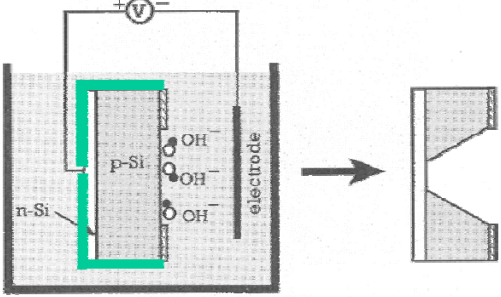


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## Electrochemical Etch Stop

- **Electrochemical etch stop**
  - ↪ n-type epitaxial layer grown on p-type wafer forms p-n junction diode
  - ↪  $V_p > V_n \rightarrow$  electrical conduction (current flow)
  - ↪  $V_p < V_n \rightarrow$  reverse bias current (very little current flow)
- **Passivation potential:** potential at which thin  $\text{SiO}_2$  film forms
  - ↪ different for p-Si and n-Si, but basically need the Si to be the anode in an electrolytic setup
- **Setup:**
  - ↪ p-n diode in reverse bias
  - ↪ p-substrate floating  $\rightarrow$  etched
  - ↪ n-layer above passivation potential  $\rightarrow$  not etched

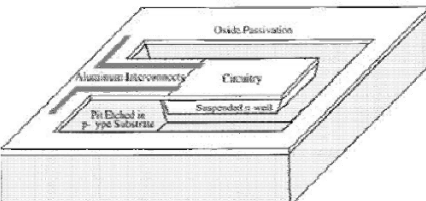
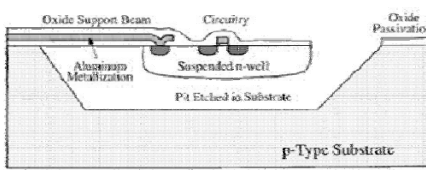


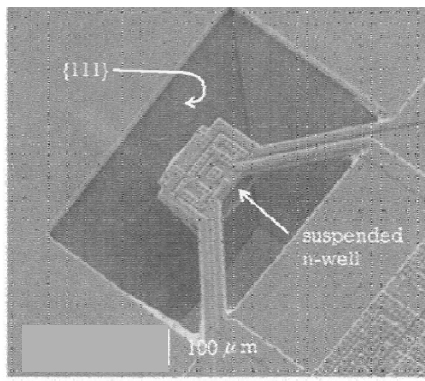
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## Electrochemical Etching of CMOS


- N-type Si well with circuits suspended f/  $\text{SiO}_2$  support beam
- Thermally and electrically isolated
- If use TMAH etchant, Al bond pads safe



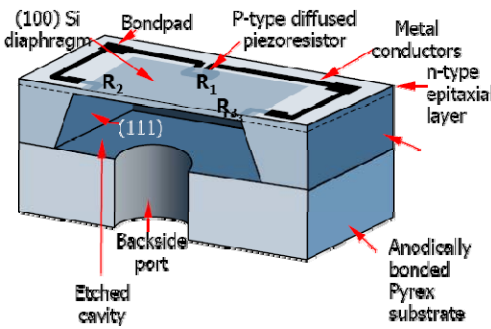
[Reay, et al. (1994)]  
[Kovacs Group, Stanford]


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## Ex: Bulk Micromachined Pressure Sensors


- **Piezoresistivity:** change in electrical resistance due to mechanical stress
- In response to pressure load on thin Si film, piezoresistive elements change resistance
- Membrane deflection < 1  $\mu\text{m}$






n-type epilayer, p-type substrate

*Deposit insulator*




Diffuse piezoresistors

*Diffuse piezoresistors*



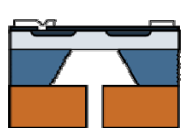
Deposit & pattern metal

*Deposit & pattern metal*



Electrochemical etch of backside cavity

*Electrochemical etch of backside cavity*



Anodic bonding of glass

*Anodic bonding of glass*


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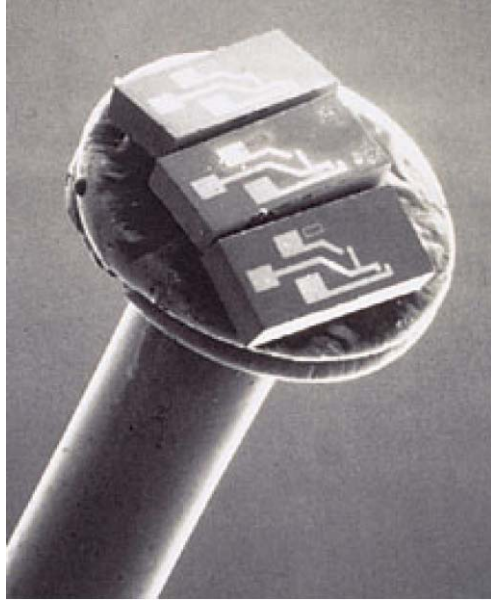
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## Ex: Pressure Sensors

- Below: catheter tip pressure sensor [Lucas NovaSensor]  
 Only 150×400×900  $\mu\text{m}^3$



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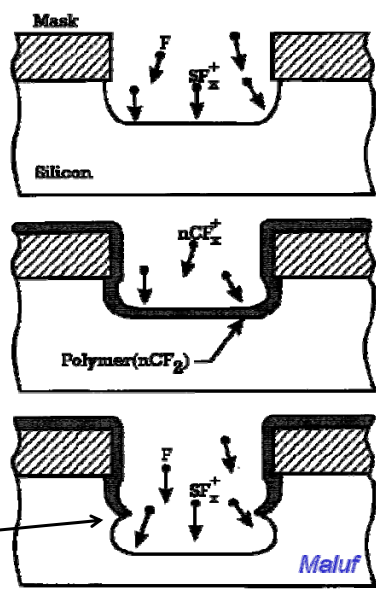
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## Deep Reactive-Ion Etching (DRIE)


**The Bosch process:**

- Inductively-coupled plasma
- Etch Rate: 1.5-4  $\mu\text{m}/\text{min}$
- Two main cycles in the etch:
  - Etch cycle** (5-15 s):  $\text{SF}_6$  ( $\text{SF}_x^+$ ) etches Si
  - Deposition cycle** (5-15 s):  $\text{C}_4\text{F}_8$  deposits fluorocarbon protective polymer  $(\text{CF}_2)_n$
- Etch mask selectivity:
  - $\text{SiO}_2 \sim 200:1$
  - Photoresist  $\sim 100:1$
- Issue:** finite sidewall roughness
  - scalloping < 50 nm
- Sidewall angle:  $90^\circ \pm 2^\circ$

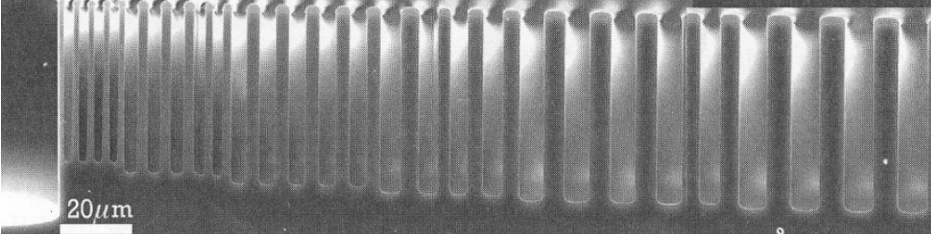


Maluf

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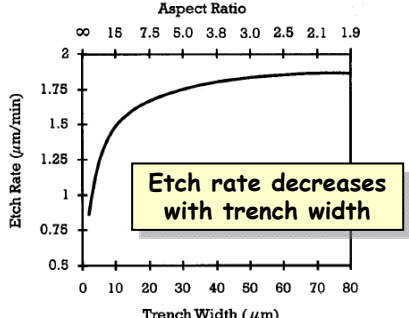


## DRIE Issues: Etch Rate Variance



20  $\mu\text{m}$

- Etch rate is diffusion-limited and drops for narrow trenches
  - Adjust mask layout to eliminate large disparities
  - Adjust process parameters (slow down the etch rate to that governed by the slowest feature)



Aspect Ratio

Etch Rate ( $\mu\text{m}/\text{min}$ )

Trench Width ( $\mu\text{m}$ )

Etch rate decreases with trench width

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**DRIE Issues: "Footing"**

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- Etch depth precision
  - Etch stop: buried layer of  $\text{SiO}_2$
  - Due to 200:1 selectivity, the (vertical) etch practically just stops when it reaches  $\text{SiO}_2$
- Problem:** Lateral undercut at  $\text{Si}/\text{SiO}_2$  interface  $\rightarrow$  "footing"
  - Caused by charge accumulation at the insulator

Poor charge relaxation and lack of neutralization by e-'s at insulator

Ion flux into substrate builds up (+) potential

mask

Si

insulation layer

Charge accumulation

Charging-induced potential perturbs the E-field

Distorts the ion trajectory

Result: strong and localized damage to the structure at  $\text{Si}-\text{SiO}_2$  interface  $\rightarrow$  "footing"

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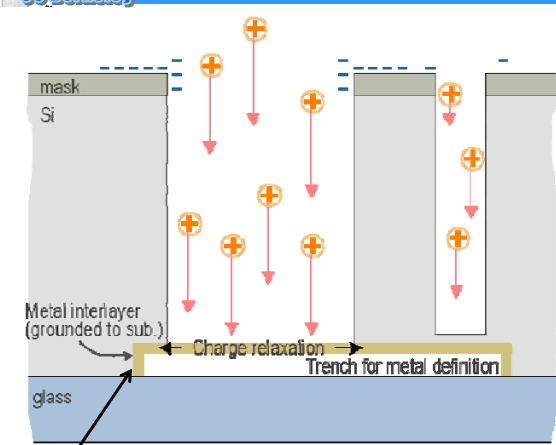
**Recipe-Based Suppression of "Footing"**

UC Berkeley

- Use **higher process pressure** to reduce ion charging [Nozawa]
  - High operating pressure  $\rightarrow$  concentration of (-) charge increases and can neutralize (+) surface charge
  - Issue:** must introduce as a separate recipe when the etch reaches the  $\text{Si}$ -insulator interface, so must be able to very accurately predict the time needed for etching
- Adjust etch recipe** to reduce overetching [Schmidt]
  - Change  $\text{C}_4\text{F}_8$  flow rate, pressure, etc., to enhance passivation and reduce overetching
  - Issue:** Difficult to simultaneously control footing in a narrow trench and prevent grass in wide trenches
- Use **lower frequency plasma** to avoid surface charging [Morioka]
  - Low frequency  $\rightarrow$  more ions with low directionality and kinetic energy  $\rightarrow$  neutralizes (-) potential barrier at trench entrance
  - Allows e-'s to reach the trench base and neutralize (+) charge  $\rightarrow$  maintain charge balance inside the trench

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### Metal Interlayer to Prevent "Footing"



Pre-defined metal interlayer grounded to substrate supplies e's to neutralize (+) charge and prevent charge accumulation at the Si-insulator interface

(a) Photolithography 1 (sacrificial)

(b) Preparatory trenches

(c) Metal interlayer deposition

(d) Lift-off (remove PR)

(e) Anodic Bonding

(f) Silicon Thinning

(g) Photolithography 2

(h) DRIE

(i) Remove metal interlayer

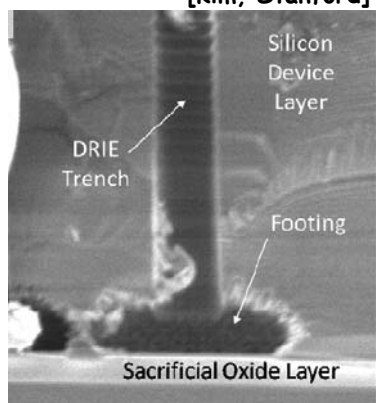
(j) Metallize

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### Footing Prevention (cont.)

- Below: DRIE footing over an oxide stop layer
- Right: efficacy of the metal interlayer footing prevention approach

[Kim, Stanford]



Silicon Device Layer

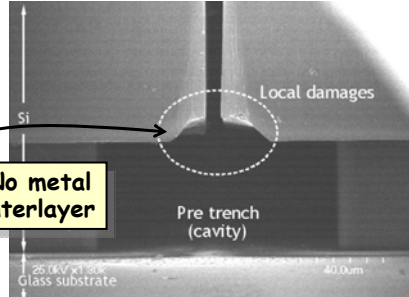
DRIE Trench

Footing

Sacrificial Oxide Layer

[Kim, Seoul Nat. Univ.]

**No metal interlayer**



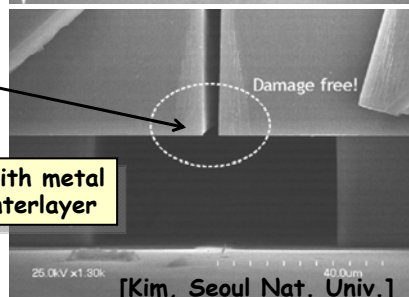
Local damages

Pre trench (cavity)

25.0kV x1.50k 40.0um

Glass substrate

**With metal interlayer**




Damage free!

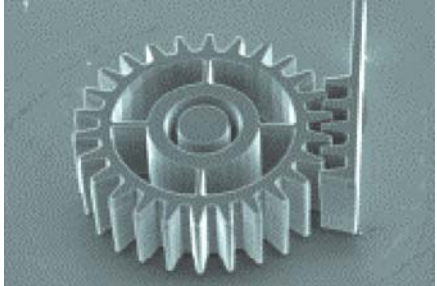
25.0kV x1.50k 40.0um

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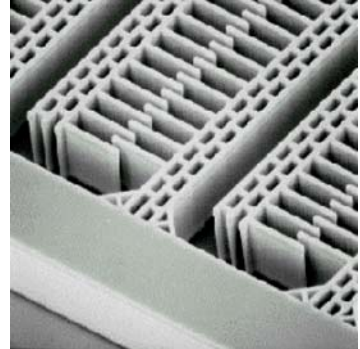




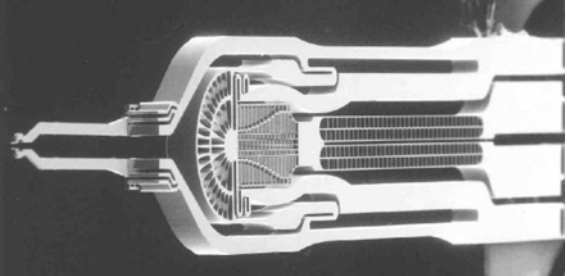
## DRIE Examples



**High aspect-ratio gear**




**Tunable Capacitor**  
[Yao, Rockwell]



**Microgripper**  
[Keller, MEMS Precision Instruments]

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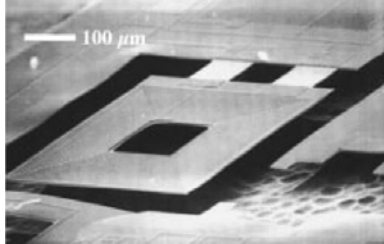
## Vapor Phase Etching of Silicon

- Vapor phase Xenon Difluoride ( $\text{XeF}_2$ )  

$$2\text{XeF}_{2(g)} + \text{Si}_{(s)} \rightarrow 2\text{Xe}_{(g)} + \text{SiF}_{4(g)}$$
- Set-up:
  - ↪ Xe sublimates at room T
  - ↪ Closed chamber, 1-4 Torr
  - ↪ Pulsed to control exothermic heat of reaction
- Etch rate: 1-3  $\mu\text{m}/\text{min}$ , isotropic
- Etch masks: photoresist,  $\text{SiO}_2$ ,  $\text{Si}_3\text{N}_4$ , Al, other metals
- Issues:
  - ↪ Etched surfaces have granular structure, 10  $\mu\text{m}$  roughness
  - ↪ Hazard:  $\text{XeF}_2$  reacts with  $\text{H}_2\text{O}$  in air to form Xe and HF


**Xactix  $\text{XeF}_2$  Etcher**





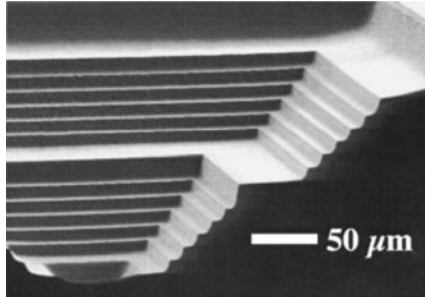
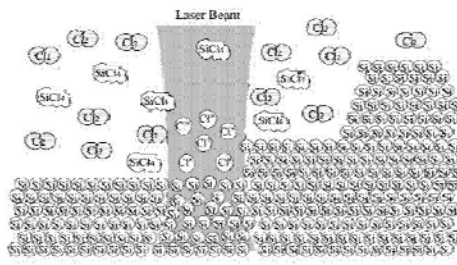
**Inductor w/ no substrate [Pister]**

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## Laser-Assisted Chemical Etching

- Laser creates Cl radicals from  $\text{Cl}_2 \rightarrow$  reaction forms  $\text{SiCl}_2$
- Etch rate:  $100,000 \mu\text{m}^3/\text{s}$ 
  - ↳ Takes 3 min. to etch  $500 \times 500 \times 125 \mu\text{m}^3$  trench
- Surface roughness: 30 nm rms
- Serial process: patterned directly from CAD file




- At right:
  - ↳ Laser assisted etching of a  $500 \times 500 \mu\text{m}^2$  terraced silicon well
  - ↳ Each step is  $6 \mu\text{m}$ -deep

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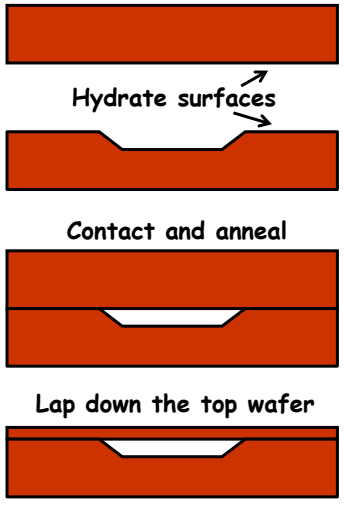
## Wafer Bonding

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## Fusion Bonding


- Two ultra-smooth ( $<1$  nm roughness) wafers are bonded without adhesives or applied external forces
- Procedure:**
  - Prepare surfaces: must be smooth and particle-free
    - Clean & hydrate:  $O_2$  plasma, hydration, or HF dip
  - When wafers are brought in contact at room temperature, get hydrogen bonding and/or van der Waals forces to hold them together
  - Anneal at  $600$ – $1200^\circ\text{C}$  to bring the bond to full strength
- Result:** a bond as strong as the silicon itself!



The diagram illustrates the four steps of fusion bonding: 1. Two separate wafers. 2. Surfaces being hydrated (indicated by arrows). 3. Wafers in contact and being annealed. 4. The top wafer being fully lapped down onto the bottom wafer.

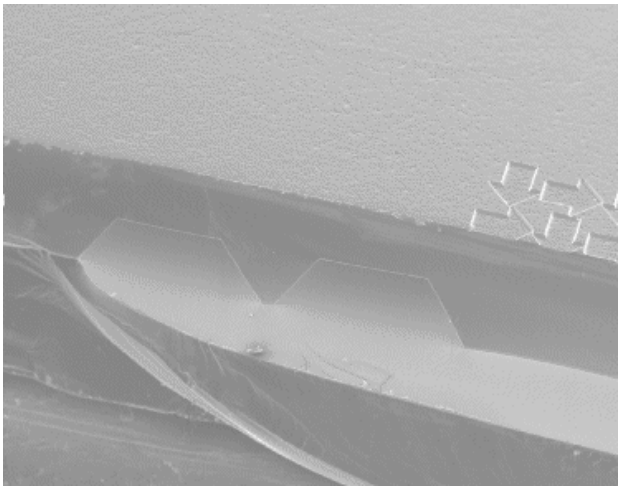
Works for Si-to-Si bonding and Si-to-SiO<sub>2</sub> bonding

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## Fusion Bonding Example


- Below:** capacitive pressure sensor w/ fusion-bonded features



A grayscale micrograph showing a complex micro-fabricated structure, which is a capacitive pressure sensor. It features various rectangular and circular patterns on a surface.

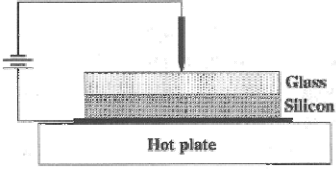
[Univ. of Southampton]

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## Anodic Bonding

- Bonds an electron conducting material (e.g., Si) to an ion conducting material (e.g., sodium glass = Pyrex)
- Procedure/Mechanism:
  - ↗ Press Si and glass together
  - ↗ Elevate temperature: 180-500°C
  - ↗ Apply (+) voltage to Si: 200-1500V
    - (+) voltage repels Na<sup>+</sup> ions from the glass surface
    - Get net (-) charge at glass surface
    - Attractive force between (+) Si and (-) glass → intimate contact allows fusing at elevated temp.
  - ↗ Current drops to zero when bonding is complete

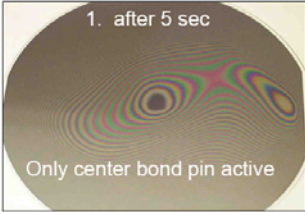


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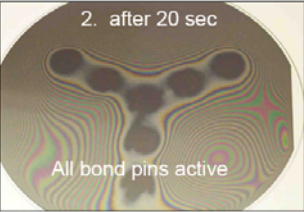


## Anodic Bonding (cont.)

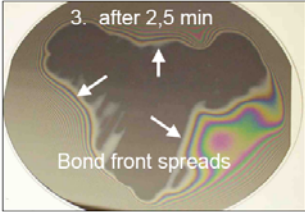
- **Advantage:** high pressure of electrostatic attraction smoothes out defects
- **Below:** 100 mm wafers, Pyrex glass 500 μm-thick, 430°C, 800V, N<sub>2</sub> @ 1000 mbar



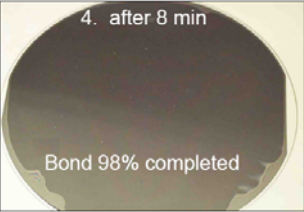
1. after 5 sec  
Only center bond pin active



2. after 20 sec  
All bond pins active




3. after 2.5 min  
Bond front spreads



4. after 8 min  
Bond 98% completed


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## Metal Layer Bonding

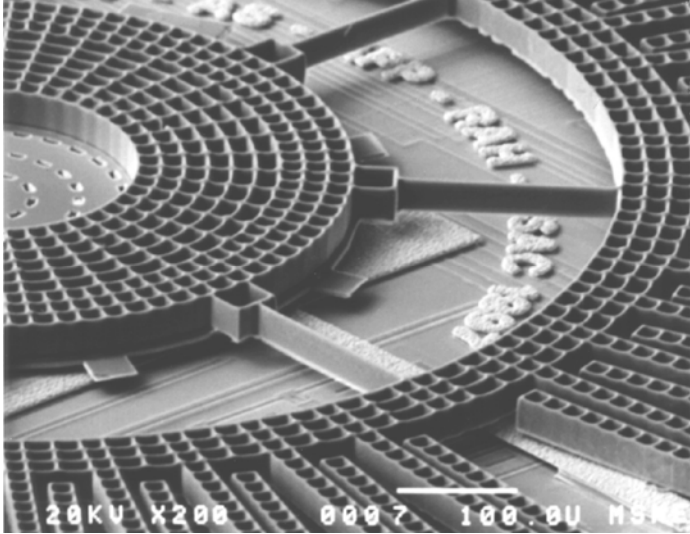
- Pattern seal rings and bond pads photolithographically
- **Eutectic bonding**
  - ↗ Uses eutectic point in metal-Si phase diagrams to form silicides
  - ↗ Au and Si have eutectic point at 363°C
  - ↗ Low temperature process
  - ↗ Can bond slightly rough surfaces
  - ↗ Issue: Au contamination of CMOS
- **Solder bonding**
  - ↗ PbSn (183°C), AuSn (280°C)
  - ↗ Lower-T process
  - ↗ Can bond very rough surfaces
  - ↗ Issue: outgassing (not good for encapsulation)
- **Thermocompression**
  - ↗ Commonly done with electroplated Au or other soft metals
  - ↗ Room temperature to 300°C
  - ↗ Lowest-T process
  - ↗ Can bond rough surfaces with topography

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## Thermocompression Bonding


- Below: Transfer of hexsil actuator onto CMOS wafer



[Singh, et al, Transducers'97]

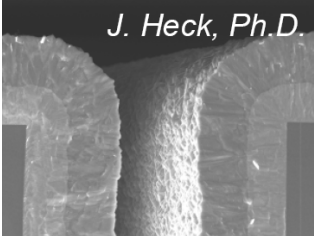
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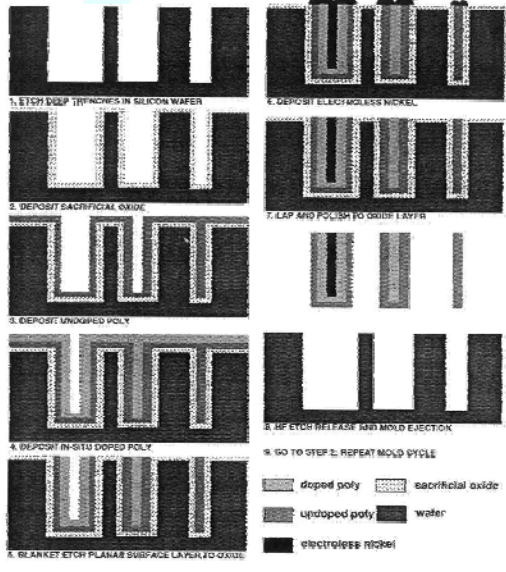





## Hexsil MEMS

- Achieves high aspect ratio structures using conformal thin films in mold trenches
- Parts are demolded (and transferred to another wafer)
- Mold can be reused
- Design with honeycomb structure for strength



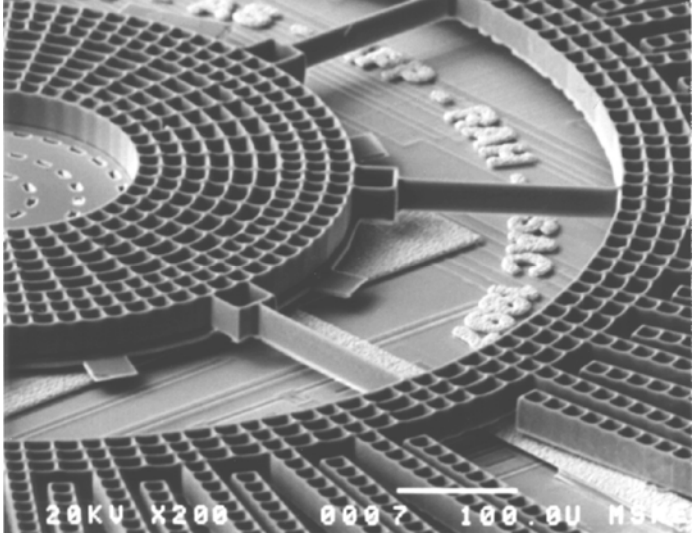


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## Hexsil MEMS Actuator

- Below: Transfer of hexsil actuator onto CMOS wafer

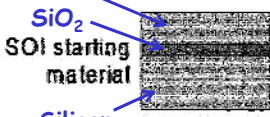

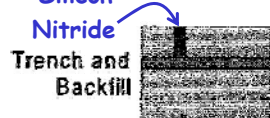

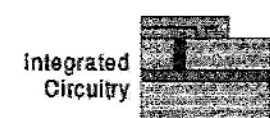





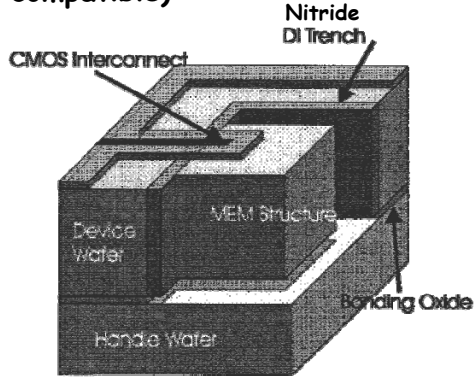
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## Silicon-on-Insulator (SOI) MEMS

- No bonding required
- Si mechanical structures anchored by oxide pedestals
- Rest of the silicon can be used for transistors (i.e., CMOS compatible)

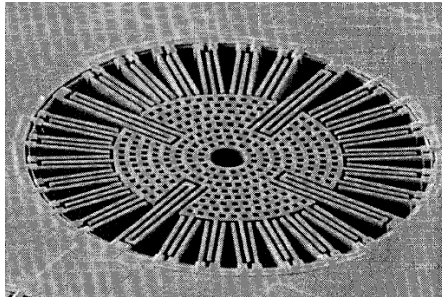
	Cross Section	Top View
SOI starting material		
Nitride Trench and Backfill		
Integrated Circuitry		
Structure definition and release		



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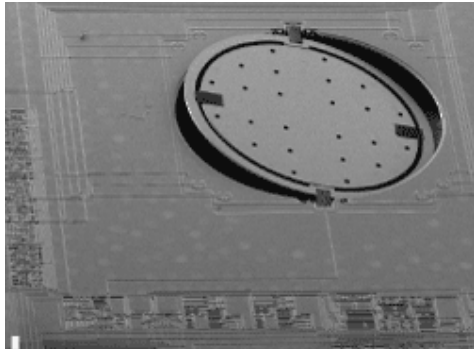


## SOI MEMS Examples




[Brosnihan]

Micromirror  
[Analog Devices]



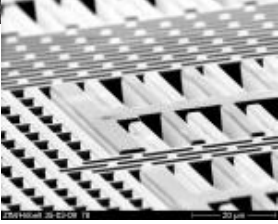
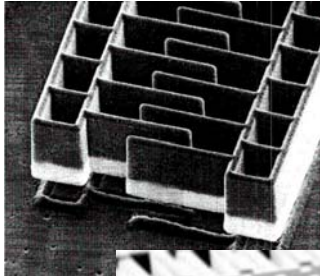
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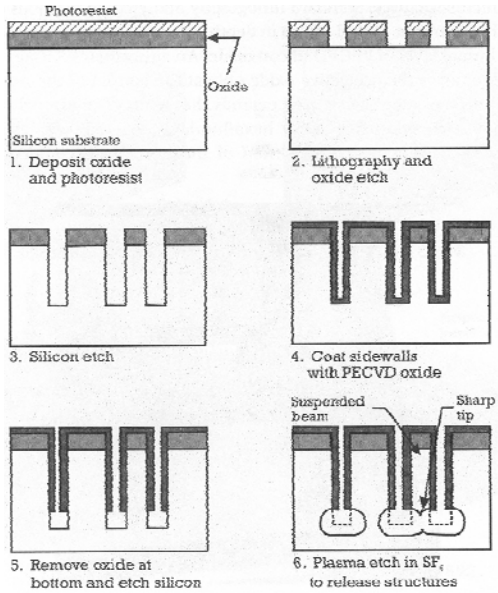




## The SCREAM Process

- **SCREAM**: **S**ingle **C**rystal **R**eactive **E**tching and **M**etallization process





1. Deposit oxide and photoresist

2. Lithography and oxide etch

3. Silicon etch

4. Coat sidewalls with PECVD oxide

5. Remove oxide at bottom and etch silicon

6. Plasma etch in  $\text{SF}_6$  to release structures

Labels: Photoreist, Oxide, Silicon substrate, Suspended beam, Sharp tip

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