EE247
Lecture 9
Switched-Capacitor Filters

• Summary of last lecture
• DDI integrators
• LDI integrators
  – Effect of parasitic capacitance
  – Bottom-plate integrator topology
• Resonators
• Bandpass filters
• Lowpass filters
  – Termination implementation

Summary Last Session
Switched-Capacitor Resistors

Charge transferred in one cycle:
\[ Q = CV_{IN} - V_{OUT} \]
\[ i = \frac{Q}{T} = Qf_s \rightarrow i = f_2C(v_{IN} - v_{OUT}) \]

With the current through the switched capacitor resistor proportional to the voltage across it, the equivalent “switched capacitor resistance” is:

\[ R_{eq} = \frac{1}{f_sC} \]

Example
\[ f = 1MHz, C = 1pF \]
\[ \rightarrow R_{eq} = 1Mega\Omega \]
Switched-Capacitor Filter

- Let’s build an “SC” filter …
- We’ll start with a simple RC LPF
- Replace the physical resistor by an equivalent SC resistor
- 3-dB bandwidth:
  \[ \omega_{-3dB} = \frac{j}{R_{eq}C_2} = f_s \times \frac{C_1}{C_2} \]
  \[ f_{-3dB} = \frac{j}{2\pi} f_s \times \frac{C_1}{C_2} \]

Switched-Capacitor Filter Advantage versus Continuous-Time Filters

- Corner freq. proportional to:
  - System clock (accurate to few ppm)
  - C ratio accurate \( \rightarrow < 0.1\% \)

- Corner freq. proportional to:
  - Absolute value of \( R_s \) & \( C_s \)
  - Poor accuracy \( \rightarrow 20 \) to 50%

Main advantage of SC filter inherent corner frequency accuracy
Typical Sampling Process
Continuous-Time (CT) ⇒ Sampled Data (SD)

Sampling Sine Waves
Aliasing

- Multiple continuous time signals can produce identical series of sampled voltages
- The folding back of signals from $nf_S + f_{\text{sig}}$ down to $f_{\text{fin}}$ is called aliasing
  - Sampling theorem: $f_s > 2f_{\text{max,Signal}}$
- If aliasing occurs, no signal processing operation downstream of the sampling process can recover the original continuous time signal
- To Avoid aliasing → two possibilities:
  1. Sample fast enough to cover all spectral components, including "parasitic" ones outside band of interest
  2. Limit $f_{\text{max,Signal}}$ through filtering

How to Avoid Aliasing

1- Push sampling frequency to x2 of the highest freq. → In most cases not practical

2- Pre-filter signal to eliminate signals above 1/2 sampling frequency- then sample
Anti-Aliasing Filter

Case 1: \( B = f_{\text{max}} - \text{Signal} = f_s/2 \)

- Non-practical since an extremely high order anti-aliasing filter (close to an ideal brickwall filter) is required
- Practical anti-aliasing filter → Nonzero filter "transition band"
- In order to make this work, we need to sample much faster than 2x the signal bandwidth → "Oversampling"

Practical Anti-Aliasing Filter

Case 2: \( B = f_{\text{max}} - \text{Signal} \ll f_s/2 \)

- More practical anti-aliasing filter
- Preferable to have an anti-aliasing filter with:
  - The lowest order possible
  - No frequency tuning required (if frequency tuning is required then why use SC filter, just use the prefilter!?)
**Tradeoff**

Oversampling Ratio versus Anti-Aliasing Filter Order

- Tradeoff: Sampling speed vs. filter order

* Assumption: anti-aliasing filter is Butterworth type

**Effect of Sample & Hold**

\[ |H(f)| = \frac{T_p}{T_s} \frac{\sin(\pi f T_p)}{\pi f T_p} \]

- Using the Fourier transform of a rectangular impulse:

**References:**

Effect of Sample & Hold on Frequency Response

\[ |H(f)| = \frac{T_p \sin(\pi f T_p)}{T_s \pi f T_p} \]

Sample & Hold Effect (Reconstruction of Analog Signals)

\[ v(t) = \sin(2\pi f_{in} t) \]

Magnitude droop due to \( \sin x / x \) effect
Sample & Hold Effect
(Reconstruction of Analog Signals)

Magnitude droop due to \( \sin x/x \) effect:

Case 1) \( f_{sig} = f_s / 4 \)

\( \text{Droop} = -1 \text{dB} \)

Case 2) \( f_{sig} = f_s / 100 \)

\( \text{Droop} = -0.0015 \text{dB} \)

→ High oversampling ratio desirable
Sampling Process Including S/H

First Order S.C. Filter

Switched-Capacitor Filters \(\rightarrow\) problem with aliasing
Sampled-Data Filters
Anti-aliasing Requirements

- Frequency response repeats at $f_s$, $2f_s$, $3f_s$, ....
- High frequency signals close to $f_s$, $2f_s$, ..., folds back into passband (aliasing)
- Most cases must pre-filter input to a sampled-data filter to remove signal at $f > f_s/2$ (nyquist $\Rightarrow f_{\text{max}} < f_s/2$)
- Usually, anti-aliasing filter included on-chip as continuous-time filter with relaxed specs. (no tuning)

Example: Anti-Aliasing Filter

- Voice-band SC filter $f_{\text{3dB}} = 4\text{kHz}$ & $f_s = 256\text{kHz}$
- Anti-aliasing filter requirements:
  - Need 40dB attenuation at clock freq.
  - Incur no phase-error from 0 to 4kHz
  - Gain error 0 to 4kHz < 0.05dB
  - Allow $\pm$30% variation for anti-aliasing corner frequency (no tuning)
    $\Rightarrow$ Oversampling ratio $= 256\text{kHz}/2\times4\text{kHz} = 32$
    $\Rightarrow$ Need to find minimum filter order
Oversampling Ratio versus Anti-Aliasing Filter Order

Maximum Aliasing Dynamic Range

$\frac{f_s}{2f_{\text{in max}}}$

* Assumption: anti-aliasing filter is Butterworth type

→ 2nd order Butterworth
→ Need to find minimum corner frequency for mag. droop < 0.05dB

Example: Anti-Aliasing Filter Specifications

- Normalized frequency for 0.05dB droop → 0.34 → 4kHz/0.34=12kHz
- Set anti-aliasing filter corner frequency for minimum corner frequency 12kHz → Nominal corner frequency 12x1.3=15.6kHz
- Check if attenuation requirement is satisfied for widest filter bandwidth → 15.6x1.3=20.2kHz
- Normalized filter corner freq. to clock freq. =256/20.2=12.6
- Check phase-error within 4kHz bandwidth

From: Williams and Taylor, p. 2-37
Example: Anti-Aliasing Filter

- Voice-band SC filter $f_{\text{3dB}} = 4\text{kHz}$ & $f_s = 256\text{kHz}$
- Anti-aliasing filter requirements:
  - Need 40dB attenuation at clock freq.
  - Incur no phase-error from 0 to 4kHz
  - Gain error 0 to 4kHz < 0.05dB
  - Allow +-30% variation for anti-aliasing corner frequency (no tuning)

→ 2-pole Butterworth LPF with nominal corner freq. of 15.6kHz & no tuning

Ease of anti-aliasing → high ratio for $f_{\text{sampling}} / f_{\text{3dB}}$

Switched-Capacitor Noise

- The mean-squared noise current due to S1 and S2’s kT/C noise is:
  $$ \bar{i}^2 = \left(Qf_s\right)^2 = 2k_BT Cf_s^2 $$

- This noise is approximately white and distributed between 0 and $f/2$
  (noise spectra → single sided by convention)
  The spectral density of the noise is:
  $$ \bar{i}^2 = \frac{2k_BT_Cf_s^2}{f_s/2} = 4k_BT_Cf_s = \frac{4k_BT}{R_{\text{eq}}} \text{ using } R_{\text{eq}} = \frac{1}{f_sC} $$

→ S.C. resistor noise equals a physical resistor noise with same value!
Switched-Capacitor Integrator

\[ V_0 = \frac{f_s C_s}{C_I} \int V_{in} \, dt \]

Main advantage: No tuning needed
→ critical frequency function of ratio of caps & clock freq.

SC Integrator

\( \phi_1 \) High → \( C_s \) Charged to Vin

\( \phi_2 \) High → Charge transferred from \( C_s \) to \( C_I \)
Continuous-Time versus Discrete Time
Design Flow

Continuous-Time
- Write differential equation
- Laplace transform \( F(s) \)
- Let \( s=j\omega \rightarrow F(j\omega) \)
- Plot \(|F(j\omega)|, \text{phase}(F(j\omega)|\)

Discrete-Time
- Write difference equation, \( \rightarrow \) relates output sequence to input sequence
  \[ V_o(nT_s) = V_i \left[ (n-I)T_s \right] - \ldots \]
- Use delay operator \( Z^{-1} \) to transform the recursive realization to algebraic equation in \( Z \) domain
  \[ V_o(Z) = Z^{-1}V_i(Z) \ldots \]
- Set \( Z = e^{j\omega T} \)
- Plot mag./phase versus frequency

SC Integrator

SC Integrator diagram with inputs and outputs labeled.

Voltage waveforms for Vin, Vs, and Vo are shown over time with clock phases indicated.

EECS 247 Lecture 9: SC Filters © 2004 H. K. Page 28
### SC Integrator

\[
\Phi_1 \rightarrow Q_i [(n-1)T_s] = C_i V_i [(n-1)T_s] \quad Q_i [(n-1)T_s] = Q_i [(n-3/2)T_s]
\]

\[
\Phi_2 \rightarrow Q_i [(n-1/2)T_s] = 0 \quad Q_i [(n-1/2)T_s] = Q_i [(n-3/2)T_s] + Q_i [(n-1)T_s]
\]

\[
\Phi_1 \rightarrow Q_i [nT_s] = C_i V_i [nT_s]
\]

Since \( V_o = -Q_i /C_i \) \& \( V_i = Q_i /C_i \) \rightarrow \( C_i V_o [nT_s] = C_i V_o [(n-1)T_s] - C_i V_i [(n-1)T_s] \)

### Discrete Time Design Flow

- Transforming the recursive realization to algebraic equation in Z domain:
  - Use Delay operator Z:

\[
\begin{align*}
nT_s & \rightarrow 1 \\
(n-1)T_s & \rightarrow Z^{-1} \\
(n-1/2)T_s & \rightarrow Z^{-1/2} \\
(n+1)T_s & \rightarrow Z^{+1} \\
(n+1/2)T_s & \rightarrow Z^{+1/2}
\end{align*}
\]
SC Integrator

\[-C_I V_o(nT_s) = -C_I V_o[(n-1)T_s] + C_S V_{in}[(n-1)T_s]\]

\[V_o(nT_s) = V_o[(n-1)T_s] - \frac{C_S}{C_I} V_{in}[(n-1)T_s]\]

\[V_o(Z) = Z^{-1}V_o(Z) - Z^{-1}\frac{C_S}{C_I} V_{in}(Z)\]

\[\frac{V_o(Z)}{V_{in}(Z)} = -\frac{C_S}{C_I} \frac{Z^{-1}}{1-Z^{-T}}\]

DDI (Direct-Transform Discrete Integrator)

z-Domain Frequency Response

- LHP singularities in s-plane map into inside of unit-circle in Z domain
- RHP singularities in s-plane map into outside of unit-circle in Z domain
- The j\(\omega\) axis maps onto the unit circle
- Particular values:
  - \(f = 0 \rightarrow z = 1\)
  - \(f = f_s/2 \rightarrow z = -1\)
- The frequency response is obtained by evaluating \(H(z)\) on the unit circle at
  \(z = e^{j\omega T} = \cos(\omega T) + j\sin(\omega T)\)
- Once \(z=-1\) (\(f_s/2\)) is reached, the frequency response repeats, as expected
- The angle to the pole is equal to \(360^\circ\) (or \(2\pi\) radians) times the ratio of the pole frequency to the sampling frequency
Switched-Capacitor Direct-Transform Discrete Integrator

\[ \frac{V_o(z)}{V_{in}} = -\frac{C_c}{C_I} \times \frac{z^{-1}}{1-z^{-1}} \]

\[ = -\frac{C_s}{C_I} \times \frac{1}{z^{-1}} \]

DDI Integrator
Pole-Zero Map in z-Plane

Z-1 = 0 \rightarrow Z=1
on unit circle

Pole from \( f \rightarrow 0 \)
in s-plane mapped to \( z=+1 \)

As frequency increases z domain pole moves on unit circle (CCW)

Onces pole gets to \( (Z=-1), (f=f_s/2) \),
frequency response repeats
DDI SC Integrator

$$V_o(Z) = \frac{C_x}{C_I} \frac{Z^{-1}}{1-Z^{-1}}$$

$$V_o(Z) = \frac{C_x}{C_I} \frac{1}{Z^{-1}} \quad Z = e^{j\omega T}$$

Series expansion for $e^x$

$$e^x = 1 + x + \frac{x^2}{2!} + \frac{x^3}{3!} + \ldots$$

For $\omega T << 1$

$$V_o(\omega) = -\frac{C_x}{C_I} \frac{j\omega T}{1}$$

Since $T = \frac{1}{f_s}$

$$V_o(\omega) = -\frac{C_x}{C_I} \frac{j\omega}{\pi}$$

$V_o(\omega) \rightarrow$ ideal integrator

DDI SC Integrator

$$V_o(Z) = \frac{C_x}{C_I} \frac{Z^{-1}}{1-Z^{-1}}$$

$Z = e^{j\omega T}$

$$= \frac{C_x}{C_I} \frac{1}{1-e^{j\omega T}} = \frac{C_x}{C_I} \frac{e^{-j\omega T/2}}{e^{j\omega T/2} - e^{-j\omega T/2}} = -\frac{C_x}{C_I} e^{-j\omega T/2} \frac{1}{2 \sin(\omega T/2)}$$

$$= -\frac{C_x}{C_I} \frac{1}{2\omega} \times \frac{e^{j\omega T/2}}{\sin(\omega T/2)} \times e^{-j\omega T/2}$$

Ideal Integrator) Magnitude Error

$$V_o(Z) = \frac{C_x}{C_I} \frac{Z^{-1}}{1-Z^{-1}}$$

$$V_o(Z) = \frac{C_x}{C_I} \frac{1}{Z^{-1}} \quad Z = e^{j\omega T}$$

Series expansion for $e^x$

$$e^x = 1 + x + \frac{x^2}{2!} + \frac{x^3}{3!} + \ldots$$

For $\omega T << 1$

$$V_o(\omega) = -\frac{C_x}{C_I} \frac{j\omega T}{1}$$

Since $T = \frac{1}{f_s}$

$$V_o(\omega) = -\frac{C_x}{C_I} \frac{j\omega}{\pi}$$

$V_o(\omega) \rightarrow$ ideal integrator
**DDI SC Integrator**

\[ \frac{V_o}{V_{in}}(Z) = \frac{1}{sC} \times \frac{\sin(\omega T/2)}{\sin(\omega T/2)} \times e^{-\frac{j \omega T}{2}} \]

Example: Mag. & phase error for:

1. \( f / f_s = 1/12 \) → Mag. Error = 1% or 0.1 dB  
   Phase error = 15 degree  
   \( Q_{intg} = -3.8 \)  
   **DDI Integrator** → magnitude error no problem  
   phase error major problem

2. \( f / f_s = 1/32 \) → Mag. Error = 0.16% or 0.014 dB  
   Phase error = 5.6 degree  
   \( Q_{intg} = -10.2 \)

**Switched Capacitor Filter**

Build with DDI Integrator

Example: 5th Order Elliptic Filter  
Singularities pushed towards RHP due to integrator excess phase
Switched Capacitor Filter
Build with DDI Integrator

Continuous-Time
Prototype

SC DDI based
Filter

Passband
Peaking

Zeros lost!

SC Integrator

Sample output \( \frac{1}{2} \) clock cycle earlier
\( \rightarrow \) Sample output on \( \phi_2 \)
**SC Integrator**

\[ \Phi_1 \rightarrow Q_i[(n-1)T_s] = C_s V_i[(n-1)T_s], \quad Q_i[(n-1)T_s] = Q_i[(n-3/2)T_s] \]

\[ \Phi_2 \rightarrow Q_i[(n-1/2)T_s] = 0, \quad Q_i[(n-1/2)T_s] = Q_i[(n-3/2)T_s] + Q_i[(n-1)T_s] \]

**LDI SC Integrator**

**LDI (Lossless Discrete Integrator)** →

*same as DDI but output is sampled ½ clock cycle earlier*

\[ \frac{V_o(Z)}{V_{ih}} = \frac{C_1}{C_f} \times \frac{Z^{-1/2}}{1-Z^{-1}}, \quad Z = e^{\pi f T} \]

\[ = \frac{C_1}{C_f} \times e^{\pi f T/2} = \frac{C_1}{C_f} \times e^{\pi f T/2} \frac{1}{1-e^{\pi f T/2}} \]

\[ = -j \frac{C_1}{C_f} \frac{1}{2 \sin(\pi f T/2)} \]

**Ideal Integrator**

\[ = \frac{C_1}{C_f} \frac{\omega f T/2}{\sin(\omega f T/2)} \]

**Magnitude Error**

\[ V_o(Z) = V_{ih} C_1 C_f Z^{-1/2} \]

**No Phase Error!**

For signals at frequency \(<<\) sampling freq.

\[ \rightarrow \text{Magnitude error negligible} \]
Frequency Warping

- Frequency response
  - Continuous time (s-plane): imaginary axis
  - Sampled time (z-plane): unit circle
- Continuous to sampled time transformation
  - Should map imaginary axis onto unit circle
  - How do SC integrators map frequencies?

\[
H_{sc}(z) = \frac{C_i}{C_m} \frac{\varepsilon^{j\omega}}{1 - \varepsilon^{-1}}
\]

\[
= -\frac{C_i}{C_m} \frac{1}{2 j \sin \pi f_T T}
\]

CT – SC Integrator Comparison

**CT Integrator**

\[
H_{ct}(s) = -\frac{1}{s \tau}
\]

\[
= -\frac{1}{2 \pi f_{sc} \tau}
\]

**SC Integrator**

\[
H_{sc}(z) = \frac{C_i}{C_m} \frac{\varepsilon^{j\omega}}{1 - \varepsilon^{-1}}
\]

\[
= -\frac{C_i}{C_m} \frac{1}{2 j \sin \pi f_{sc} T}
\]

Identical time constants:

\[
\tau = RC = \frac{C_m}{f_c C_i}
\]

Compare: \( H_{ct}(f_{RC}) = H_{sc}(f_{sc}) \)

\[
f_{sc} = \frac{f_c}{\pi} \sin \left( \pi \frac{f_{sc}}{f_c} \right)
\]
LDI Integration

\[ f_{SC} = \frac{f_s}{\pi} \sin \left( \pi \frac{f_{RC}}{f_s} \right) \]

- "RC" frequencies up to \( f_s/\pi \) map to physical (real) "SC" frequencies
- Frequencies above \( f_s/\pi \) do not map to physical frequencies
- Mapping is symmetric about \( f_s/2 \) (aliasing)
- "Accurate" only for \( f_{RC} \ll f_s \)

Switched Capacitor Filter
Build with LDI Integrator

\[ |H(j\omega)| \]

Zeros Preserved

- \( f_s/2 \)
- \( f_s \)
- \( 2f_s \)
- \( f \)
SC Integrator
Parasitic Sensitivity

Effect of parasitic capacitors:

1. \( C_{p1} \) - driven by opamp o.k.
2. \( C_{p2} \) - at opamp virtual gnd o.k.
3. \( C_{p3} \) – Charges to \( V_{in} \) & discharges into \( C_I \)

→ Problem parasitic sensitive
Parasitic Insensitive 
Bottom-Plate SC Integrator

Sensitive parasitic cap. $C_{p1}$ rearrange circuit so that $C_{p1}$ does not charge/discharge

$\phi 1 = 1 \rightarrow$ capacitor grounded

$\phi 2 = 1 \rightarrow$ capacitor at virtual ground

Solution: Bottom plate capacitor integrator

Bottom Plate S.C. Integrator

Input/Output z-transform
Note: Delay from Vi+ and Vi- to output is different
$\rightarrow$ Special attention needed to input/output connections

<table>
<thead>
<tr>
<th></th>
<th>Vo1 on $\phi 1$</th>
<th>Vo2 on $\phi 2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vi+ on $\phi 1$</td>
<td>$\frac{z^{-l}}{1-z^{-l}}$</td>
<td>$\frac{z^{-l/2}}{1-z^{-l}}$</td>
</tr>
<tr>
<td>Vi- on $\phi 2$</td>
<td>$\frac{z^{-l/2}}{1-z^{-l}}$</td>
<td>$\frac{-l}{1-z^{-l}}$</td>
</tr>
</tbody>
</table>
Bottom Plate S.C. Integrator
z-Transform Model

LDI Switched Capacitor Ladder Filter

Delay around integ. Loop is \((Z^{-1/2} \times Z^{1/2} = I) \Rightarrow LDI\) function
Switched Capacitor LDI Resonator

Resonator Signal Flowgraph

\[ \frac{\omega_1}{s} \]
\[ \frac{\omega_2}{s} \]

\[ \omega_1 = \frac{f_s}{R C_1} \times C_2 \]
\[ \omega_2 = \frac{f_s}{R C_3} \times C_4 \]

Fully Differential Switched Capacitor Resonator
Switched Capacitor LDI Bandpass Filter
Continuous-Time Termination

\[ \omega_0 = \frac{C_3}{C_4} = f_s \times \frac{C_1}{C_2} \]
\[ Q = \frac{C_4}{C_2} \]

Bandpass Filter
Signal Flowgraph

Switched Capacitor LDI Bandpass Filter
Continuous-Time Termination

\[ f_0 = \frac{1}{2\pi} f_s \times \frac{C_1}{C_2} \]
\[ \Delta f = \frac{f_0}{Q} \]
\[ = \frac{1}{2\pi} f_s \times \frac{C_4}{C_2 C_4} \]

Both accurately determined by cap ratios & clock frequency

Magnitude (dB)

-3dB

0

\[ f_0 \]

Frequency

\[ \Delta f \]
Fifth Order All-Pole LDI Low-Pass Ladder Filter
Complex Conjugate Terminations


Fifth Order All-Pole Low-Pass Ladder Filter
Termination Implementation

Sixth Order Elliptic LDI Bandpass Filter


Use of T-Network

High Q filter \(\rightarrow\) large cap. ratio for Q & transmission zero implementation
To reduce large ratios required \(\rightarrow\) T-networks utilized

Sixth Order Elliptic Bandpass Filter Utilizing T-Network


S.C. Resonator

Regular sampling
Each opamp busy settling only during one of the clock phases
→ Idle during the other clock phase
S.C. Resonator Using Double-Sampling

Double-sampling:

- 2nd set of switches & sampling caps added to all integrators
- While one set of switches/caps sampling the other one transfers charge into the intg. cap
- Opamps busy during both clock phases
- Effective sampling freq. twice clock freq. while opamp bandwidth stays the same

Double-Sampling Issues

Issues to be aware of:
- Jitter in the clock
- Unequal clock phases
- Mismatch in sampling caps.
  \( \rightarrow \) parasitic passbands

Double-Sampled Fully Differential S.C. 6th Order All-Pole Bandpass Filter