D/A Converters

- D/A architecture examples
  - Unit element
  - Binary weighted

- Static performance
  - Component matching
  - Architectures
    - Unit element
    - Binary weighted
    - Segmented
  - Dynamic element matching

- Dynamic performance
  - Glitches

- DAC Examples

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R-String DAC

- Advantages:
  - Simple, fast for <8-10bits
  - Inherently monotonic
  - Compatible with purely digital technologies

- Disadvantages:
  - $2^B$ resistors & $2^B$ switches for B bits → High element count & larger area for B>10bits
  - High settling time for B > 10:
    $\tau_{\text{max}} = 0.25 \times 2^B \text{RC}$

R-String DAC Including Interpolation

Resistor string DAC
Resistor string interpolator increases resolution w/o drastic increase in complexity
e.g. 6bit DAC → 3+3

Considerations:
Interpolation string loading of main R string
Large R values → less loading but lower speed
Can use buffers

Use buffers
→ Issues: offset & speed
Static DAC INL / DNL Errors

- Component matching
- Systematic errors
  - Contact resistance
  - Edge effects in capacitor arrays
  - Process gradient
  - Finite current source output resistance
- Random errors
  - Lithography
  - Often Gaussian distribution (central limit theorem)


Gaussian Distribution

\[
p(x) = \frac{1}{\sqrt{2\pi\sigma}} e^{-\frac{(x-\mu)^2}{2\sigma^2}}
\]

where standard deviation: \( \sigma = \sqrt{\text{E}(X^2) - \mu^2} \)
Yield

\[ P(-X \leq x \leq +X) = \frac{1}{\sqrt{2\pi}} \int_{-x}^{+x} e^{-\frac{x^2}{2}} dx = \text{erf} \left( \frac{X}{\sqrt{2}} \right) \]

<table>
<thead>
<tr>
<th>( X/\sigma )</th>
<th>( P(-X \leq x \leq X) ) [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.2000</td>
<td>15.8519</td>
</tr>
<tr>
<td>0.4000</td>
<td>31.0843</td>
</tr>
<tr>
<td>0.6000</td>
<td>45.1494</td>
</tr>
<tr>
<td>0.8000</td>
<td>57.6289</td>
</tr>
<tr>
<td>1.0000</td>
<td>68.2689</td>
</tr>
<tr>
<td>1.2000</td>
<td>76.9861</td>
</tr>
<tr>
<td>1.4000</td>
<td>83.8487</td>
</tr>
<tr>
<td>1.6000</td>
<td>89.0401</td>
</tr>
<tr>
<td>1.8000</td>
<td>92.8139</td>
</tr>
<tr>
<td>2.0000</td>
<td>95.4500</td>
</tr>
</tbody>
</table>
Example

- Measurements show that the offset voltage of a batch of operational amplifiers follows a Gaussian distribution with $\sigma = 2\text{mV}$ and $\mu = 0$.

- Fraction of opamps with $|V_{os}| < X = 6\text{mV}$:
  - $X/\sigma = 3 \rightarrow 99.73\%$ yield (we’d still test before shipping!)

- Fraction of opamps with $|V_{os}| < X = 400\text{\mu V}$:
  - $X/\sigma = 0.2 \rightarrow 15.85\%$ yield

Component Mismatch

Example: Two side-by-side Resistors

Large # of devices measured & curved $\rightarrow$ typically if sample size large shape is Gaussian

E.g. Let us assume in this example 1000 Rs measured & 68.5% within $\pm 4\text{OHM}$ or $+0.4\%$ of average $\rightarrow 1\sigma$ for resistors $\rightarrow 0.4\%$
Component Mismatch

Two side-by-side Resistors

\[ R = \frac{R_1 + R_2}{2} \]
\[ dR = R_1 - R_2 \]

\[ \sigma_{db}^2 \propto \frac{I}{\text{Area}} \]

For typical technologies & geometries

1\( \sigma \) for resistors \( \rightarrow \) 0.02 to 5%

In the case of resistors \( \sigma \) is a function of area

DNL Unit Element DAC

E.g. Resistor string DAC:

\[ \Delta = R_{\text{nom}} I_{\text{ref}} \]
\[ \Delta_i = R_i I_{\text{ref}} \]

\[ DNL_i = \frac{\Delta_{\text{nom}} - \Delta}{\Delta} \]
\[ = \frac{R_i - R_{\text{nom}}}{R_{\text{nom}}} \frac{dR_{\text{nom}}}{R_i} \]
\[ \sigma_{DNL} = \frac{\sigma_{dR}}{R} \]

DNL of unit element DAC is independent of resolution!
DNL Unit Element DAC

E.g. Resistor string DAC:

\[ \sigma_{DNL} = \frac{\sigma_{dR}}{R_i} \]

Example:

If \( \sigma_{dR/R} = 0.4\% \), what DNL spec goes into the datasheet so that 99.9% of all converters meet the spec?

Answer:
From table: for 99.9%
\[ \frac{X}{\sigma} = 3.3 \]
\[ \sigma_{DNL} = \sigma_{dR/R} = 0.4\% \]
\[ 3.3 \sigma_{DNL} = 1.3\% \]
\[ \rightarrow \text{DNL} = \pm 0.013 \text{ LSB} \]

DNL of unit element DAC is independent of resolution!

DAC INL Analysis

\[
\begin{array}{c|cc}
\text{Ideal} & \text{Variance} \\
A & n & n\sigma_x^2 \\
B & N-n & (N-n)\sigma_y^2 \\
\end{array}
\]

\[ E = A-n \quad r = n/N \]
\[ = A-r(A+B) \]
\[ = A(1-r) \cdot B \cdot r \]
\[ \rightarrow \text{Variance of } E: \]
\[ \sigma_E^2 = (1-r)^2 \cdot \sigma_A^2 + r^2 \cdot \sigma_B^2 \]
\[ = N \cdot r \cdot (1-r) \cdot \sigma^2 \]
\[ \rightarrow \text{Maximum @ } r = 0.5, n = N/2 \]
\[ \rightarrow \text{Max INL @ midscale} \]
**DAC INL**

\[
\sigma_E^2 = n \left( 1 - \frac{n}{N} \right) \sigma_e^2
\]

*To find max. variance:* \[ \frac{d\sigma_E^2}{dn} = 0 \]

\[ \rightarrow n = N/2 \]

- Error is maximum at mid-scale (N/2):

  \[
  \sigma_{\text{INL}} = \frac{1}{2} \sqrt{2^B - 1} \sigma_e
  \]

  *with* \[ N = 2^B - 1 \]

- INL depends on DAC resolution and element matching \( \sigma_e \)
- While \( \sigma_{\text{INL}} = \sigma_e \)

Ref: Kuboki et al, TCAS, 6/1982

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**Untrimmed DAC INL**

**Example:**

\[
\sigma_{\text{INL}} = 0.1 \text{ LSB}
\]

\[
\sigma_e = \begin{cases} 1 \% & B = 8.6 \\ 0.5 \% & B = 10.6 \\ 0.2 \% & B = 13.3 \\ 0.1 \% & B = 15.3 \end{cases}
\]
Simulation Example

- $\sigma_{\varepsilon} = 1\%$
- $B = 12$
- $\sigma_{\text{INL}} = 0.3$ LSB (midscale)

Binary Weighted DAC

- INL same as for unit element DAC
- DNL depends on transition
  - Example:
    - 0 to 1 $\Rightarrow \sigma_{\text{DNL}}^2 = \sigma_{(dI/I)}^2$
    - 1 to 2 $\Rightarrow 3\sigma_{(dI/I)}^2$
- Consider MSB transition: 0111 $\Rightarrow$ 1000 ...
MOS Device Matching

\[ I_d = \frac{I_{d1} + I_{d2}}{2} \]

\[ \frac{dI_d}{I_d} = \frac{I_{d1} - I_{d2}}{I_d} \]

\[ \frac{dI_d}{I_d} = \left[ \frac{dW/L}{W/L} \right] + \left( \frac{dV_{th}}{V_{GS}-V_{th}} \right) \]

- Current matching depends on:
  - Device ratio matching
    - Larger area less mismatch effect
  - Threshold voltage matching
    - Larger gate-overdrive less threshold voltage mismatch effect

Current-Switched DACs in CMOS

\[ \frac{dI_d}{I_d} = \left[ \frac{dW/L}{W/L} \right] + \left( \frac{dV_{th}}{V_{GS}-V_{th}} \right) \]

- Advantages:
  - Can be very fast
  - Small area for <9-10 bits

- Disadvantages:
  - Matching depends on \( V_{th} \) matching & device W/L matching

Example: 8-bit Binary Weighted
**DNL of Binary Weighted DAC**

- Worst-case transition occurs at mid-scale:
  
  \[
  \sigma_{DNL}^2 = \left( \frac{2^{B-i}-1}{2^{B-i}} \right) \sigma_x^2 + \left( \frac{2^{B-i}}{2^{B-i}} \right) \sigma_x^2
  \]
  
  \[
  \approx 2^i \sigma_x^2
  \]
  
  \[
  \sigma_{DNL_{max}} = 2^{B/2} \sigma_x
  \]
  
  \[
  \sigma_{INL_{max}} = \frac{1}{2} \sqrt{2^i - 1} \sigma_x \approx \frac{1}{2} \sigma_{DNL_{max}}
  \]

- **Example:**
  
  \( B = 12, \ \sigma_x = 1\% \)
  
  \( \sigma_{DNL} = 0.64 \) LSB
  
  \( \sigma_{INL} = 0.32 \) LSB

---

**Simulation Example**

- DNL and INL of 12 Bit converter (from converter decision thresholds)

\( \sigma_x = 1\% \)

\( B = 12 \)

\( \sigma_{DNL} = 0.6 \) LSB

(mid-scale)

MSB transitions clearly visible
“Another” Random Run …

Now (by chance) worst DNL is mid-scale.

Statistical result!

Unit Element vs Binary Weighted

Unit Element DAC
\[
\begin{align*}
\sigma_{\text{DNL}} & = \sigma_e \\
\sigma_{\text{INL}} & = 2^{\frac{1}{2}} \sigma_e
\end{align*}
\]

Binary Weighted DAC
\[
\begin{align*}
\sigma_{\text{DNL}} & \equiv 2^{\frac{N}{2}} \sigma_e = 2\sigma_{\text{INL}} \\
\sigma_{\text{INL}} & \equiv 2^{\frac{N}{2}-1} \sigma_e
\end{align*}
\]

Number of switched elements:
\[
S = 2^B
\]

Significant difference in performance and complexity!
Unit Element vs Binary Weighted DAC

**Example: B=10**

<table>
<thead>
<tr>
<th>Unit Element DAC</th>
<th>Binary Weighted DAC</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \sigma_{DNL} = \sigma_\varepsilon )</td>
<td></td>
</tr>
<tr>
<td>( \sigma_{INL} \approx 2^{\frac{B}{2}-1} \sigma_\varepsilon = 16 \sigma_\varepsilon )</td>
<td></td>
</tr>
<tr>
<td>( \sigma_{DNL} \approx 2^{\frac{B}{2}} \sigma_\varepsilon = 32 \sigma_\varepsilon )</td>
<td></td>
</tr>
<tr>
<td>( \sigma_{INL} \approx 2^{\frac{B}{2}-1} \sigma_\varepsilon = 16 \sigma_\varepsilon )</td>
<td></td>
</tr>
</tbody>
</table>

Number of switched elements:

- Unit Element DAC: \( S = 2^B = 1024 \)
- Binary Weighted DAC: \( S = B = 10 \)

*Significant difference in performance and complexity!*

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**DAC INL/DNL Summary**

- DAC architecture has significant impact on DNL
- INL is independent of DAC architecture and requires element matching commensurate with overall DAC precision
- Results are for uncorrelated random element variations
- Systematic errors and correlations are usually also important

Segmented DAC

- **Objective:**
  compromise between unit element and binary weighted DAC

- **Approach:**
  \( B_1 \) MSB bits → unit elements
  \( B_2 = B - B_1 \) LSB bits → binary weighted

- INL: unaffected
- DNL: worst case occurs when LSB DAC turns off and one more MSB DAC element turns on: same as binary weighted DAC with \( B_2 + 1 \) bits
- Number of switched elements: \( (2^{B_1} - 1) + B_2 \)

\[ \begin{array}{c|c|c|c}
\text{DAC Architecture} & \sigma_{\text{INL}[\text{LSB}]} & \sigma_{\text{DNL}[\text{LSB}]} & \# \text{s.e.} \\
\hline
\text{Unit element (10+0)} & 0.32 & 0.01 & 4095 \\
\text{Binary weighted(0+10)} & 0.32 & 0.64 & 12 \\
\text{Segmented 5+7} & 0.32 & 0.16 & 31 + 7 \\
\text{Segmented 6+6} & 0.32 & 0.113 & 63 + 6 \\
\end{array} \]
Dynamic DAC Error: Glitch

- Consider binary weighted DAC transition 011 → 100
- DAC output depends on timing
- Plot shows situation where
  - LSB/MSBs on time
  - LSB early, MSB late
  - LSB late, MSB early

Glitch Energy

- Glitch energy (worst case): $\sim dt \times 2^{B-1}$
- LSB energy: $\sim T$
- Need $dt \times 2^{B-1} \ll T$ or $dt \ll 2^{B+1} T$
- Examples:

<table>
<thead>
<tr>
<th>$f_s$ [MHz]</th>
<th>B</th>
<th>$dt$ [ps]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>12</td>
<td>$\ll 488$</td>
</tr>
<tr>
<td>20</td>
<td>16</td>
<td>$\ll 1.5$</td>
</tr>
<tr>
<td>1000</td>
<td>10</td>
<td>$\ll 2$</td>
</tr>
</tbody>
</table>
DAC Reconstruction Filter

- Need for and requirements depend on application

- Tasks:
  - Correct for sinc distortion
  - Remove “aliases” (stair-case approximation)

Reconstruction Filter Options

- Digital and SC filter possible only in combination with oversampling (signal bandwidth $B << \frac{f_s}{2}$)
- Digital filter can prewarp spectrum to compensate inband sinc attenuation (from ZOH)
Sample DAC Implementations

- Untrimmed segmented

- Current copiers:

- Dynamic element matching:
Current-Switched DACs in CMOS

\[ I_j = k(V_{GS_{j}} - V_t)^2 \]
\[ V_{G_{S_{j}}} = V_{G_{S_{j}}} - 3RI \]
\[ V_{G_{S_{j}}} = V_{G_{S_{j}}} - 5RI \]
\[ V_{G_{S_{j}}} = V_{G_{S_{j}}} - 6RI \]

\[ I_1 = k(V_{GS_{1}} - V_t)^2 = I_0 \left( 1 - \frac{3RI}{V_{GS_{1}} - V_{th}} \right)^2 \]
\[ R_m = \frac{2I_0}{V_{GS_{1}} - V_{th}} \]
\[ I_2 = I_1 \left( 1 - \frac{3RI}{2R_m} \right) = I_1 \left( 1 - \frac{3RI}{2R_m} \right) \]
\[ I_3 = I_1 \left( 1 - \frac{3RI}{2R_m} \right) = I_1 \left( 1 - \frac{3RI}{2R_m} \right) \]
\[ I_4 = I_1 \left( 1 - \frac{3RI}{2R_m} \right) = I_1 \left( 1 - 6R_m \right) \]

- Assumption: \( RI \) is small compared to transistor gate overdrive
- Desirable to have \( gm \) small

Example: 4 unit element current sources
Current-Switched DACs in CMOS

Assumption: $R_I$ is small compared to xtor gate overdrive
Desirable to have $g_m$ small

Example: 4 unit element current sources

A 10-bit 1-GSample/s Nyquist Current-Steering CMOS D/A Converter

Anne Van den Bosch, Student Member, IEEE, Marc A. F. Borremans, Student Member, IEEE, Michel S. J. Steyaert, Senior Member, IEEE, and Willy Sansen, Fellow, IEEE
A Self-Calibration Technique for Monolithic High-Resolution D/A Converters

D. WOUTER J. GROENEVELD, HANS J. SCHOUWENAARS, SENIOR MEMBER, IEEE, HENK A. H. TERMEER, AND CORNELIS A. A. BASTIAANSEN

Fig. 2. Calibration principle. (a) Calibration. (b) Operation.
Dynamic Element Matching for High-Accuracy Monolithic D/A Converters

RUDY J. VAN DE PLASCHIE

Fig. 2. (a) New current divider schematic diagram. (b) Time dependence of various currents in the new divider.
Dynamic Element Matching

During $\Phi_1$

\[ I_{11}^{(1)} = \frac{1}{2}I_o(1 + \Delta) \]
\[ I_{11}^{(2)} = \frac{1}{2}I_o(1 - \Delta) \]

During $\Phi_2$

\[ I_{11}^{(3)} = \frac{1}{2}I_o(l - \Delta) \]
\[ I_{11}^{(4)} = \frac{1}{2}I_o(l + \Delta) \]

\[ \langle I_1 \rangle = \frac{I_{11}^{(1)} + I_{11}^{(2)}}{2} = \frac{I_o(1 - \Delta) + (1 + \Delta)}{2} \]
\[ = \frac{I_o}{2} \]

\[ f_{err} = \frac{I_{11}^{(3)} - I_{11}^{(4)}}{2} \]

(a) Binary weighted current network using different switching frequencies. (b) Time dependence of currents flowing in the first and second divider stage.

(b) Error analysis results.
Dynamic Element Matching

During $\Phi_1$

\[ I_{11}^o = \frac{1}{2} I_o (1 + \Delta_1) \]
\[ I_{12}^i = \frac{1}{2} I_i (1 - \Delta_1) \]
\[ I_{11}^i = \frac{1}{2} I_{11}^o (1 + \Delta_1) = \frac{1}{2} I_o (1 + \Delta_1) (1 + \Delta_1) \]
\[ I_{12}^i = \frac{1}{2} I_{12}^o (1 - \Delta_1) = \frac{1}{2} I_i (1 - \Delta_1) (1 - \Delta_1) \]

\[ \langle I_1 \rangle = \frac{I_{11}^o + I_{12}^i}{2} = \frac{I_o}{4} (1 + \Delta_1)(1 + \Delta_1) + \frac{I_i}{4} (1 - \Delta_1)(1 - \Delta_1) \]

During $\Phi_2$

\[ I_{21}^o = \frac{1}{2} I_o (1 - \Delta_2) \]
\[ I_{22}^i = \frac{1}{2} I_i (1 + \Delta_2) \]
\[ I_{21}^i = \frac{1}{2} I_{21}^o (1 - \Delta_2) = \frac{1}{2} I_o (1 - \Delta_2) (1 - \Delta_2) \]
\[ I_{22}^i = \frac{1}{2} I_{22}^o (1 + \Delta_2) = \frac{1}{2} I_i (1 + \Delta_2) (1 + \Delta_2) \]

\[ \langle I_2 \rangle = \frac{I_{21}^o + I_{22}^i}{2} = \frac{I_o}{4} (1 - \Delta_2)(1 - \Delta_2) + \frac{I_i}{4} (1 + \Delta_2)(1 + \Delta_2) \]

E.g. $\Delta_1 = \Delta_2 = 1\% \rightarrow$ matching error is $(1\%)^2 = 0.01\%$

MOS Sampling Circuits
Re-Cap

- How can we build circuits that "sample"

Ideal Sampling

- In an ideal world, zero resistance sampling switches would close for the briefest instant to sample a continuous voltage $v_{\text{IN}}$ onto the capacitor $C$
- Not realizable!
Ideal T/H Sampling

- $V_{\text{out}}$ tracks input when switch is closed
- Grab *exact* value of $V_{\text{in}}$ when switch opens
- "Track and Hold" (T/H)

Continuous

T/H signal

(SD Signal)

Clock

DT Signal

$T = 1/f$
Practical Sampling

- kT/C noise
- Finite $R_{sw}$ → limited bandwidth
- $R_{sw} = f(V_{in})$ → distortion
- Switch charge injection (EE240)
- Clock jitter

kT/C Noise

$$\frac{k_B T}{C} \leq \frac{A^2}{12}$$

$$C \geq 12k_B T \left( \frac{2^B - 1}{V_{FS}} \right)^2$$

In high resolution ADCs kT/C noise usually dominates overall error (power dissipation considerations).

<table>
<thead>
<tr>
<th>B</th>
<th>$C_{min}$ ($V_{FS} = 1V$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>0.003 pF</td>
</tr>
<tr>
<td>12</td>
<td>0.8 pF</td>
</tr>
<tr>
<td>14</td>
<td>13 pF</td>
</tr>
<tr>
<td>16</td>
<td>206 pF</td>
</tr>
<tr>
<td>20</td>
<td>52,800 pF</td>
</tr>
</tbody>
</table>
Acquisition Bandwidth

- The resistance \( R \) of switch \( S1 \) turns the sampling network into a lowpass filter with risetime \( \tau = RC \).

- Assuming \( V_{in} \) is constant during the sampling period and \( C \) is initially discharged

\[
v_{out}(t) = v_{in}(1 - e^{-t/\tau})
\]

Switch On-Resistance

\[
V_{in} - V_{out}
\left(t = \frac{1}{2f_s}\right) \ll \Delta
\]

\[
V_{in}e^{-t/2f_s} \ll \Delta
\]

Worst Case: \( V_{in} = V_{FS} \)

\[
\tau \ll \frac{T}{2 \ln(2^B - 1)}
\]

\[
R \ll -\frac{1}{2f_sC \ln(2^B - 1)}
\]

Example:

\( B = 14 \), \( C = 13pF \), \( f_s = 100MHz \)

\( T/\tau \gg 19.4 \), \( R \ll 40\Omega \)
Switch On-Resistance

\[ I_{Ds(sink)} = \mu C_{on} \frac{W}{L} (V_{GS} - V_{TH} - \frac{V_{DS}}{2}) V_{DS} \]

\[ R_{ON} = \frac{1}{\mu C_{on} \frac{W}{L} (V_{GS} - V_{TH})} = \frac{1}{\mu C_{on} \frac{W}{L} (V_{DD} - V_{TH} - V_{in})} \]

\[ \frac{1}{R_{ON}} \equiv \frac{dI_{DS(sink)}}{dV_{DS}} \bigg|_{V_{in} \to 0} \]

for \( \frac{R_{in}}{V_{in}} = \frac{1}{\mu C_{on} \frac{W}{L} (V_{DD} - V_{TH})} \)

\[ R_{ON} = \frac{R_{in}}{V_{DD} - V_{in}} \]

Sampling Distortion

\[ V_{out} = V_{in} \left( 1 - e^{-\frac{T}{2} \left( \frac{V_{in}}{V_{DD} - V_{in}} \right)} \right) \]

10-bit ADC & \( T/\tau = 10 \)

\( V_{DD} - V_{in} = 2V \quad V_{FS} = 1V \)
Sampling Distortion

- SFDR is very sensitive to sampling distortion

- Solutions:
  - Overdesign $\rightarrow$ Larger switches
    $\rightarrow$ increased switch charge injection
  - Complementary switch
  - Maximize $V_{DD}/V_{FS}$
    $\rightarrow$ decreased dynamic range
  - Constant $V_{GS} \sim f(V_{in})$
    $\rightarrow$ ...

10-bit ADC  $T/\tau = 20$
$V_{DD} - V_{th} = 2V$  $V_{FS} = 1V$