ADC Converters

- Sampling
  - Sampling switch induced distortion
  - Sampling switch conductance dependence on input voltage
  - Sampling switch charge injection
    - Complementary switch
    - Use of dummy device
    - Bottom-plate switching
  - Track & hold circuit
  - S/H circuit incorporating gain

- ESD protection impact on converter performance

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Practical Sampling

- $k T / C$ noise
  \[
  C \geq 12 k_T T \left[ \frac{2^h - 1}{V_{FS}} \right]^2
  \]

- Finite $R_{sw}$ → limited bandwidth
  \[
  R \ll -\frac{1}{2f C \ln(2^h - 1)}
  \]

- $g_{sw} = f(V_{in})$ → distortion
  \[
  g_{ON} = g_o \left( 1 - \frac{V_m}{V_{DD} - V_{th}} \right)
  \text{ for } g_o = \mu C_m \frac{W}{L} (V_{DD} - V_{th})
  \]

- Switch charge injection
- Clock jitter
Sampling Distortion

10bit ADC & $T/\tau = 10$
$V_{DD} - V_{th} = 2V$  $V_{FS} = 1V$

$V_{DD} - V_{th} = 4V$  $V_{FS} = 1V$

- Effect of lower supply voltage on sampling distortion
  - HD3 increases by $(V_{DD1}/V_{DD2})^2$
  - HD2 increases by $(V_{DD1}/V_{DD2})$

Sampling Distortion

- SFDR is sensitive to sampling distortion to improve distortion
  - Larger VDD
  - Higher sampling bandwidth

- Solutions:
  - Overdesign → Larger switches
    → Increased switch charge injection
    → Increased nonlinear S&D junction C
  - Maximize VDD/VFS
    → Decreased dynamic range if VDD const.
  - Complementary switch
  - Constant & max. $V_{GS}$? $f(V_{GS})$

$10bit$ $ADC$  $T/\tau = 20$
$V_{DD} - V_{th} = 2V$  $V_{FS} = 1V$
Complementary Switch

- Complementary n & p switch advantages:
  - Increases the overall conductance
  - Linearize the switch conductance for the range $V_{tp} < V_{in} < V_{dd} - V_{tn}$

Complementary Switch Issues
Supply Voltage Evolution

- Supply voltage scales down with technology scaling
- Threshold voltages do not scale accordingly

**Complementary Switch**

**Effect of Supply Voltage Scaling**

- As supply voltage scales down input voltage range for constant $g_o$ shrinks
- Complementary switch not effective when $V_{dd}$ becomes comparable to $V_{in}$.

**Boosted & Constant $V_{GS}$ Sampling**

- Increase gate overdrive voltage as much as possible + keep $V_{GS}$ constant
  - Switch overdrive voltage is independent of signal level
  - Error from finite $R_{ON}$ is linear (to first order)
  - Lower $R_{on}$ achieved $\rightarrow$ lower time constant
Constant $V_{GS}$ Sampling

![Diagram of Constant $V_{GS}$ Sampling]

Constant $V_{GS}$ Sampling Circuit

![Diagram of Constant $V_{GS}$ Sampling Circuit]
Clock Voltage Doubler

Clock Voltage Doubler

Constant $V_{GS}$ Sampler: $\Phi$ LOW

- Sampling switch M11 is OFF
- C3 charged to VDD

Constant $V_{GS}$ Sampler: $\Phi$ LOW

\[ \text{Input voltage source} \]
**Constant \( V_{GS} \) Sampler: \( \Phi \) HIGH**

- C3 previously charged to VDD
- M8 & M9 are on: C3 across G-S of M11
- M11 on with constant VGS = VDD

**Constant \( V_{GS} \) Sampling**
Complete Circuit


Advanced Clock Boosting

Advanced Clock Boosting

- Gate tracks average of input and output, reduces effect of I-R drop at high frequencies
- Bulk also tracks signal ⇒ reduced body effect (technology used allows connecting bulk to S)
- SFDR = 76.5dB at f_{in}=200MHz (measured)

Switch Off-Mode Feedthrough Cancellation

- High-pass feedthrough paths past an open switch
- Feedthrough cancellation with a dummy switch

Practical Sampling

• $R_{SW} = f(V_{in}) \rightarrow$ distortion
• Switch charge injection

Sampling Switch Charge Injection

• First assume $V_{IN}$ is a DC voltage
• When switch turns off $\rightarrow$ offset voltage induced on $C_s$
• Why?
Sampling
Switch Charge Injection

MOS xtor operating in triode region
Cross section view

Distributed channel resistance &
gate & junction capacitances

- Channel \( \rightarrow \) distributed RC network
- Channel to substrate junction capacitance \( \rightarrow \) distributed & variable
- Over-lap capacitance \( C_{ov} = L_D W C_{ov} \) associated with GS & GD overlap

Switch Charge Injection
Slow Clock

- Since clock fall time \( \gg \) device speed
  → During the period \((t- \rightarrow t_{off})\) current in channel discharges channel charge
  into source
- Only source of error → Charge transfer from \( C_{ov} \) into \( C_s \)
Switch Charge Injection
Slow Clock

\[ \Delta V = -\frac{C_{ov}}{C_{ov} + C_s} (V_i + V_{th} - V_L) \]

\[ = -\frac{C_{ov}}{C_s} (V_i + V_{th} - V_L) \]

\[ V_o = V_i \left( 1 + \varepsilon \right) + V_{os} \]

where \( \varepsilon = \frac{C_{ov}}{C_s} \), \( V_{os} = -\frac{C_{ov}}{C_s} (V_{th} - V_L) \)

Switch Charge Injection
Slow Clock - Example

\[ C_{in} = 0.3fF / \mu \quad C_{os} = 5fF / \mu^2 \quad V_{th} = 0.5V \]

\[ \varepsilon = -\frac{C_{os}}{C_s} = \frac{12 \mu \times 0.3fF / \mu}{1pF} = -0.36 \% \rightarrow 7-bit \]

\[ V_{os} = -\frac{C_{ov}}{C_s} (V_{th} - V_L) = -1.8mV \]
Switch Charge Injection
Fast Clock

- Sudden gate voltage drop $\rightarrow$ no gate voltage to establish current in channel $\rightarrow$
  channel charge has no choice but to escape out towards S & D

\[ \Delta V = \frac{C_{ov}}{C_{ov} + C_s} (V_G - V_{th}) - \frac{1}{2} \frac{Q_s}{C_t} \]

\[ V_s = V(t+\epsilon)+V_{in} \]

where $\epsilon = \frac{1}{2} \frac{WC_{ov}L}{C_s}$

\[ V_s = \frac{C_{ov}}{C_s} (V_G - V_{th}) - \frac{1}{2} \frac{WC_{ov}L(V_G - V_{th})}{C_t} \]

- Assumption $\rightarrow$ channel charge divided between S & D 50% & 50%
- Source of error $\rightarrow$ channel charge transfer + charge transfer from $C_{ov}$ into $C_t$
Switch Charge Injection
Fast Clock- Example

\[ C_w = 0.31 F/\mu \quad C_s = 5 F/\mu^2 \quad V_{th} = 0.5 V \quad V_{IN} = 3V \]

\[ \epsilon = \frac{W L C_w}{C_s} \frac{12 \mu \times 0.35 \times 5 F/\mu}{1 pF} = -2.1\% \to 4.5-bit \]

\[ V_{on} = \frac{C_w}{C_s} (V_H - V_L) \frac{1}{2} \frac{W C_w L (V_H - V_L)}{C_s} = -9 mV - 26.3 mV = -45.3 mV \]

Both errors are a function of clock fall time, input voltage level, source impedance & sampling capacitance.
Switch Charge Injection Error Reduction

- How do we reduce the error?
  - Reduce size switch?

\[ \tau = \frac{C_s}{\mu C_{inv} W L (V_{ Gates} - V_{th})} \]

\[ \Delta V_s = -\frac{1}{2} \frac{Q_\Delta}{C_s} \]

\[ FOM = \tau \times \Delta V_s = \frac{C_s}{\mu C_{inv} W L (V_{ Gates} - V_{th})} \times \frac{1}{2} \frac{W C_{inv} L (V_{ th} - V_{ th})}{C_s} \]

\[ FOM = \frac{L^2}{\mu} \]

→ Reducing switch size increases \( \tau \) → increased distortion → not a viable solution

→ Small \( \tau \) and \( \Delta V \) → use minimum channel length

→ For a given technology \( \tau \times \Delta V = \text{conts.} \)

Sampling Switch Charge Injection Summary

- Extra charge injected onto sampling capacitor @ switch device turn-off
  - Charge sharing with \( C_{OV} \)
  - Channel charge transfer

- Issues:
  - DC offset
  - Input dependant error voltage → distortion

- Solutions:
  - Complementary switch?
  - Addition of dummy switches?
  - Bottom-plate sampling?
Switch Charge Injection
Complementary Switch

• In slow clock case if area of devices are equal → effect of overlap capacitor for n & p devices cancel to first order (matching n & p area)

\[
Q_{b-n} = W_n C_o I_n (V_{H} - V_L - V_{th,n})
\]
\[
Q_{b-p} = W_p C_o I_p (V_{L} - V_H - V_{th,p})
\]
\[
\Delta V_o = \frac{I}{2} \left( \frac{Q_{b-p}}{C_o} - \frac{Q_{b-n}}{C_o} \right)
\]
\[
V_o = V_H (1 + \varepsilon) + V_{th}
\]
\[
\varepsilon = \frac{I}{2} \times \frac{W_n C_o I_n + W_p C_o I_p}{C_o}
\]

• In fast clock case
  • Offset cancelled for equal device area
  • Input voltage dependant error worse!

Switch Charge Injection
Complementary Switch

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Switch Charge Injection Dummy Switch

- Dummy switch same L and main switch but half W
- Main device clock goes low, dummy device goes high → dummy switch acquires same amount of channel charge main switch needs to lose
- Effective only if exactly half of the charge transferred to M2 and good matching between clock fall/rise

\[ W_{M2} = \frac{1}{2} W_{M1} \]

Switch Charge Injection Dummy Switch

- To guarantee half of charge goes to each side → create the same environment on both sides
  - Add \( C \) equal to sampling capacitor to the other side of the switch + add fixed resistor
  - Degrades sampling bandwidth

\[ R \]
Dummy Switch

Dummy Switch Effectiveness Test

- Dummy switch \( \Rightarrow W = \frac{1}{2} W_{\text{main}} \)
- Note large Ls \( \Rightarrow \) good device area matching

\[ \begin{array}{|c|c|c|c|}
\hline
V_{\text{in}} & \text{UNCOMPENSATED SWITCH} & \text{COMPENSATED WITH DUMMY SWITCH} & \text{BALANCED SWITCH} \\
\hline
0 \text{V} & -160 \text{mV} & -45 \text{mV} & 6 \text{mV} \\
5 \text{V} & -105 \text{mV} & -30 \text{mV} & 1 \text{mV} \\
10 \text{V} & -40 \text{mV} & -11 \text{mV} & 0.5 \text{mV} \\
\hline
\end{array} \]


Switch Charge Injection

Bottom Plate Sampling

- Switches M2A@ B are opened slightly earlier compared to M1A&B
  \( \Rightarrow \) Injected charge by the opening or M2AB is constant & eliminated when used differentially

- Since bottom plate of \( C_s \) is open when M1A&B are opened \( \Rightarrow \) no charge injected on \( C_s \)
Flip-Around T/H

- Concept based on bottom-plate sampling
Flip-Around T/H

Flip-Around T/H - Timing

S1 opens early to sample the input “Bottom Plate Sampling”
Charge Injection

- At the instant of sampling, some of the charge stored in sampling switch S1 is dumped onto C.
- With "Bottom Plate Sampling", charge injection comes only from S1 and is to first-order independent of $v_{IN}$:
  - Only a dc offset is added to the input signal.
  - This dc offset can be removed with a differential architecture.

Flip-Around T/H

- Constant switch $V_{GS}$ to minimize distortion.

Flip-Around T/H

- S1 is an n-channel MOSFET
- Since it always switches the same voltage, its on-resistance, $R_{S1}$, is signal-independent (to first order)
- Choosing $R_{S1} >> R_{S1A}$ minimizes the non-linear component of $R = R_{S1A} + R_{S1}$
  - $S1A$ is a wide (much lower resistance than S1) constant $V_{GS}$ switch
  - In practice size of S1A is limited by the (nonlinear) S/D capacitance that also adds distortion
  - If S1A’s resistance is negligible, aperture delay depends only on S1 resistance
  - S1 resistance is independent of $V_{IN}$; hence, aperture delay is independent of $V_{IN}$
S/H Combined with Gain Stage

- Gain = 4Cl/Ci = 4

S/H Combined with Gain Stage

- Gain = \(4C/C = 4\)


ESD Protection

ADC Architectures
What is ESD?

- Electrostatic discharge
- Example: Charge built up on human body while walking on carpet...
- Charged objects near or touching IC pins can discharge through on-chip devices
- Without dedicated protection circuitry, ESD events are destructive

Model and Protection Circuit

Figure 1. Human Body Model for ESD testing. [http://www.idt.com/docs/AN_123.pdf]

[http://www.ce-mag.com/archive/03/ARG/dunnihoo.html]
Equivalent Circuit

- Nonlinear capacitance causes distortion
- Distortion increases with frequency
  - Today's converters: High frequency, low distortion!

[Fig. 1. Equivalent input circuit.]

ESD Circuit Distortion

\[ C(V_{in}) = 2.4 \text{pF} \]

for \( V_{in} = 2.0 \text{V} \)

ESD Circuit Distortion

• Analysis: Volterra Series (see handout on the web)

• Example:

\[ R = 25\, \Omega \]
\[ C_{j} = 1\, \text{pF} \]
\[ C_{L} = 5\, \text{pF} \]
\[ V_{\text{peak}} = 0.5\, \text{V} \]
ESD Circuit Distortion

- Distortion from ESD circuits approaches state of-the-art ADC performance!
- If you are working on a new, record breaking ADC, better think about ESD now...
- Solutions still pre-mature
- Lots of company IP