EE247
Lecture 18

ADC Converters

– Sampling switch charge injection
  • Bottom plate sampling
  • Flip around track & hold
  • Sample and hold including gain
  • Sample and hold including offset cancellation
– Impact of ESD protection on converters
– ADC architectures

Sampling Switch Charge Injection

Summary

• Extra charge injected onto sampling capacitor @ switch device turn-off
  – Charge sharing with $C_{ov}$
  – Channel charge transfer
• Issues:
  – DC offset
  – Input dependant error voltage $\rightarrow$ distortion
• Solutions:
  – Complementary switch $\rightarrow$ only cancels offset, does not address input signal dependant error
  – Addition of dummy switches $\rightarrow$ cancels charge injection to $1^{st}$ order but not fully
  – Bottom-plate sampling?
Switch Charge Injection
Bottom Plate Sampling

- Switches M2A@B are opened slightly earlier compared to M1A&B
  → Injected charge by the opening or M2AB is constant & eliminated when used differentially
- Since bottom plate of C_s is open when M1A&B are opened → no charge injected on C_s

Flip-Around T/H

- Concept based on bottom-plate sampling
Flip-Around T/H

Charging C

Flip-Around T/H

Holding
Charge Injection

- At the instant of sampling, some of the charge stored in sampling switch S1 is dumped onto C.
- With "Bottom Plate Sampling", charge injection comes only from S1 and is to first-order independent of $v_{\text{IN}}$.
  - Only a dc offset is added to the input signal.
  - This dc offset can be removed with a differential architecture.
Flip-Around T/H

Constant switch $V_{GS}$ to minimize distortion

Small Nch-only

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Flip-Around T/H

- S1 is an n-channel MOSFET
- Since it always switches the same voltage, its on-resistance, $R_{S1}$, is signal-independent (to first order)
- Choosing $R_{S1} \gg R_{S1A}$ minimizes the non-linear component of $R = R_{S1A} + R_{S1}$
  - S1A is a wide (much lower resistance than S1) constant $V_{GS}$ switch
  - In practice size of S1A is limited by the (nonlinear) S/D capacitance that also adds distortion
  - If S1A’s resistance is negligible $\rightarrow$ delay depends only on S1 resistance
  - S1 resistance is independent of $v_{IN}$ $\rightarrow$ delay is independent of $v_{IN}$

Differential Flip-Around T/H

Differential Flip-Around T/H

- Gain = 1
- Feedback factor = 1
- $\Delta V_{in-cm} = V_{out_com} - V_{sig_com}$

$\Rightarrow$ Amplifier needs to have large input common-mode compliance

Choice of Sampling Switch Size


- THD simulated w/o sampling switch boosted clock $\rightarrow$ -45dB
- THD simulated with sampling switch boosted clock (see figure)
Input Common-Mode Cancellation


Track mode (φ high)
\[ V_{C1} = V_{I1}, \; V_{C2} = V_{I2}, \; V_{o1} = V_{o2} = 0 \]

Hold mode (φ low)
\[ V_{o1} + V_{o2} = 0, \; V_{o1} - V_{o2} = -(V_{I1} - V_{I2})(C_1/(C_1 + C_2)) \]

→ Input common-mode level removed
S/H + Charge Redistribution Amplifier

Track mode ($S1, S3 \rightarrow on \rightarrow S2 \rightarrow off$)
$V_{C1} = V_{os} - V_{IN}$, $V_{C2} = 0$
$V_o = V_{os}$

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S/H + Charge Redistribution Amplifier Cont’d

$V_{C1} \rightarrow V_{os}$
$\Delta V_{C1} = V_{os} - (V_{os} - V_{IN}) = V_{IN}$
$\Delta Q_1 = C_1 \Delta V_{C1} = C_1 V_{IN}$
$\Delta Q_2 = C_2 \Delta V_{C2} = \Delta Q_1$
$\Delta V_{C2} = \left[ \frac{C_1}{C_2} \right] V_{C1} = V_{C2}$
$V_o = V_{C2} + V_{os} = \left( \frac{C_1}{C_2} \right) V_{IN} + V_{os}$

Hold/amplify mode ($S1, S3 \rightarrow off \rightarrow S2 \rightarrow on$)

$\Delta Q_1$, $\Delta Q_2$, $\Delta V_{C2}$

$V_{os}$, $V_o$

→ Offset NOT cancelled, but not amplified
→ Input-referred offset $= (C_2/C_1) \times V_{os}$, & $C_2 < C_1$
S/H & Input Difference Amplifier

Sample mode (S1, S3 → on S2 → off)
\[ V_{C1} = V_{os} - V_{I1}, \quad V_{C2} = 0 \]
\[ V_o = V_{os} \]

Input Difference Amplifier Cont’d

Cont’d Subtract/Amplify mode (S1, S3 → off S2 → on)

During previous phase:
\[ V_{C1} = V_{os} - V_{I1}, \quad V_{C2} = 0 \]
\[ V_o = V_{os} \]

\[ V_{C1} = V_{os} - V_{I2} \]
\[ \Delta V_{C1} = (V_{os} - V_{I2}) - (V_{os} - V_{I1}) = V_{I1} - V_{I2} \]
\[ \Delta V_{C2} = \left( \frac{C_2}{C_1} \right) \Delta V_{C1} = \left( \frac{C_2}{C_1} \right) (V_{I1} - V_{I2}) \]
\[ V_o = \left( \frac{C_1}{C_2} \right) (V_{I1} - V_{I2}) + V_{os} \]

→ Offset NOT cancelled, but not amplified
→ Input-referred offset = \((C_2/C_1)\)x\(V_{OS}\) & \(C_2 < C_1\)
S/H & Summing Amplifier

Sample mode (S1, S3, S5 \(\rightarrow\) on S2, S4 \(\rightarrow\) off)
\[ V_{C1} = V_{os} - V_{I1}, \quad V_{C2} = V_{os} - V_{I3}, \quad V_{C3} = 0 \]
\[ V_o = V_{os} \]
S/H & Summing Amplifier Cont’d

Amplify mode \((S1, S3, S5 \rightarrow \text{off}, \ S2, S4 \rightarrow \text{on})\)

\[
\begin{align*}
V_{C1} &= V_{in} - V_{in} = \Delta V_{C1} = V_{in} - V_{in} \\
V_{C2} &= V_{in} - V_{in} = \Delta V_{C2} = V_{in} - V_{in} \\
\Delta V_{C3} &= \Delta V_{C1} + \Delta V_{C2} = C_{1}V_{C1} + C_{2}V_{C2} \\
\Delta V_{C3} &= \Delta V_{C1} + \Delta V_{C2} = C_{1}V_{C1} + C_{2}V_{C2} \\
V_{o} &= \left( C_{1} \right) \left( V_{in} - V_{in} \right) + \left( C_{2} \right) \left( V_{in} - V_{in} \right) + V_{in}
\end{align*}
\]

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Differential S/H Combined with Gain Stage

Differential S/H Combined with Gain Stage

- Gain = $4C/C = 4$
- Feedback factor = $1/(1+G) = 0.2$
- Input common-mode level removed
- Amplifier offset not removed

Differential S/H Including Offset Cancellation

- Operation during offset cancellation shown
- Auxiliary inputs added with $A_{aux}/A_{main}=10$
- During offset cancellation phase $AZ$ and $S1$ closed $\rightarrow$ main amplifier offset stored on $C_{AZ}$
- Auxiliary amp chosen to have lower gain so that aux. amp offset & charge injection associated with opening of switch $AZ$ $\rightarrow$ reduced by $A_{aux}/A_{main}=1/10$
- Requires an extra auto-zero clock phase


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Differential S/H Including Offset Cancellation

- Operational amplifier $\rightarrow$ dual input folded-cascode opamp
- M3,4 auxiliary input, M1,2 main input
- To achieve $1/10$ gain ratio $W_{M3,4}=1/10x W_{M1,2}$ & current sources are scaled by $1/10$
- M5,6,7 $\rightarrow$ common-mode control
- Output stage $\rightarrow$ dual cascode $\rightarrow$ high DC gain

ESD Protection
ADC Architectures

What is ESD?

- Electrostatic discharge
- Example: Charge built up on human body while walking on carpet...
- Charged objects near or touching IC pins can discharge through on-chip devices
- Without dedicated protection circuitry, ESD events are destructive
Model and Protection Circuit

[Diagram of a model and protection circuit]

Equivalent Circuit

- Nonlinear capacitance causes distortion
- Distortion increases with frequency
  - Today's converters: High frequency, low distortion!

[Diagram of an equivalent circuit]

ESD Circuit Distortion

- Analysis:
  - Model nonlinear cap & run SPICE
  - Hand calculations using Volterra Series
- Example:

\[ C(V_{in}) = 2.4\, \text{pF} \]
for \( V_{in} = 2.0\, \text{V} \)
ESD Circuit Distortion

- Distortion from ESD circuits approaches state-of-the-art ADC performance!
- If you are working on a new, record breaking ADC, better think about ESD now...
- Solutions still pre-mature
- Lots of company IP
ADC Architectures

- Slope Converters
- Successive approximation
- Flash
- Folding
- Time-interleaved / parallel converter
- Residue type ADCs
  - Two-step
  - Pipeline
  - Algorithmic
  - …
- Oversampled ADCs

Single Slope ADC

- Low complexity
- Hard to generate precise ramp
- Better: Dual Slope, Multi-Slope
**Dual Slope ADC**

Integrate $V_{in}$ for fixed time, de-integrate with $V_{ref}$ applied \( \rightarrow T_{De-Int} \sim \frac{V_{in}}{V_{ref}} \)

- Insensitive to most linear error sources

**Successive Approximation**

- Binary search over DAC output
- High accuracy achievable (16+ Bits)
- Moderate speed proportional to B (MHz range)
Flash Converter

- Very fast: only 1 clock cycle per conversion
- High complexity: $2^B - 1$ comparators
- High input capacitance

Folding Converter

- Significantly fewer comparators than flash
- Fast
- Nonidealities in folder limit resolution to ~10 Bits
Time Interleaved Converter

- Extremely fast: Limited by speed of S/H
- Accuracy limited by mismatch in individual ADCs (timing, offset, gain, …)

Residue Type ADC

- Quantization error output (“residuum”) enables cascading for higher resolution
- Great flexibility for stages: flash, oversampling ADC, …
- Optional S/H enables parallelism (pipelining)
- Fast: one clock per conversion (with S/H), latency
**Pipelined ADC**

- Approaches speed of flash, but much lower complexity
- One clock per conversion, but K clocks latency
- Efficient digital calibration possible
- Versatile: from 16 Bits / 1 MS/s to 14 Bits / 100 MS/s

**Algorithmic ADC**

- Essentially same as pipeline, but a single stage is used for all partial conversions
- K clocks per conversion
Oversampled ADC

- Hard to comprehend … “easy” to build
- Input is oversampled (M times faster than output rate)
- Reduces Anti-Aliasing filter requirements and capacitor size
- Accuracy independent of component matching
- Very high resolution achievable (> 20 Bits)

![Oversampled ADC Diagram]

Throughput Rate Comparison

<table>
<thead>
<tr>
<th>Resolution [Bit]</th>
<th>Clock Cycles per Conversion</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flash, Pipeline-1 to 2</td>
<td></td>
</tr>
<tr>
<td>Successive Approximation-2</td>
<td></td>
</tr>
<tr>
<td>Oversampled-2^e</td>
<td></td>
</tr>
<tr>
<td>Serial-2^e</td>
<td></td>
</tr>
</tbody>
</table>

![Throughput Rate Comparison Graph]
Speed-Resolution Map

[www.v-corp.com]