ADC Converters
- ADC architectures
- Comparator architectures
  - High gain amplifier with differential analog input & single-ended large swing output
  - Latched comparators; in response to a strobe, input stage disabled & digital output stored in a latch till next strobe
  - Sample-data comparators
    - Offset cancellation

ADC Architectures
- Slope Converters
- Successive approximation
- Flash
- Folding
- Time-interleaved / parallel converter
- Residue type ADCs
  - Two-step
  - Pipeline
  - Algorithmic
  - ...
- Oversampled ADCs
Residue Type ADC

- Quantization error output ("residuum") enables cascading for higher resolution
- Great flexibility for stages: flash, oversampling ADC, ...
- Optional S/H enables parallelism (pipelining)
- Fast: one clock per conversion (with S/H), latency

Pipelined ADC

- Approaches speed of flash, but much lower complexity
- One clock per conversion, but K clocks latency
- Efficient digital calibration possible
- Versatile: from 16Bits / 1MS/s to 14Bits / 100MS/s
Algorithmic ADC

- Essentially same as pipeline, but a single stage is used for all partial conversions
- K clocks per conversion

Oversampled ADC

- Hard to comprehend … “easy” to build
- Input is oversampled (M times faster than output rate)
- Reduces Anti-Aliasing filter requirements and capacitor size
- Accuracy independent of component matching
- Very high resolution achievable (> 20 Bits)
Throughput Rate Comparison

![Throughput Rate Comparison Graph]

Speed-Resolution Map

![Speed-Resolution Map Graph]

[www.v-corp.com]
High-Speed A/D Converters

• Flash Converter
  – Comparator design considerations
  – Binary Encoder
• Interpolation
• Folding
• Pipelined ADCs

Flash Converter

• Very fast: only 1 clock cycle per conversion
• High complexity: $2^B - 1$ comparators
• High input capacitance
Voltage Comparators

Function: compare the instantaneous value of two analog signals

Important features:
- Maximum clock rate \( f_s \) → settling time, slew rate, small signal bandwidth
- Resolution → gain, offset
- Overdrive recovery
- Input capacitance (and linearity!)
- Power dissipation
- Common-mode rejection
- Kickback noise
- ...

Ref: Prof. B. Wooley, Course notes EE315 Stanford University
Comparators w/ High-Gain Amplification

Amplify $V_{in}(\text{min})$ to $V_{DD}$
$V_{in}(\text{min})$ determined by ADC resolution

Example: 12-bit res. & full-scale input $2V \rightarrow 1\text{LSB}=0.5\text{mV}$

$A = \frac{2.5V}{0.25mV} = 10,000$
$V_{os} < 1 \text{ LSB}$

For 2.5V output:

$\rightarrow$ Cascade of lower gain stages to broadband response

$f_u = 10$-$1000\text{MHz}$

$f_0 = \frac{1\text{GHz}}{10,000} = 100\text{kHz}$
$
\tau_0 = \frac{1}{2\pi f_0} = 1.6\mu\text{sec}$

Too slow!
$\rightarrow$ Cascade of lower gain stages to broadband response
Open Loop Cascade of Amplifiers

For 1-stage only:

\[ |A_v(0)| = g_m R_L \]

\[ \omega_o = -3 \text{dB frequency} = \frac{1}{R_L C_T} \]

\[ \omega_u = -\text{unity gain frequency} = \frac{g_m}{C_T} \]

\[ \omega_u = \frac{\omega_o}{|A_v(0)|} \]

For Cascade of N-stages:

\[ A_v(z) = [A_v(z)]^N \]

Define

\[ \omega_{3dB} = -3 \text{dB frequency of the N-stage cascade} \]

Then

\[ |A_v(z)| = |A_v(0)|^{N-1} \]

and

\[ \omega_{3dB} = \frac{\omega_u}{2^{N-1}} \]

For a specified \( |A_v(0)| \):

\[ |A_v(0)| = \left| A_v(0) \right|^{1/N} \]

\[ \Rightarrow \omega_{3dB} = \frac{\omega_u}{2^{N-1}} \left| A_v(0) \right|^{1/N} \]

Thus,

\[ \frac{\omega_{3dB}}{\omega_u} = \left| A_v(0) \right|^{1/N} \]

\[ \left( \frac{\omega_{3dB}}{\omega_u} \right)^{N-1} = \left| A_v(0) \right|^{(N-1)/N} \]
Open Loop Cascade of Amplifiers

For $|A_T(\text{DC})| = 10,000$

<table>
<thead>
<tr>
<th>$N$</th>
<th>$A_T(0)$</th>
<th>$A_T^0$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>10,000</td>
</tr>
<tr>
<td>2</td>
<td>64</td>
<td>100</td>
</tr>
<tr>
<td>3</td>
<td>236</td>
<td>21.5</td>
</tr>
<tr>
<td>4</td>
<td>435</td>
<td>10</td>
</tr>
<tr>
<td>5</td>
<td>611</td>
<td>6.3</td>
</tr>
<tr>
<td>10</td>
<td>1067</td>
<td>2.5</td>
</tr>
<tr>
<td>20</td>
<td>1185</td>
<td>1.6</td>
</tr>
</tbody>
</table>

Example:

$N = 3$, $f_a = 1\, \text{GHz}$, $A_T(0) = 10000$

$f_{0N} = \frac{1\, \text{GHz}}{(10,000)^{\frac{1}{3}}} \sqrt{2\frac{1}{3} - 1} \approx 24\, \text{MHz}$

$\tau_{0N} = \frac{1}{2\pi f_{0N}} = 7\, \text{ns}$ (1.6\,\mu s for 1-stage)

$5\tau_{0N} = 35\, \text{ns}$

Cascade of 3-stage
→ speed 236 higher compared to 1-stage (constant overall gain & $f_a$)

Open Loop Cascade of Amplifiers
Offset Voltage

- Cascade of amplifiers
  → Input-referred offset increases
- Choice of # of stages important
  → Speed vs offset tradeoff

Example:
For 3-stage case with gain/stage ~22
→ Increase in offset ~ 4.5%
Open Loop Cascade of Amplifiers

Step Response

• Assuming linear behavior

\[
\begin{align*}
V_{e1} &= \frac{1}{C_0} \int g_m V_{in} dt = g_m \frac{1}{C} V_{in} t \\
V_{e2} &= \frac{1}{C_0} \int g_m V_{e1} dt = g_m \frac{1}{C} \int V_{in} dt - \frac{1}{2} g_m V_{in}^2 t \\
V_{e3} &= \frac{1}{C_0} \int g_m V_{e2} dt = g_m \frac{1}{C} \int \left( \frac{1}{2} g_m V_{in}^2 \right) dt \\
&= \frac{1}{3} g_m \frac{1}{C} V_{in}^2 t^2
\end{align*}
\]

N Stages

\[
V_{eN} = \frac{g_m N^2}{C N} V_{in}
\]

For the output to reach a specified \(V_{out}\) (i.e., \(V_{eN} = V_{out}\)) the delay is

\[
\tau_p = \frac{C}{g_m} \left( N V_{out} \right)^{-\frac{1}{N}}
\]
Open Loop Cascade of Amplifiers

$\text{Delay}/(C/g_m)$

- Minimum total delay broad function of $N$
- Relationship between # of stages that minimize delay ($N_{op}$) and gain ($V_{out}/V_{in}$) approximately:

$$N_{op} = 1.1 \ln(V_{out}/V_{in}) + 0.79$$

for gain < 1000

- Or gain of 10dB (sqrt10) per stage results in near optimum delay


Offset Cancellation

- Disadvantage of using cascade of amplifiers:
  - Increased overall input-referred offset
- Sampled-data cascade of amplifiers $V_{os}$ can be cancelled
  - Store on ac-coupling capacitors in series with amplifier stages
- Offset associated with a specific amplifier can be cancelled by storing it in series with either the input or the output of that stage
Offset Cancellation
Output Series Cancellation

• Amp modeled as ideal + $V_{os}$ (input referred)

• Store offset:
  • S1, S4 → open
  • S2, S3 → closed
  $\Rightarrow V_C = A V_{os}$

Amplify:
• S1, S4 → closed
• S2, S3 → open
  $\Rightarrow V_C = A V_{os}$

Circuit requirements:
• Amp not saturate during offset storage
• High-impedance (C) load $\Rightarrow C_c$ not discharged
• $C_c \gg C_L$ to avoid attenuation
• $C_c \gg C_{switch}$ offset due to charge injection
Offset Cancellation
Cascaded Output Series Cancellation

1. S1 open, S2, 3, 4, 5 closed

\[ V_{C1} = A_1 \times V_{os1} \]
\[ V_{C2} = A_2 \times V_{os2} \]
\[ V_{C3} = A_3 \times V_{os3} \]
Offset Cancellation
Cascaded Output Series Cancellation

2- $S_3 \to$ open
•Feedthrough from $S_3 \to$ offset on $X$
•Switch offset, $\varepsilon_2$ stored on $C_1$
•Since $S_4$ remains closed, offset associated with $\varepsilon_2 \to$ stored on $C_2$

\[
\begin{align*}
V_X &= \varepsilon_2 \\
V_{C_1} &= A_1 \times V_{os1} \cdot \varepsilon_2 \\
V_{C_2} &= A_2 \times (V_{os2} + \varepsilon_2)
\end{align*}
\]

Offset Cancellation
Cascaded Output Series Cancellation

3- $S_4 \to$ open
•Feedthrough from $S_4 \to$ offset on $Y$
•Switch offset, $\varepsilon_3$ stored on $C_2$
•Since $S_5$ remains closed, offset associated with $\varepsilon_3 \to$ stored on $C_3$

\[
\begin{align*}
V_Y &= \varepsilon_3 \\
V_{C_2} &= A_2 \times (V_{os2} + \varepsilon_2) \cdot \varepsilon_3 \\
V_{C_3} &= A_3 \times (V_{os3} + \varepsilon_3)
\end{align*}
\]
Offset Cancellation
Cascaded Output Series Cancellation

4. S2 $\rightarrow$ open, S1 $\rightarrow$ closed, S5 $\rightarrow$ open

- S1 closed & S2 open $\rightarrow$ since input connected to low impedance source charge injection not of major concern
- Switch offset, $\epsilon_4$ introduced due to S5 opening
  - $\epsilon_4$ not cancelled
  - As shown in the following analysis, $\epsilon_4$ referred to the input will be attenuated by the overall gain

\[
V_X = A_1(V_{in} + V_{os1}) - V_{C1}
= A_1(V_{in} + V_{os1}) - (A_1 V_{os1} - \epsilon_2)
= A_1 V_{in} + \epsilon_2
\]
\[
V_Y = A_2(V_X + V_{os2}) - V_{C2}
= A_2(A_1 V_{in} + \epsilon_2 + V_{os2}) - [A_2(V_{os2} + \epsilon_2) - \epsilon_3]
= A_1 A_2 V_{in} + \epsilon_3
\]
\[
V_{out} = A_3(V_Y + V_{os3}) - V_{C3}
= A_3(A_1 A_2 V_{in} + \epsilon_3 + V_{os3}) - [A_3(V_{os3} + \epsilon_3) - \epsilon_4]
= A_1 A_2 A_3 V_{in} + \epsilon_4
\]
Offset Cancellation
Cascaded Output Series Cancellation

\[ V_{out} = A_1 \cdot A_2 \cdot A_3 \left( V_{in} + \frac{f_o}{A_1 \cdot A_2 \cdot A_3} \right) \]

Input-Referred Offset = \( \frac{f_o}{A_1 \cdot A_2 \cdot A_3} \)

Example:
3-stage open-loop differential amplifier with offset cancellation + output amplifier (see ref.)

\[ A_{Total}^{(DC)} = 2 \times 10^6 = 120 \text{dB} \]

- Input-referred offset < 5µV
- Input-referred offset drift < 0.05µV

Offset Cancellation
Input Series Cancellation

Store offset

\[ S1 = 0 \text{ (off)} \]
\[ S2, S3 = 1 \text{ (conducting)} \]

\[ V_C = -A(V_C - V_{os}) \]
\[ = \frac{A}{A+1}V_{os} - V_{os} \]

Note: Amplifier has to be compensated for unity gain stability

Offset Cancellation
Input Series Cancellation

Amplify

\[ S2, S3 \rightarrow \text{open} \]
\[ S1 \rightarrow \text{closed} \]

\[ V_{out} = -A(V_{in} + V_C - V_{os}) = -A\left[V_{in} + \frac{V_{os}}{A+1} - 1\right] \]

\[ \therefore V_{out} = -A\left(V_{in} - \frac{V_{os}}{A+1}\right) \]

and

Input-Reflected Offset = \frac{V_{os}}{A+1}
Offset Cancellation
Cascaded Input Series Cancellation

$$V_{out} = A_1 A_2 V_{in} + \frac{V_{os2}}{A_1 (A_2 + 1)} \frac{e_2}{A_1}$$

Input-Referenced Offset = $$\frac{V_{os2}}{A_1 (A_2 + 1)} \frac{e_2}{A_1}$$

$$e_2 \rightarrow$$ opening of S4 charge injection

→ Amplifier A1 offset → fully cancelled
→ Amplifier A2 offset → attenuated by 1/A1.A2
→ Error associated with opening of S4 charge injection attenuated by 1/A1

CMOS Comparators
Cascade of Gain Stages

Fully differential gain stages → 1st order cancellation of switch feedthrough & charge injection offsets

1-Output series offset cancellation

2-Input series offset cancellation
CMOS Comparators
Cascade of Gain Stages

3-Combined input & output series offset cancellation

\[
\text{\(V_{\text{in1}}\)} \quad \text{\(V_{\text{in2}}\)}
\]

\(V_{\text{out1}}\) & \(V_{\text{out2}}\) are both stored on a single pair of coupling capacitors.

CMOS Latched Comparators

Comparator amplification need not be linear
\(
\rightarrow \text{can use a latch} \rightarrow \text{regeneration}
\)

\rightarrow \text{Amplification + positive feedback}
CMOS Latched Comparators

Latch can be modeled as a single-pole amp + positive feedback

Ac Model:

\[ V_{out} = V_{in} \]

Delay

Compared to a 3-stage open-loop cascade of amps for equal gain of 1000

\[ \rightarrow \text{Latch faster by about x3} \]

Only drawback \[ \rightarrow \text{high latch offset (typically 10-100mV)} \]

\[ \rightarrow \text{Use preamp w/gain =10-100 to reduce input-referred latch offset} \]

\[ \rightarrow \text{Or use offset cancellation} \]

\[ \tau_{D(3-state \text{ amp})} = 18.2 \left( \frac{C}{g_m} \right) \]

Normalized Latch Delay

<table>
<thead>
<tr>
<th>( A_L )</th>
<th>( \tau_D ) (( \frac{C}{g_m} ))</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>2.3</td>
</tr>
<tr>
<td>100</td>
<td>4.6</td>
</tr>
<tr>
<td>1000</td>
<td>5.9</td>
</tr>
<tr>
<td>10K</td>
<td>9.2</td>
</tr>
</tbody>
</table>
Latched Comparator

- Clock rate $f_s$
- Resolution
- Overload recovery
- Input capacitance (and linearity!)
- Power dissipation
- Common-mode rejection
- Kickback noise
- ...

Comparators Overdrive Recovery

Linear model for a single-pole amplifier:

During reset amplifier settles exponentially to its zero input condition with $\tau_0 = RC$

Assume $V_m \rightarrow$ maximum input normalized to $1/2\text{lsb} (=1)$

Example: Worst case input/output waveforms
- Limit output voltage swing by
  1. Passive clamp
  2. Active restore
  3. Low gain/stage
Comparators Overdrive Recovery
Limiting Output

Clamp
Adds parasitic capacitance

Active Restore
After outputs are latched → Activate φ_R & equalize output nodes

CMOS Comparator Example

- Flash ADC: 8 bits, ±1/2 LSB INL @ fs=15MHz (V_ref=3.8V)
- No offset cancellation

Comparator with Auto-Zero


Auto-Zero Implementation

Comparator Example

• Variation on Yukawa latch used w/o preamp
• No dc power when $\phi$ high
• Good for low resolution ADCs
• M11 & M12 added to vary comparator threshold
• To 1st order, for $W_1=W_2$ & $W_{11}=W_{12}$
  $V_{th,\text{latch}} = \frac{W_{11}}{W_1} \times V_R$
  where $V_R = V_{R+} - V_{R-}$


Comparator Example

• Used in a pipelined ADC with digital correction → no offset cancellation
• Note differential reference
• M7, M8 operate in triode region
• Preamp gain ≈ 10
• Input buffers suppress kick-back

Flash Converter Errors

- Comparator input:
  - Offset
  - Nonlinear input capacitance
  - Kickback noise (disturbs reference)
  - Signal dependent sampling time

- Comparator output:
  - Sparkle codes (... 111101000 ...)
  - Metastability

Typical Flash Output Decoder

Binary Output (negative)

Thermometer to Binary decoder ROM
Sparkle Codes

Correct Output:
0110 … 1000

Actual Output:
1110

Erronous 0
(comparator offset?)

Sparkle Tolerant Encoder

Protects against a single sparkle.

Meta Stability

Different gates interpret metastable output $X$ differently

Correct Output: 0111 or 1000

Actual Output: 1111

Solutions:
- Latches (high power)
- Gray encoding


Gray Encoding

- Each $T_i$ affects only one $G_i$
  - Avoids disagreement of interpretation by multiple gates
- Protects also against sparkles
- Follow Gray encoder by (latch and) binary encoder

<table>
<thead>
<tr>
<th>Thermometer Code</th>
<th>Gray</th>
<th>Binary</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_1$ $T_2$ $T_3$ $T_4$ $T_5$ $T_6$ $T_7$</td>
<td>$G_1$</td>
<td>$G_2$</td>
</tr>
<tr>
<td>0 0 0 0 0 0 0</td>
<td>0 0 0 0 0 0 0</td>
<td>0 0 0 0</td>
</tr>
<tr>
<td>1 0 0 0 0 0 0</td>
<td>0 0 0 1 0 0 0</td>
<td>0 1 1</td>
</tr>
<tr>
<td>1 1 0 0 0 0 0</td>
<td>0 1 1 0 1 0 0</td>
<td>1 1 1</td>
</tr>
<tr>
<td>1 1 1 0 0 0 0</td>
<td>0 1 1 0 1 0 0</td>
<td>1 1 1</td>
</tr>
<tr>
<td>1 1 1 1 0 0 0</td>
<td>1 1 0 1 0 0 0</td>
<td>1 1 1</td>
</tr>
<tr>
<td>1 1 1 1 1 0 0</td>
<td>1 1 1 1 1 0 0</td>
<td>1 1 1</td>
</tr>
<tr>
<td>1 1 1 1 1 1 1</td>
<td>1 1 1 1 1 1 1</td>
<td>1 1 1</td>
</tr>
</tbody>
</table>

$G_1 = T_1 T_3 + T_5 T_7$

$G_2 = T_2 T_6$

$G_3 = T_4$