

**Problem 1**

To simplify the derivation, let's normalize everything with respect to  $I_{ref} = V_{ref}/R_{total}$  – i.e. calculate INL and DNL based on deviation of the resistor string, instead of in term of voltage deviation.

Correct for gain/FS error

$$\begin{aligned} MSB &= \sum_{i=0}^{2^N-1} R + i \cdot \Delta R \\ &= (2^N - 1) \cdot R + \frac{2^N (2^N - 1)}{2} \cdot \Delta R \\ &= (2^N - 1) [R + 2^{N-1} \cdot \Delta R] \end{aligned}$$

$$LSB = \frac{MSB}{(2^N - 1)} = R + 2^{N-1} \cdot \Delta R$$

$$\begin{aligned} DNL[i] &= \frac{[R + (2^N - i) \cdot \Delta R] - [R + 2^{N-1} \cdot \Delta R]}{R + 2^{N-1} \cdot \Delta R} && (LSB) \\ &= \frac{(2^{N-1} - i) \cdot \Delta R}{R + 2^{N-1} \cdot \Delta R} \\ &= \frac{(2^{N-1} - i) \cdot \frac{\Delta R}{R}}{1 + 2^{N-1} \cdot \frac{\Delta R}{R}} && \text{for } i = 1 \rightarrow (2^N - 1) \end{aligned}$$

$$\begin{aligned} INL[k] &= \frac{\sum_{i=1}^k (2^{N-1} - i) \cdot \Delta R}{R + 2^{N-1} \cdot \Delta R} && (LSB) \\ &= \frac{[k \cdot 2^{N-1} - \frac{(k+1) \cdot k}{2}] \Delta R}{R + 2^{N-1} \cdot \Delta R} \\ &= \frac{[k \cdot 2^{N-1} - \frac{(k+1) \cdot k}{2}] \frac{\Delta R}{R}}{1 + 2^{N-1} \cdot \frac{\Delta R}{R}} \end{aligned}$$

$$(DNL[0] = 0; INL[0] = 0)$$

Assume N large. Max DNL (absolute value) happens at the endpoints ( $i=1$  and  $i=2^N-1$ ), max INL happens at the midpoint ( $i=2^{N-1}$ ).

$$| \text{DNL}_{\max} | = \frac{(2^{N-1} - 1) \cdot \frac{\Delta R}{R}}{1 + 2^{N-1} \cdot \frac{\Delta R}{R}}$$

$$\text{INL}_{\max} = \frac{(2^{2N-3} - 2^{N-2}) \frac{\Delta R}{R}}{1 + 2^{N-1} \cdot \frac{\Delta R}{R}}$$

For 8-bit DAC with  $\Delta R/R = 0.05\%$  :

$$\text{DNL}_{\max} = 0.0597 \text{ LSB}$$

$$\text{INL}_{\max} = 3.82 \text{ LSB}$$

## Problem 2

Key points :

- Given a fixed-area unit-current cell
  - We can associate a  $\sigma$  (assuming Gaussian distribution), which is a function of the area, to quantify the mismatches between unit current cells
  - We can then quantify INL and DNL for different DAC topology/segmentation as a function of  $\sigma$
  - DNL of a thermometer DAC is low – actually it's equal to  $\sigma$
  - DNL of a binary DAC is much higher
  - INL for both thermometer and binary DAC is about the same. INL spec would ultimately impose a minimum unit current cell area requirement regardless of topology/segmentation
- Knowing the above, to achieve a certain DNL, we can observe the following
  - Area of unit current cell for a binary DAC needs to be much larger than a thermometer based DAC
  - If we segment the DAC, as function of segmentation, the total current cell area is a decreasing function – where no segmentation here represent a fully binary DAC and a 100% segmentation represent a fully thermometer DAC
  - However thermometer DAC requires a digital decoder, whose area is non-negligible – this offsets the area benefit of a thermometer DAC – and therefore creating a *convex* function of segmentation vs. total DAC area
- Given the above convex function, we can optimize ! (Figure 9)
- DAC Layout techniques : use of dummies, common-centroid layout, global & local biasing, decoder randomization
  
- As technology scales we expect that the digital area (decoder) to faithfully scales down. Although technology scaling does give rise to finer lithography capability, random dopant fluctuations would still exist, and therefore it's rather unreasonable to think that  $\sigma$  would scale down with technology. Therefore we would expect that the required unit-current cell area to remain relatively constant if we were to maintain the same DNL/INL requirement. Based on Fig 9. we can expect the  $A_{\text{digital}}$  line to shifts down, as the digital area decreases, and hence the optimal point would move more to the right – i.e. favoring a more highly segmented DAC. In the limiting case where the digital area is negligible, we would of course implement a fully thermometer DAC for the reasons mentioned in the first point above.