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College of Engineering
Department of Electrical Engineering
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Homework 6
Due Tuesday Nov. 22, 2005

EECS 247
FALL 2005

Problem 1:

An 8-bit flash ADC is build with close to an ideal resistor string with VFS=1V.

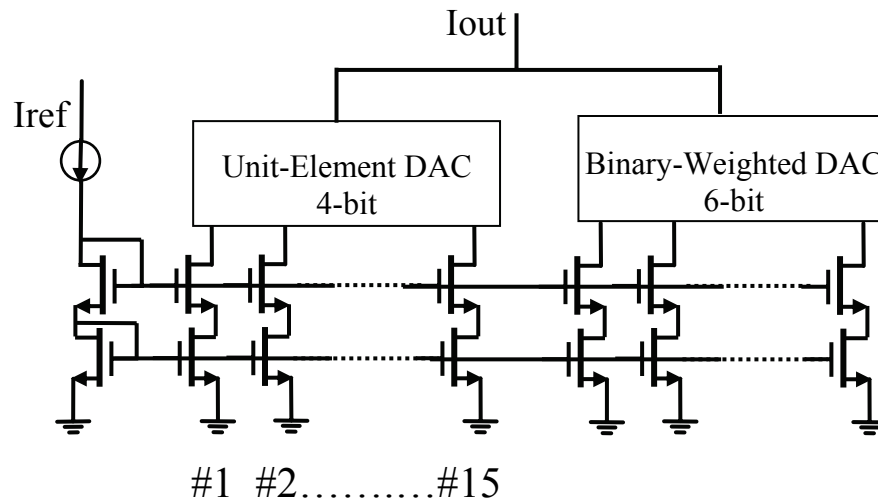
The designer of the comparator has measured the input-referred offset voltage to be within $\pm 3\text{mV}$ for 99.7% of the measured samples.

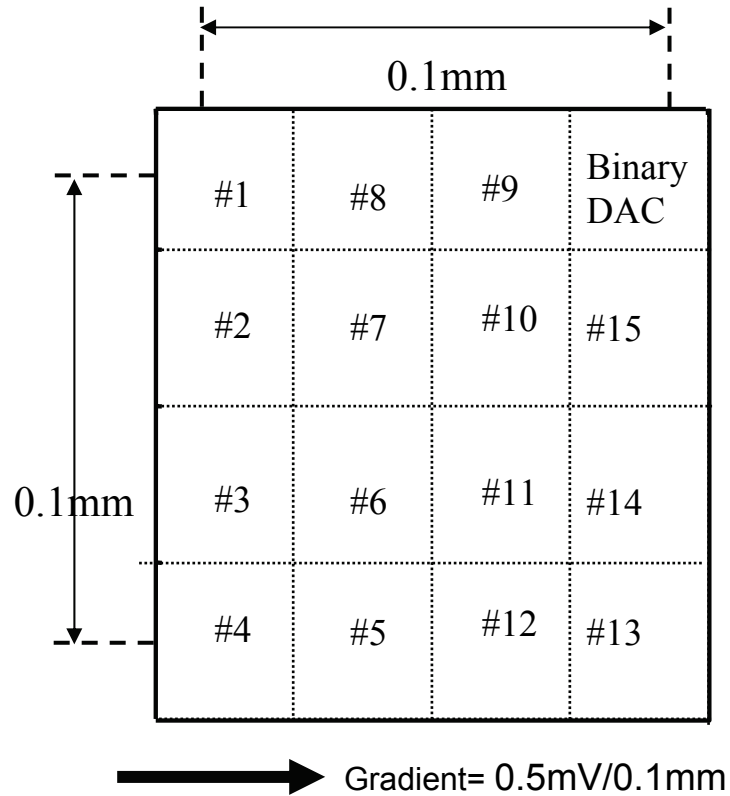
Compute the standard deviation of the ADC DNL and INL.

Problem 2:

The 10-bit segmented DAC shown below, comprises 15 equal unit-element current sources and a 6-bit binary weighted DAC. The current sources are laid out in a rectangular array as shown. Assume that the 6-bit DAC is laid out to occupy the 16th site of the array. All the devices operate at the same $(V_{gs}-V_{th})$. Assume the threshold voltages are affected by a systematic process related gradient which causes an offset much larger than the expected random offset. The process gradient is in the direction shown on the array and has a value of $0.5\text{mV}/0.1\text{mm}$.

- a) Compute the minimum value required for $(V_{gs}-V_{th})$ to achieve $1/2\text{LSB}$ integral linearity for this 10-bit DAC.
- b) What is the differential nonlinearity?





Problem 3.

Study the publication:

D. W. Cline, P.R Gray "A power optimized 13-b 5MSamples/s pipelined analog-to-digital converter in 1.2um CMOS," JSSC 3/1996

Summarize the important points in less than one page.