

Problem 1:

1)

$$V_{os} := 0V$$

$$V_{FS_ideal} := \frac{V_{ref} \cdot (2^N - 1)}{2^N}$$

$$V_{FS_real} := \frac{V_{ref} \cdot [(2^N - 1) \cdot R + \Delta R \cdot (2^N - 1) \cdot 2^{N-1}]}{2^N \cdot R + \Delta R \cdot (2^N - 1) \cdot 2^{N-1}} - V_{os}$$

$$DAC_Gain := \frac{V_{FS_real}}{V_{FS_ideal}}$$

$$DAC_Gain := \frac{R + \Delta R \cdot 2^{N-1}}{R + \frac{\Delta R \cdot (2^N - 1)}{2}}$$

$$Ideal_step := \frac{V_{ref}}{2^N}$$

$$Real_step := \frac{V_{ref} \cdot (R + M \cdot \Delta R)}{2^N \cdot R + \Delta R \cdot (2^N - 1) \cdot 2^{N-1}} \quad \text{where } M \text{ depends on the position in the } R \text{ string}$$

$$Normalized_step := \frac{Real_step}{DAC_Gain}$$

$$Normalized_step := \frac{V_{ref} \cdot (R + M \cdot \Delta R)}{2^N \cdot (R + \Delta R \cdot 2^{N-1})}$$

$$\text{DNL} := \frac{\text{Normalized_step} - \text{Ideal_step}}{\text{Ideal_step}}$$

$$\text{DNL}(M) := \frac{\Delta R \cdot (M - 2^{N-1})}{(R + \Delta R \cdot 2^{N-1})} \quad \text{and } M \text{ goes from } 1 \text{ to } 2^N - 1.$$

$$\text{INL}(I) := \sum_{I=1}^M \text{DNL}(I)$$

$$\text{INL}(I) := \frac{\Delta R \cdot I}{(R + \Delta R \cdot 2^{N-1})} \cdot \left[\frac{(I+1)}{2} - 2^{N-1} \right] \quad \text{and } I \text{ goes from } 1 \text{ to } 2^N - 1.$$

2)

Maximum DNL and INL:

$$\text{DNL}_{\max} = \text{DNL}(2^N - 1) = -\text{DNL}(1) = \frac{\Delta R \cdot (2^{N-1} - 1)}{(R + \Delta R \cdot 2^{N-1})}$$

$$\text{INL}_{\max} = \text{INL}(2^{N-1}) = \frac{2^{N-2} \Delta R}{(R + \Delta R \cdot 2^{N-1})} \cdot (1 - 2^{N-1})$$

3)

LSB := 1

N := 8

R := 1

$\Delta R := 0.0005$

$$\text{DNL}_{\max} := \frac{\frac{\Delta R}{R} \cdot (2^{N-1} - 1)}{\left(1 + \frac{\Delta R}{R} \cdot 2^{N-1}\right)} \quad \text{DNL}_{\max} = 0.06 \text{ LSB}$$

$$\text{INL}_{\max} := \frac{2^{N-2} \frac{\Delta R}{R}}{\left(1 + \frac{\Delta R}{R} \cdot 2^{N-1}\right)} \cdot (1 - 2^{N-1}) \quad \text{INL}_{\max} = -3.82 \text{ LSB}$$

Problem 2:

This paper presents the design of a 10-b 500-MSample/s CMOS DAC, in particular the design of a DAC capable of achieve a high SFDR (i.e >60dB SFDR for signals from DC to Nyquist at 200MSamples/s).

To achieve this performance, the authors endeavour to find the best compromise, or segmentation, between binary weighted and thermometer coded elements.

The authors state that binary weighted DACs are smaller in size than corresponding thermometer coded DAC for the same INL, since binary weighted DAC do not need any digital decoding logic. However, binary weighted DACs suffer from worst DNL at the midcode transitions, are not guaranteed to be monotonic for large N, and introduce distortion due to glitching. Thermometer coded DAC do not suffer from these problems, in particular the later problem since the glitching is proportional to the signal.

The authors then compare the area of the analog blocks for the two types of implementation. The INL performance hinges on the area of the entire analog core, so the two implementations have the same INL performance per unit area. The DNL however, greatly favors the thermometer code since the matching requirements become very stringent for the binary weighted DAC at midcode transitions.

To leverage the strengths of both the thermometer coded and the binary weighted DACs, the MSB are implemented in thermometer code and the LSB in binary weight. The amount of segmentation is determined by the total required area to meet the specifications. At low level of segmentation (mostly binary weighted implementation), the area required to meet the DNL specs dominates. As the the amount of segmenation increases, the minimum core area needed to meet the INL requirements dominates. At high levels of segmentation, the digital logic for the thermometer coded bits begins to dominate.

As technology scales, the overhead due to the digital decoding logic will decrease. The area constraint of the core due to the INL requirements will stay the same, as will the area constraint of the core due to the DNL requirement in the case of the binary weighted bits. What this means for figure 9 is that the slope of the digital area will decrease pushing the optimum closer to the fully thermometer coded DAC.

One comment I have about figure 9 is that what they contend is the optimum point in fact represents a "3dB point", where the area is twice as large as they state (so 2^7 instead of 2^6). If reducing area is the goal, then in my opinion, the optimum point is the midpoint between the two intersection points (segmentation of around 55%).

Furthermore, to buttress the segmentation, the authors used good layout practices to eliminate the effects of process gradients in their quest to hit the desired specs.

