EE 247 Homework #6

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Part 1:

$N := 8$ $V_{FS} := 1V$ $Yield := 99.73\%$ $V_{os} := 3mV$ $V_{ref} := V_{FS}$

$\Delta := \frac{V_{FS}}{2^N}$ $\Delta = 3.906\,mV$

$\sigma_{vos} := 1V$ $CTOL := 10^{-15}$ $TOL := 10^{-15}$

Given

$$Yield = erf\left(\frac{3mV}{\sqrt{2}\cdot\sigma_{vos}}\right)$$

$\sigma_{vos} := Find(\sigma_{vos})$ $\sigma_{vos} = 1\,mV$

$$DNL_i = \frac{\left(V_i - V_{os_i}\right) - \left(V_{i-1} - V_{os_{i-1}}\right) - \Delta}{\Delta} = \frac{V'_i - V'_{i-1}}{\Delta} - 1$$

$$\sigma_{DNL}^2 = \frac{\sigma_{vos}^2 + \sigma_{vos}^2}{\Delta^2} = \frac{2\cdot\sigma_{vos}^2}{\Delta^2}$$

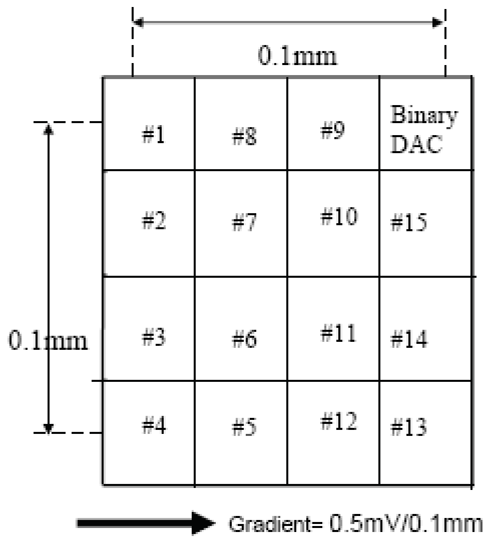
$$\sigma_{DNL} := \sqrt{\frac{2\cdot\sigma_{vos}^2}{\Delta^2}}$$ $\sigma_{DNL} = 0.362\,LSB$

$$INL_i = \sum_{n=0}^{i} DNL_n = \sum_{n=1}^{i}\left(\frac{V'_n - V'_{n-1}}{\Delta} - 1\right) = \frac{V'_i - V'_0}{\Delta} - i$$

$$\sigma_{INL} := \sqrt{\frac{\sigma_{vos}^2}{\Delta^2}}$$ $\sigma_{INL} = 0.256\,LSB$

Part 2:

$N_{MSB} := 4 \qquad N_{LSB} := 6 \qquad \delta V_{th} := \frac{0.5mV}{0.1mm}$



Looking at the layout, we can conclude that the unit current sources #1-4 have the same threshold voltages, #5-8, #9-12 and #13-15.

The binary DAC would also have the same threshold voltage as #13-15.

$L := 0.1mm \qquad W := 0.1mm$

$2^{N_{LSB}} = 64 \qquad 2^{N_{LSB}+N_{MSB}} = 1024$

Define the reference current as:

$I_{ref} = \frac{k}{2} \cdot V_{dsat}^2 \qquad k \cdot \frac{V_{dsat}}{I_{ref}} = \frac{2}{V_{dsat}}$

$$I_{refB} = \frac{k}{2} \cdot \left(V_{dsat} - \delta V_{th} \cdot L\right)^2 = \frac{k}{2} \cdot V_{dsat}^2 - \frac{k}{2} \cdot 2 \cdot V_{dsat} \cdot \delta V_{th} \cdot L = I_{ref} - \frac{k}{2} \cdot 2 \cdot V_{dsat} \cdot \delta V_{th} \cdot L$$

Define the "unit" current in the second column:

$$I_{ref2} = \frac{k}{2} \cdot \left(V_{dsat} - \delta V_{th} \cdot \frac{1}{3} \cdot L\right)^2 = \frac{k}{2} \cdot V_{dsat}^2 - \frac{k}{2} \cdot 2 \cdot V_{dsat} \cdot \delta V_{th} \cdot \frac{1}{3} \cdot L$$

$$\frac{I_{ref2}}{I_{ref}} = 1 - k \cdot \frac{V_{dsat}}{I_{ref}} \cdot \delta V_{th} \cdot \frac{1}{3} \cdot L = 1 - \frac{2}{V_{dsat}} \cdot \delta V_{th} \cdot \frac{1}{3} \cdot L$$

For the 3rd and 4th columns:

$$\frac{I_{ref3}}{I_{ref}} = 1 - \frac{2}{V_{dsat}} \cdot \delta V_{th} \cdot \frac{2}{3} \cdot L \qquad \frac{I_{ref4}}{I_{ref}} = 1 - \frac{2}{V_{dsat}} \cdot \delta V_{th} \cdot L$$

Generating the DAC transfer function, and deriving the DNL and INL, we see that the maximum INL occurs at code 512. From inspection, we see that:

$V_{dsat} := 341.33\text{mV}$

The transfer functions, DLN and INL plots are shown below:

$$b := 0..2^{N_{MSB}+N_{LSB}} - 1$$

Define the values of the current sources:

$$I_{LSB}(i, V_{dsat}) := i \cdot \left(1 - \frac{2}{V_{dsat}} \cdot \delta V_{th} \cdot L\right)$$

$$I_{MSB}(i, V_{dsat}) := \begin{cases} 0 & \text{if } i = 0 \\ 2^{N_{LSB}} & \text{if } 0 < i \le 4 \\ 2^{N_{LSB}} \cdot \left(1 - \frac{2}{V_{dsat}} \cdot \delta V_{th} \cdot \frac{1}{3} \cdot L\right) & \text{if } 4 < i \le 8 \\ 2^{N_{LSB}} \cdot \left(1 - \frac{2}{V_{dsat}} \cdot \delta V_{th} \cdot \frac{2}{3} \cdot L\right) & \text{if } 8 < i \le 12 \\ 2^{N_{LSB}} \cdot \left(1 - \frac{2}{V_{dsat}} \cdot \delta V_{th} \cdot L\right) & \text{if } i > 12 \end{cases}$$

Thus, the current as a function of the current sources (normalized to the reference current):

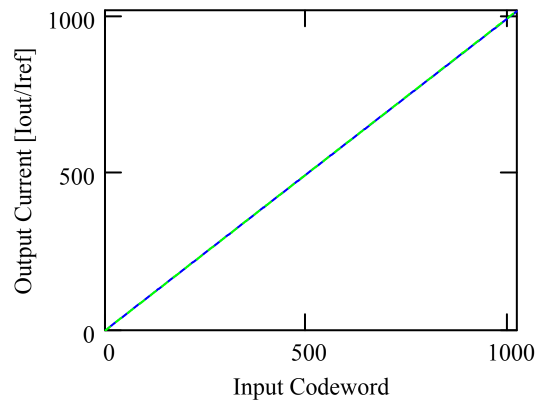
$$I_{out} := \left| \begin{array}{l} \text{for } m \in 0..2^{N_{MSB}} - 1 \\ \quad \text{for } n \in 0..2^{N_{LSB}} - 1 \\ \quad\quad z_{m,n} \leftarrow \left(\sum_{k=0}^{m} I_{MSB}(k, V_{dsat})\right) + I_{LSB}(n, V_{dsat}) \\ c \leftarrow \left(z^T\right)^{\langle 0 \rangle} \\ \text{for } s \in 0..2^{N_{MSB}} - 2 \\ \quad c \leftarrow \text{stack}\left[c, \left(z^T\right)^{\langle s+1 \rangle}\right] \\ c \end{array} \right.$$

The gain error is:

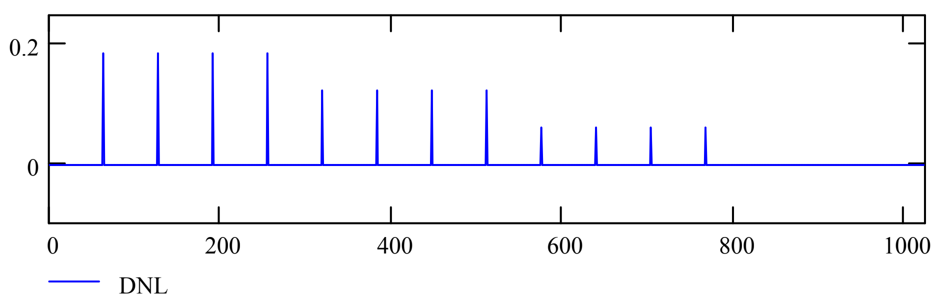
$$\varepsilon_{gain} := \frac{Iout_{2^{N_{LSB}+N_{MSB}}-1}}{2^{N_{LSB}+N_{MSB}}-1}$$

$\varepsilon_{gain} = 0.999$

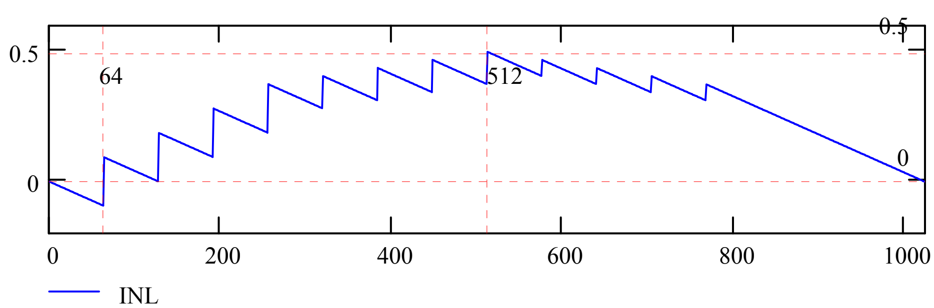
$$DNL := \begin{array}{|l} \text{for } h \in 0..2^{N_{MSB}+N_{LSB}}-2 \\ \quad x_h \leftarrow \dfrac{Iout_{h+1} - Iout_h}{\varepsilon_{gain}} - 1 \\ x \end{array}$$



$$INL := \begin{array}{|l} x_0 \leftarrow 0 \\ \text{for } h \in 0..2^{N_{MSB}+N_{LSB}}-2 \\ \quad x_{h+1} \leftarrow \sum_{d=0}^{h} DNL_d \\ x \end{array}$$



$DNL_{63} = 0.186\ LSB$ $DNL_{319} = 0.124\ LSB$ $DNL_{575} = 0.061\ LSB$ $DNL_0 = -0.0015\ LSB$



$max(INL) = 0.5\ LSB$ $min(INL) = -0.093\ LSB$ $max(DNL) = 0.186\ LSB$ $min(DNL) = -0.0015\ LSB$

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"A Power Optimized 13-b 5MSample/s Pipelined ADC in 1.2μm CMOS" by D. W. Cline and P. R. Gray, JSSC March 1996

Summary of Important Points:

In high resolution pipelined ADCs, the thermal noise (kT/C) related power consumption is dependent on the gain of each stage (G) and the rate of scaling of the capacitor sizes for each stage.

For the sample and hold / DAC / subtraction / gain block shown in Figure 2, the input referred thermal noise distribution over the pipeline stages determines the power distribution over the stages.

Figure 3 shows the two extreme cases of capacitive scaling. One extreme is when all the stages are sized the same, resulting in equal power dissipation per stage, while the input referred noise contribution per stage decreases. The other extreme is when the noise contribution of each stage is made the same. This reduced the power contributions of the succeeding stages due to the decrease in the capacitances needed for the subsequent stages.

Increasing the interstage gain implies higher resolution per stage. This results in reduced feedback capacitance loading, however, the input capacitance of the succeeding stage increases. This usually limits the resolution per stage to around 1.5 bits. However, scaling the capacitor faster allows the use of higher resolution per stage in a high-resolution pipelined ADC.

The power of each pipeline stage is then expressed as the power needed to charge the effective load of the amplifier (including the effect of the feedback capacitor and input capacitance of the next pipeline stage), in a specified time (based on the linear settling time of the amplifier), which is also dependent on the capacitances.

The optimal capacitance taper factor and interstage gain that minimizes the overall pipeline ADC power is then found. The results of these optimizations are presented in Figures 16 and 17. This optimization shows that increasing the resolution per stage implies more aggressive capacitance scaling to counter the increasing input capacitance of each stage, resulting in lower overall power consumption.

This capacitance scaling is limited by the smallest capacitor that can be realized reliably. When this limit is reached, reduced interstage gain can be used for the subsequent stages since capacitance scaling cannot be used to reduce the load presented by the next stage. However, from a practical point of view, the same interstage gain is usually used for all pipeline stages.

This power optimization is applied to a 13-bit ADC in 1.2μm CMOS, and its characteristics are shown in Table 1.