EE247
Lecture 10

• Switched-Capacitor Filters
  – Switched-capacitor integrators
    • DDI integrators
    • LDI integrators
    • Effect of parasitic capacitance
    • Bottom-plate integrator topology
  – Resonators
  – Bandpass filters
  – Lowpass filters
    • Termination implementation
    • Transmission zero implementation
  – Switched-capacitor filter design considerations
  – Switched-capacitor filters utilizing double sampling technique
  – Effect of non-idealities

Switched-Capacitor Integrator
DDI Switched-Capacitor Integrator

\[\Phi_1 \rightarrow Q_1[(n-1)T_s] = C_s V_i[(n-1)T_s], \quad Q_1[(n-3/2)T_s] = Q_1[(n-3/2)T_s]\]

\[\Phi_2 \rightarrow Q_2[(n-1/2)T_s] = 0, \quad Q_1[(n-1/2)T_s] = Q_1[(n-3/2)T_s] + Q_2[(n-1)T_s]\]

\[\Phi_1 \rightarrow Q_1[nT_s] = C_s V_i[nT_s], \quad Q_1[(n-1)T_s] = Q_1[(n-1)T_s] + Q_s[(n-1)T_s]\]

Since \(V_{o1} = -Q_1/C_i \quad \text{&} \quad V_i = Q_1/C_s \Rightarrow C_i V_{o1}[(n-1)T_s] = C_i V_{o1}[(n-1)T_s] - C_s V_i[(n-1)T_s] \]
DDI Switched-Capacitor Integrator
Output Sampled on $\phi_1$

\[-C_I V_o(nT) = -C_I V_o[(n-1)fs] + C_s V_{in}[n-1fs]\]

\[V_o(nT) = V_o[(n-1)fs] - \frac{C_s}{C_f} V_{in}[n-1fs]\]

\[V_o(Z) = Z^{-1} V_o(Z) - Z^{-1} \frac{C_s}{C_f} V_{in}(Z)\]

\[\frac{V_o}{V_{in}}(Z) = -\frac{C_s}{C_f} \frac{Z-1}{1-Z^{-1}}\]

DDI (Direct-Transform Discrete Integrator)

z-Domain Frequency Response

- LHP singularities in s-plane map into inside of unit-circle in Z domain
- RHP singularities in s-plane map into outside of unit-circle in Z domain
- The j$\omega$ axis maps onto the unit circle
- Particular values:
  - $f=0 \rightarrow z=1$
  - $f=f_s/2 \rightarrow z=-1$
- The frequency response is obtained by evaluating $H(z)$ on the unit circle at
  $z = e^{j\omega T} = \cos(\omega T) + j\sin(\omega T)$
- Once $z=-1$ ($f_s/2$) is reached, the frequency response repeats, as expected
- The angle to the pole is equal to
  360° (or 2$\pi$ radians) times the ratio of the pole frequency to the sampling frequency

$\frac{(\cos(\omega T), \sin(\omega T))}{f_s}$

$\frac{2\pi f}{f_s}$

$\frac{f}{f_s}$
Switched-Capacitor Direct-Transform Discrete Integrator

\[ \frac{V_o(z)}{V_{in}} = -\frac{C_s}{C_I} \times \frac{z^{-1}}{1-z^{-1}} \]

\[ = -\frac{C_s}{C_I} \times \frac{1}{z-1} \]

DDI Integrator
Pole-Zero Map in z-Plane

Z-1=0 → Z=1 on unit circle

Pole from f→0 in s-plane mapped to z=+1

As frequency increases z domain pole moves on unit circle (CCW)

Once pole gets to (Z=-1), (f=f_s/2), frequency response repeats
DDI Switched-Capacitor Integrator

\[
\frac{V_o}{V_{in}}(Z) = -\frac{C_o}{C_I} \times \frac{Z^{-1}}{1-Z^{-1}}, \quad Z = e^{j\omega f}
\]

\[
= \frac{C_o}{C_I} \times \frac{1}{1-e^{j\omega f/2}} = \frac{C_o}{C_I} \times e^{-j\omega f/2} - e^{j\omega f/2}
\]

\[
= -\frac{C_o}{C_I} \times e^{-j\omega f/2/T} \times \frac{1}{\sin(\omega f/2)}
\]

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<tr>
<th>Ideal Integrator</th>
<th>Magnitude Error</th>
<th>Phase Error</th>
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Example: Mag. & phase error for:
1- \( f/fs = 1/12 \) \( \rightarrow \) Mag. Error = 1% or 0.1dB
Phase error = 15 degree
\( Q_{mag} = -3.8 \)

2- \( f/fs = 1/32 \) \( \rightarrow \) Mag. Error = 0.16% or 0.014dB
Phase error = 5.6 degree
\( Q_{mag} = -10.2 \)

DDI Integrator
\( \rightarrow \) magnitude error no problem
phase error major problem
Switched Capacitor Filter
Build with DDI Integrator

Example: 5th Order Elliptic Filter
Singularities pushed towards RHP due to integrator excess phase

s-plane

Coarse View

Fine View

Pole
Zero

$|H(j\omega)|$

SC DDI based Filter
Zeros lost!

Continuous-Time Prototype

$f_s/2$ $f_s$ $2f_s$ $f$

Passband Peaking

Continuous-Time Prototype
Switched-Capacitor Integrator
Output Sampled on $\Phi_2$

Sample output $\frac{1}{2}$ clock cycle earlier
$\rightarrow$ Sample output on $\Phi_2$

\[ Q_s[(n-1)T_s] = C_s V_i[(n-1)T_s], \quad Q_I[(n-3/2)T_s] = Q_s[(n-3/2)T_s] \]

\[ \Phi_1 \rightarrow Q_s[(n-1)T_s] = C_s V_i[(n-1)T_s], \quad Q_I[(n-1)T_s] = Q_s[(n-1)T_s] \]

\[ \Phi_2 \rightarrow Q_s[(n-1/2)T_s] = 0, \quad Q_I[(n-1/2)T_s] = Q_s[(n-1/2)T_s] + Q_s[(n-1)T_s] \]

\[ \Phi_1 \rightarrow Q_s[nT_s] = C_s V_i[nT_s], \quad Q_I[nT_s] = Q_s[nT_s] + Q_s[(n-1)T_s] \]

\[ \Phi_2 \rightarrow Q_s[(n+1/2)T_s] = 0, \quad Q_I[(n+1/2)T_s] = Q_s[(n+1/2)T_s] + Q_s[nT_s] \]
Switched-Capacitor Integrator
Output Sampled on $\phi_2$

$Q_i[(n+1/2)Ts] = Q_i[(n-1/2)Ts] + Q_i[nTs]$ $V_{i2} = -Q_i/C_i & V_i = Q_s/C_s \Rightarrow C_i V_{i2}[(n+1/2)Ts] = C_i V_{i2}[(n-1/2)Ts] - C_s V_i[nTs]$ Using the $z$-operator rules:

$\Rightarrow C_i V_{i2} Z^{1/2} = C_i V_{i2} Z^{-1/2} - C_s V_i$

$V_{i2}(Z) = -\frac{C_s}{C_i} \times \frac{Z^{-1/2}}{1-Z^{-1}}$

LDI Switched-Capacitor Integrator

LDI (Lossless Discrete Integrator) $\Rightarrow$
same as DDI but output is sampled $1/2$ clock cycle earlier

$V_{i2}(Z) = -\frac{C_s}{C_i} \times \frac{Z^{-1/2}}{1-Z^{-1}}$, $Z = e^{j\pi f_2 T}$ $V_{i2}(Z) = -\frac{C_s}{C_i} \times \frac{Z^{-1/2}}{1-e^{j\pi f_2 T}}$

$= -j \frac{C_s}{C_i} \frac{1}{2\sin(\pi f_2 T/2)}$

No Phase Error!
For signals at frequencies $<<$ sampling freq.
$\Rightarrow$ Magnitude error negligible

Ideal Integrator

Magnitude Error
Frequency Warping

- Frequency response
  - Continuous time (s-plane): imaginary axis
  - Sampled time (z-plane): unit circle
- Continuous to sampled time transformation
  - Should map imaginary axis onto unit circle
  - How do SC integrators map frequencies?

\[ H_{sc}(z) = \frac{C_s}{C_m} \frac{z^{-j\omega}}{1 - z^{-1}} \]
\[ = -\frac{C_s}{C_m} \frac{1}{2j \sin \pi f_{sc} T} \]

CT – SC Integrator Comparison

CT Integrator
\[ H_{sc}(s) = \frac{1}{s^\tau} \]
\[ = \frac{1}{2\pi f_{sc} \tau} \]

SC Integrator
\[ H_{sc}(z) = \frac{C_s}{C_m} \frac{z^{-j\omega}}{1 - z^{-1}} \]
\[ = -\frac{C_s}{C_m} \frac{1}{2j \sin \pi f_{sc} T} \]

Identical time constants:
\[ \tau = RC = \frac{C_m}{f_s C_s} \]

Compare: \( H_{RC}(f_{RC}) = H_{SC}(f_{SC}) \)
\[ f_{SC} = \frac{f_s}{\pi} \sin \left( \pi \frac{f_{SC}}{f_s} \right) \]
LDI Integration

\[ f_{\text{SC}} = \frac{f_s}{\pi} \sin \left( \pi \frac{f_{\text{RC}}}{f_s} \right) \]

- "RC" frequencies up to \( f_s/\pi \) map to physical (real) "SC" frequencies
- Frequencies above \( f_s/\pi \) do not map to physical frequencies
- Mapping is symmetric about \( f_s/2 \) (aliasing)
- "Accurate" only for \( f_{\text{RC}} \ll f_s \)

Switched-Capacitor Filter
Built with LDI Integrators

Zeros Preserved
Switched-Capacitor Integrator
Parasitic Sensitivity

Effect of parasitic capacitors:
1. $C_{p1}$ - driven by opamp o.k.
2. $C_{p2}$ - at opamp virtual gnd o.k.
3. $C_{p3}$ - Charges to $V_{in}$ & discharges into $C_i$

$\rightarrow$ Problem parasitic sensitivity

Parasitic Insensitive
Bottom-Plate Switched-Capacitor Integrator

Sensitive parasitic cap. $\rightarrow C_{p1}$ $\rightarrow$ rearrange circuit so that $C_{p1}$ does not charge/discharge

$\phi_1=1 \rightarrow C_{p1}$ grounded

$\phi_2=1 \rightarrow C_{p1}$ at virtual ground

$\text{Solution: Bottom plate capacitor integrator}$
Bottom Plate Switched-Capacitor Integrator

Input/Output z-transform
Note: Delay from $V_{i+}$ and $V_{i-}$ to output is different
→ Special attention needed to input/output connections

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<th>$V_{o2}$ on $\phi_2$</th>
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<tr>
<td>$V_{i+}$ on $\phi_1$</td>
<td>$\frac{z^{-1}}{1-z^{-1}}$</td>
<td>$\frac{z^{-1/2}}{1-z^{-1}}$</td>
</tr>
<tr>
<td>$V_{i-}$ on $\phi_2$</td>
<td>$\frac{-z^{-1/2}}{1-z^{-1}}$</td>
<td>$\frac{-1}{1-z^{-1}}$</td>
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LDI Switched-Capacitor Ladder Filter

Delay around integ. Loop is \((Z^{-1/2}, Z^{+1/2} = l) \Rightarrow \text{LDI function}\)

Switched-Capacitor LDI Resonator

**Resonator Signal Flowgraph**

\[
\frac{\omega_1}{s} = \frac{1}{s}
\]

\[
\frac{\omega_2}{s} = \frac{1}{R_{eq} C_2}
\]

\[
\omega_1 = \frac{1}{R_{eq} C_2} = f_s \times \frac{C_1}{C_2}
\]

\[
\omega_2 = \frac{1}{R_{eq} C_4} = f_s \times \frac{C_3}{C_4}
\]
Fully Differential Switched-Capacitor Resonator

Switched-Capacitor LDI Bandpass Filter Utilizing Continuous-Time Termination

\[ \omega_0 = \frac{C_2}{C_4} f_s \times \frac{C_2}{C_2} \]

\[ Q = \frac{C_2}{C_2} \]
s-Plane versus z-Plane

Example: 2nd Order LDI Bandpass Filter

Switched-Capacitor LDI Bandpass Filter
Continuous-Time Termination

\[ f_0 = \frac{1}{2\pi f_s} \cdot \frac{C_1}{C_2} \]
\[ \Delta f = \frac{f_0}{Q} \]
\[ = \frac{1}{2\pi f_s} \cdot \frac{C_1 Q}{C_2 C_4} \]

Both accurately determined by cap ratios & clock frequency
Fifth Order All-Pole LDI Low-Pass Ladder Filter

Complex Conjugate Terminations

- Complex conjugate terminations (alternate phase switching)

Sixth-Order Elliptic LDI Bandpass Filter

Use of T-Network

High Q filter $\rightarrow$ large cap. ratio for Q & transmission zero implementation
To reduce large ratios required $\rightarrow$ T-networks utilized

Sixth Order Elliptic Bandpass Filter
Utilizing T-Network

- T-networks utilized for:
  - Q implementation
  - Transmission zero implementation


Switched-Capacitor Resonator

Regular sampling
Each opamp busy settling only during one of the clock phases
→ Idle during the other clock phase
Switched-Capacitor Resonator Using Double-Sampling

Double-sampling:

- 2nd set of switches & sampling caps added to all integrators
- While one set of switches/caps sampling the other set transfers charge into the intg. cap
- Opamps busy during both clock phases
- Effective sampling freq. twice clock freq. while opamp bandwidth requirement remains the same

Double-Sampling Issues

Issues to be aware of:
- Jitter in the clock
- Unequal clock phases
- Mismatch in sampling caps.

Double-Sampled Fully Differential S.C. 6th Order All-Pole Bandpass Filter


Sixth Order Bandpass Filter Signal Flowgraph
Double-Sampled Fully Differential 6th Order S.C. All-Pole Bandpass Filter

- Cont. time termination (Q) implementation
- Folded-Cascode opamp with $f_m = 100$MHz used
- Center freq. 3.1MHz, filter $Q=55$
- Clock freq. 12.83MHz $\to$ effective oversampling ratio 8.27
- Measured dynamic range 46dB ($IM3=1\%$)


Effect of Opamp Nonidealities on Switched Capacitor Filter Behaviour

- Opamp finite gain
- Opamp finite bandwidth
- Finite slew rate of the opamp
Effect of Opamp Non-Idealities
Finite DC Gain

\[ H(s) = -f_s \frac{C_s}{C_f} \frac{1}{s + f_s \frac{C_s}{C_f} \times \frac{L}{a}} \]

\[ H(s) = \frac{-\omega_0}{s + \omega_0 \times \frac{L}{a}} \]

\[ Q = \frac{a \times \omega_0}{\omega_0} \]

\[ Q = a \]

\[ \text{Finite DC gain same effect in S.C. filters as for C.T. filters} \]

Effect of Opamp Non-Idealities
Finite Opamp Bandwidth

Assumption- 
Opamp \( \rightarrow \) does not slew (will be revisited)
Opamp has only one pole \( \rightarrow \) exponential settling

Effect of Opamp Non-Idealities  
Finite Opamp Bandwidth

\[ H_{\text{actual}}(Z) = H_{\text{ideal}}(Z) \left[ 1 - e^{-k} + e^{k} \times \frac{C_f}{C_f + C_s} Z^{-1} \right] \]

where  
\[ k = \pi \times \frac{C_f}{C_f + C_s} \times \frac{f_t}{f_s} \]

\[ f_t \rightarrow \text{Opamp unity-gain-frequency}, \quad f_s \rightarrow \text{Clock frequency} \]


---

Effect of Opamp Finite Bandwidth  
on Filter Magnitude Response

\[ \frac{|T|_{\text{non-ideal}}}{|T|_{\text{ideal}}} (\text{dB}) \]

Magnitude deviation due to finite opamp unity-gain-frequency

Example: 2nd order bandpass with Q=25

Effect of Opamp Finite Bandwidth on Filter Magnitude Response

Example:
For 1dB magnitude response deviation:

1- $f_c/f_s = 1/12$
   $f_c/f_t \approx 0.04$
   $f_t > 25f_c$

2- $f_c/f_s = 1/32$
   $f_c/f_t \approx 0.022$
   $f_t > 45f_c$

3- Cont.-Time
   $f_c/f_s = 1/700$
   $f_t > 700f_c$

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<th>$f_c/f_t$</th>
<th>Active RC</th>
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<td>1/12</td>
<td>1/32</td>
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Effect of Opamp Finite Bandwidth
Maximum Achievable Q

Example:
For Q of 40 required
Max. allowable biquad Q
for peak gain change <10%

1- \( f_c/f_s = 1/32 \)
   \( f_c/f_s < 0.02 \)
   \( f_c > 50f_s \)

2- \( f_c/f_s = 1/12 \)
   \( f_c/f_s < 0.015 \)
   \( f_c > 28f_s \)

3- \( f_c/f_s = 1/6 \)
   \( f_c/f_s < 0.05 \)
   \( f_c > 20f_s \)


Effect of Opamp Finite Bandwidth on Filter Critical Frequency

Critical frequency deviation due to finite opamp unity-gain-frequency
Example: 2nd order filter

Effect of Opamp Finite Bandwidth on Filter Critical Frequency

Example:
For maximum critical frequency shift of <1%

1- \( f_c/f_s = 1/32 \)
   \( f_c/f_t \approx 0.028 \)
   \( f_t > 36f_c \)

2- \( f_c/f_s = 1/12 \)
   \( f_c/f_t \approx 0.046 \)
   \( f_t > 22f_c \)

3- Active RC
   \( f_c/f_t \approx 0.008 \)
   \( f_t > 125f_c \)


Sources of Distortion in Switched-Capacitor Filters

- Distortion induced by finite slew rate of the opamp
- Opamp output/input transfer function non-linearity
- Capacitor non-linearity
- Distortion incurred by finite setting time of the opamp
- Distortion due to switch clock feed-through and charge injection
What is Slewing?

Assume opamp is of a simple differential pair class A transconductance type

\[ V_{in} \]

\[ V_{o} \]

\[ C_s \]

\[ C_I \]

\[ I_s \]

\[ V_{i+} \]

\[ V_{i-} \]

\[ V_{cs} \]

\[ V_{max} \]

\[ I_{max} = I_{ss} \]

\[ I_o \]

\[ V_{max} \]

\[ V_{in} \]

Slope ~ \( g_m \)

\[ V_{cs} > V_{max} \rightarrow \text{Output current constant } I_o = I_{ss} \rightarrow \text{Slewing} \]

After \( V_{cs} \) is discharged enough to have \( V_{cs} < V_{max} \rightarrow \text{Linear settling} \)
Distortion Induced by Opamp Finite Slew Rate

Ideal Switched-Capacitor Output Waveform
Slew Limited Switched-Capacitor Output Settling

Distortion Induced by Finite Slew Rate of the Opamp

Distortion Induced by Opamp Finite Slew Rate

- Error due to exponential settling changes linearly with signal amplitude
- Error due to slew-limited settling changes non-linearly with signal amplitude (doubling signal amplitude X4 error)

\[ H_{Dk} = \frac{V_o}{S_f T_s} \frac{8\left(\sin\frac{a_o T_s}{2}\right)^2}{\pi k (k-2)} \]

\[ \rightarrow H_{D3} = \frac{V_o}{S_f T_s} \frac{8\left(\sin\frac{a_o T_s}{2}\right)^2}{15\pi} \]

Distortion Induced by Finite Slew Rate of the Opamp

- Note that for a high order switched capacitor filter \( \rightarrow \) only the last stage slewing will affect the output linearity (as long as the previous stages settle to the required accuracy)
  \( \rightarrow \) Can reduce slew limited linearity by using an amplifier with a higher slew rate \textit{only} for the last stage
  \( \rightarrow \) Can reduce slew limited linearity by using class A/B amplifiers
  - Even though the output/input characteristics is non-linear the significantly higher slew rate compared to class A amplifiers helps improve slew rate induced distortion
- In cases where the output is sampled by another sampled data circuit (e.g. an ADC or a S/H) \( \rightarrow \) no issue with the slewing of the output as long as the output settles to the required accuracy & is sampled at the right time

More Realistic Switched-Capacitor Circuit Slew Scenario

At the instant \( C_s \) connects to input of opamp (\( t=0^+ \))
- Opamp not yet active at \( t=0^+ \) due to finite opamp delay
- Feedforward path from input to output generates a voltage spike at the output
- Eventually, opamp becomes active & starts slewing
More Realistic SC Slew Scenario