EE247 Lecture 14

• Administrative issues
  - To avoid having EE247 & EE 142 or EE290C midterms on the same day, EE247 midterm moved from Oct. 20th to Thurs. Oct. 27th
  - Homework #4 due on Thurs. Oct. 20th
  - H.K.’s office hours changed from 3-4 to 2:30 to 3:30

• Data Converters
  - Spectral testing including windowing
  - Practical aspects of converter testing
    - Signal source
    - Clock generator
    - Evaluation board considerations
    - Evaluation set-up
    - Debugging
ADC Testing (Continued)

- Need to find "decision levels", i.e. input voltages at all code boundaries
  - One way: Adjust voltage source to find exact code trip points "code boundary servo"
  - More versatile: Histogram testing
    - Apply a signal with known distribution (ramp or sinusoid) and analyze digital code distribution at ADC output

- Spectral testing- Reveals ADC errors associated with dynamic behavior i.e. ADC performance as a function of frequency
  - Direct Discrete-Fourier-Transform (DFT) based measurements
  - Feasible when input signal can be locked to sampling frequency
  - Resticts input signal frequency
  - DFT measurements including windowing

Direct DFT
Choice of Number of Cycles & Number of Samples

To overcome frequency spectrum leakage problem:
  - Number of Cycles → integer

  - $N / \text{cycles} = f_s / f_x \rightarrow \text{non-integer}$

  - Preferable to have $N \rightarrow \text{power of 2}$ (FFT instead of DFT)
Windowing

- Spectral leakage can be virtually eliminated by “windowing” time samples prior to the DFT
  - Windows taper smoothly down to zero at the beginning and the end of the observation window
  - Time samples are multiplied by window coefficients on a sample-by-sample basis
- Windowing sinusoidal waveforms places the window spectrum at the sinewave frequency
  - Convolution in frequency

Window

- Time samples are multiplied by window coefficients on a sample-by-sample basis
- Multiplication in the time domain corresponds to convolution in the frequency domain
- Example: Nuttall window
Windowed Data

- Signal before windowing
- Signal after windowing
  - Windowing removes the discontinuity at block boundaries

Nuttall Window DFT

- Only first 20 bins shown
- Response attenuated by -120dB for bins > 5
- Lots of windows to choose from (go by name of inventor-Blackman, Harris...)
- Various window trade-off attenuation versus width (smearing of sinusoids)
DFT of Windowed Signal

- Spectra of signal before and after windowing
- Window gives ~ 100dB attenuation of sidelobes (use longer window for higher attenuation)
- Signal energy “smeared” over several (approximately 10) bins

Integer Cycles versus Windowing

- Integer number of cycles
  - Signal energy for a single sinusoid falls into single DFT bin
  - Requires careful choice of \( f_x \)
  - Ideal for simulations
  - Measurements \( \rightarrow \) need to lock \( f_x \) to \( f_s \) (PLL)

- Windowing
  - No restrictions on \( f_x \) \( \rightarrow \) no need to have the signal locked to \( f_s \) \( \rightarrow \) ideal for measurements
  - Signal energy (and harmonics) distributed over several DFT bins
  - Requires more data points for a fixed accuracy
Spectral ADC Testing

- ADC with B bits
- ±1 full scale input

B = 10;
delta = 2/(2^B-1);
th = -1+delta/2:delta:1-delta/2;
x = sin(...);
y = adc(x, th) * delta - 1;
s = abs(fft(y)/N*2); s = s(1:N/2);
f = (0:length(s)-1) / N;

ADC Output Spectrum

- Signal amplitude:
  - Bin: N * fx/fs + 1
    (Matlab arrays start at 1)
  - A = 0dBFS

- SNR?
ADC Simulated Output Spectrum

- Noise bins: all except signal bin
  \[ b_x = N * f_x / f_s + 1; \]
  \[ A_s = 20 \times \log_{10}(s(b_x)) \]
  \[ s(b_x) = 0; \]
  \[ A_n = 10 \times \log_{10}(\text{sum}(s.^2)) \]
  \[ \text{SNR} = A_s - A_n \]

- SNR = 62dB (10 bits)
- Computed SQNR = 6.02xN+1.76dB

Note: In a real circuit including thermal/flicker noise, the measured total noise is the sum of quantization & noise associated with the circuit.

Why is noise floor not @ 62dB?

- DFT bins act like an analog spectrum analyzer with bandwidth of \( f_s / N \), rather than \( f_s / 2 \)

- The DFT noise floor is \( 10 \times \log_{10}(N/2) \)dB below the actual noise floor (assuming white noise)

- For \( N=2048 \): 30dB
DFT Plot Annotation

1. Specify how many DFT points (N) are used, or
2. Shift DFT noise floor by \(10\log_{10}(N/2)\) dB, or
3. Normalize to "noise power in 1Hz bandwidth"

Spectral Performance Metrics
ADC Including Nonlinearities

- Signal S
- DC
- Distortion D
- Noise N

- Signal-to-noise ratio
  \(\text{SNR} = \frac{S}{N}\)
- Signal-to-distortion ratio
  \(\text{SDR} = \frac{S}{D}\)
- Signal-to-noise+distortion ratio
  \(\text{SNDR} = \frac{S}{(N+D)}\)
- Spurious-free dynamic range
  \(\text{SFDR}\)
Harmonic Components

- At multiples of $f_s$
- Aliasing:
  - $f_{\text{signal}} = f_s = 0.18 f_s$
  - $f_2 = 2 f_0 = 0.36 f_s$
  - $f_3 = 3 f_0 = 0.54 f_s$
    $\rightarrow 0.46 f_s$
  - $f_4 = 4 f_0 = 0.72 f_s$
    $\rightarrow 0.28 f_s$
  - $f_5 = 5 f_0 = 0.90 f_s$
    $\rightarrow 0.10 f_s$
  - $f_6 = 6 f_0 = 1.08 f_s$
    $\rightarrow 0.08 f_s$

Spectrum versus INL, DNL

Good DNL and poor INL suggests distortion problem

INL $\rightarrow$ Not fully symmetric
Relationship INL-SFDR/SNDR

- Depends on "shape" of INL
- Rule of Thumb: SFDR ≈ 20log\(2^B/\text{INL}\)
  - E.g. 1LSB INL, 10b → SFDR≈60dB
- Beware, this is of course only true under the same conditions at which the INL was taken, i.e. typically low input frequency

ADC Noise Example

- At right is the spectrum of a 10-Bit converter
- SNDR = 47dB – something’s amiss
- Distortion?
  SDR = 59.9dB – no
- Must be a noise problem, but is it thermal or quantization noise?
Noise Investigation

• At right is the spectrum of the same 10-Bit converter for \( f_x = f_s / 16 \)

• Since \( f_x \) divides \( f_s \), the quantization noise is periodic!

• It falls into the same bins the harmonics would normally occupy

• Hence
  – SNR \( \rightarrow \) thermal noise
  – SDR \( \rightarrow \) quantization noise (apparently the culprit)

\[
\begin{array}{c|c|c|c|c}
N & \text{SNR} & \text{SDR} & \text{SNDR} & \text{SFDR} \\
4096 & 65.0 \text{dB} & 48.4 \text{dB} & 47.2 \text{dB} & 49.5 \text{dB}
\end{array}
\]

Noise Investigation

• After re-design and re-fab. Same test performed:
  \( f_x = f_s / 16 \)

• The quantization noise is not a major error:
  SDR = 74dB

• SNR = 56.1dB
  This corresponds to Gaussian thermal noise with variance \( \Delta/2 \) at the converter input ... a reasonable design choice

\[
\begin{array}{c|c|c|c|c}
N & \text{SNR} & \text{SDR} & \text{SNDR} & \text{SFDR} \\
4096 & 56.1 \text{dB} & 73.9 \text{dB} & 55.0 \text{dB} & 77.5 \text{dB}
\end{array}
\]
Noise Investigation

- The DNL and INL confirm the good result.

- But the INL shows some “bowing” … let’s see if our test masked a distortion problem.

![DNL and INL of 10 Bit converter]

- For that we revert to simulating with $f_s/f_x$ non-integer.

- A 3rd harmonic is barely visible.

- How can we “lift” it out of the noise?

![Amplitude vs Frequency]

N = 4096
SNR = 55.9dB  SDR = 76.4dB
SNDR = 55.1dB  SFDR = 77.3dB
Noise Investigation

- Increasing $N$, the number of samples (and hence the measurement or simulation time) distributes the noise over more bins
- More bins $\rightarrow$ less noise power per bin (total noise stays constant)
- $\text{SFDR} = 78\text{dB}$ for 10Bit is acceptable in many applications

![Amplitude vs Frequency Graph](image)

- $N = 65536$
- $\text{SNR} = 55.9\text{dB}$
- $\text{SDR} = 77.9\text{dB}$
- $\text{SNDR} = 55.2\text{dB}$
- $\text{SFDR} = 78.5\text{dB}$

SNR Degradation due to DNL

- For ideal quantizer we assumed uniform quantization error over $\pm \Delta/2$
- Let’s now add uniform DNL over $\pm 0.5\text{LSB}$ and repeat math...

![DNL Plot](image)

[Source: Ion Opris]
SNR Degradation due to DNL

- Integrate triangular pdf:
  \[
  \overline{e^2} = 2 \int_{0}^{\Delta} (1 - e) \frac{e^2}{\Delta} de = \frac{\Delta^2}{6} \quad \Rightarrow \text{SNR} = 6.02 \cdot N - 1.25 \text{ [dB]}
  \]

- Compare to ideal quantizer:
  \[
  \overline{e^2} = \int_{-\Delta/2}^{+\Delta/2} \frac{e^2}{\Delta} de = \frac{\Delta^2}{12} \quad \Rightarrow \text{SNR} = 6.02 \cdot N + 1.76 \text{ [dB]}
  \]

SNR Degradation due to DNL

- More general case:
  - Uniform quantization error $\pm 0.5\Delta$
  - Uniform DNL error $\pm \text{DNL}$ [LSB]
  - Convolution yields trapezoid
  - SQNR becomes:
    \[
    SQNR = \frac{1}{2} \left( \frac{2^N \Delta^2}{2} \right) + DNL^2 \]
    \[
    \frac{\Delta^2}{12} \frac{1}{3}
    \]

3dB
SNR Degradation due to DNL

- Degradation in dB: \[ SNR_{deg} = 1.76 - 10 \log \left( \frac{1}{8} \frac{1}{1 + \frac{DNL^2}{3}} \right) \]

Uniform DNL?

- DNL distribution of 12-bit ADC test chip
- Not quite uniform...
Effective Number of Bits (ENOB)

• Is a 12-Bit converter with 68dB SNDR really a 12-Bit converter?

• Effective Number of Bits

\[
ENOB = \frac{SNDR - 1.76dB}{6.02dB} = \frac{68 - 1.76}{6.02} = 11.0\text{Bits}
\]

ENOB

• At best, we get "ideal" ENOB only for zero thermal noise, zero DNL, zero INL

• Low noise is costly, 4x penalty in power per (ENOB-) bit or 6dB SNDR

• Rule of thumb for good performance /power tradeoff: ENOB < N-1
R. H. Walden, "Analog-to-digital converter survey and analysis," *IEEE J. on Selected Areas in Communications*, pp. 539-50, April 1999

Converter Testing
Practical Aspects
Just Got Silicon Back...

- Now what?
- Practical aspects of converter testing
- Equipment requirements
- Pitfalls

Direct ADC-DAC Test

- Need a very good DAC
- Actually a good way to "get started"...
Direct ADC-DAC Test

• Issues to beware of:
  – Linearity of the signal generator output has to be much better than ADC linearity
  – Spectrum analyzer nonlinearities
    → May need to build/purchase filters to address one or both above problems
  – Clock generator signal jitter

Filtering ADC Input Signal

Signal Generator

Output Signal Amplitude

Bandpass Filter

ADC

Input Signal Amplitude

 DAC

Notch Filter

Spectrum Analyzer

Notch Filter

Bandpass

or Lowpass Filter

Device Under Test (DUT)

Signal Generator

Clock Generator

0 ... f

f_in

2f_in

3f_in

4f_in

... f

ADC Input Signal Amplitude

0 ... f

f_in

2f_in

3f_in

4f_in

... f

Bandpass Filter

Signal Generator Output Signal Amplitude
Filtering Input to Spectrum Analyzer
Prevent Signal Distortion Incurred by Spec. Analyzer

DAC Output Signal Amplitude

Spectrum Analyzer Input Signal Amplitude

ADC Test Setup

Specs?

Signal Generator

Evaluation Board?

How to get data across?

ADC

Data Acquisition

PC

Specs?

Clock Generator


EECS 247 Lecture 14: Data Converters © 2005 H.K. Page 39

EECS 247 Lecture 14: Data Converters © 2005 H.K. Page 40
Example: State-Of-The-Art ADC (2001)


<table>
<thead>
<tr>
<th>Technology &amp; Supply</th>
<th>0.35micron technology &amp; 3V Supply</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>14 bits</td>
</tr>
<tr>
<td>Conversion Rate</td>
<td>75 MSPS</td>
</tr>
<tr>
<td>Input Range</td>
<td>2 Vpp differential</td>
</tr>
<tr>
<td>SNR @ Nyquist</td>
<td>73 dB</td>
</tr>
<tr>
<td>SFDR @ Nyquist</td>
<td>88 dB</td>
</tr>
<tr>
<td>DNL</td>
<td>0.615SB</td>
</tr>
<tr>
<td>INL</td>
<td>2.015SB</td>
</tr>
</tbody>
</table>

• Your converter will perform even better...
• Testing a high performance converter may be just as challenging as designing it!
• Key to success is to be aware of test setup and equipment limitations

Signal Source

• Need: SFDR>95dB @ f\textsubscript{in}=f\textsubscript{s}/2=37.5MHz
• Let’s see, how about the "value priced" signal generator available in most labs...
  • f=0...15MHz
  • Harmonic distortion (f>1MHz): -35dBc
    → Does not cover the required frequency range & poor linearity
A Better Signal Source

• OK, now we've spent about $40k, this should work now... (?)
  • f=100kHz...3GHz
  • Harmonic distortion (f>1MHz): -30dBc!
  • Still need a filter to eliminate harmonic distortion!

Filtering Out Harmonics

• Given HD=-30dBc, we need a stopband rejection > 65dB to get SFDR>95dB
Available Filters

Elliptical Function Bandpass Filters 1kHz to 20MHz

- Fixed frequency filters!
- Want to test at many frequencies → Need to have many different filters!

Stopband to Passband Bandwidth Ratios

<table>
<thead>
<tr>
<th>Series Number</th>
<th>BWR</th>
<th>Stopband Attenuation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q34</td>
<td>4.0:1</td>
<td>-40dBc</td>
</tr>
<tr>
<td>Q40</td>
<td>4.0:1</td>
<td>-40dBc</td>
</tr>
<tr>
<td>Q36</td>
<td>10.0:1</td>
<td>-60dBc</td>
</tr>
<tr>
<td>Q24</td>
<td>2.5:1</td>
<td>-60dBc</td>
</tr>
<tr>
<td>Q70</td>
<td>3.5:1</td>
<td>-60dBc</td>
</tr>
<tr>
<td>Q56</td>
<td>3.5:1</td>
<td>-60dBc</td>
</tr>
</tbody>
</table>

Example: ADC Linearity Test
**Filter Distortion**

- Beware: The filters themselves could also introduce distortion
- Distortion is usually not specified, need to contact manufacturer directly!
- Often guaranteed: HD<-85dBC,
- Don't trust your filters blindly...
Clock Generator

• Let us check if for the clock a "value-priced" signal generator will suffice...

• No! The clock signal controls sampling instants – which we assumed to be precisely equi-distant in time (period T)

• Variability in T causes errors
  – "Aperture Uncertainty" or "Aperture Jitter"

• How much Jitter can we tolerate?

Clock Jitter

• Sampling jitter adds an error voltage proportional to the product of (t_J - t_0) and the derivative of the input signal at the sampling instant

• Jitter doesn't matter when sampling dc signals (x'(t_0) = 0)
Clock Jitter

- The error voltage is
  \[ e = x'(t_0)(t_J - t_0) \]

Jitter Example

### Sinusoidal input
- **Amplitude:** \[ A \]
- **Frequency:** \[ f_s \]

\[ x(t) = A \sin(2\pi f_s t) \]

\[ x'(t) = 2\pi f_s A \cos(2\pi f_s t) \]

\[ |x'(t)|_{\text{max}} \leq 2\pi f_s A \]

### Worst case
- \[ A = \frac{A_{FS}}{2} \]
- \[ f_s = \frac{f_s}{2} \]

\[ |e(t)| \ll \frac{A_{FS}}{2^{1+b}} \]

\[ dt \ll \frac{l}{2^b \pi f_s} \]

### Requirement:
- \[ |e(t)| \leq |x'(t)| dt \]
- \[ |e(t)| \leq |2\pi f_s A| dt \]

<table>
<thead>
<tr>
<th># of Bits</th>
<th>( f_s )</th>
<th>( dt )</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>10 MHz</td>
<td>0.5 ps</td>
</tr>
<tr>
<td>12</td>
<td>100 MHz</td>
<td>0.8 ps</td>
</tr>
<tr>
<td>8</td>
<td>1000 MHz</td>
<td>1.2 ps</td>
</tr>
</tbody>
</table>
Law of Jitter

- The worst case looks pretty stringent … what about the “average”?
- Let’s calculate the mean squared jitter error (variance)
- If we’re sampling a sinusoidal signal
  \[ x(t) = A \sin(2\pi f_c t), \]
  then
  \[ x'(t) = 2\pi f_c A \cos(2\pi f_c t) \]
  \[ E\{[x'(t)]^2\} = 2\pi^2 f_c^2 A^2 \]
- Assume the jitter has variance \( E\{(t_j - t_0)^2\} = \tau^2 \)

Law of Jitter

- If \( x'(t) \) and the jitter are independent
  \[ E\{[x'(t)(t_j - t_0)]^2\} = E\{[x'(t)]^2\} E\{(t_j - t_0)^2\} \]

- Hence, the jitter error power is
  \[ E\{e^2\} = 2\pi^2 f_c^2 A^2 \tau^2 \]

- If the jitter is uncorrelated from sample to sample, this “jitter noise” is white
Law of Jitter

\[ DR_{jitter} = \frac{A^2}{2} \frac{1}{f_s^2 A^2 \tau^2} \]

\[ = \frac{1}{2\pi f_s \tau^2} \]

\[ = -20 \log_{10}(2f_s\tau) \]

ADC under test:
SNR=73dB
\[ f_{in}=37.5MHz \]
⇒ \( \tau < 1 \text{ps rms} \)

More on Jitter

- Once we have a good enough generator, other circuit and test setup related issues may determine jitter, but...
- Usually, clock jitter in the single-digit pico-second range can be prevented by appropriate design techniques
  - Separate supplies
  - Separate analog and digital clocks
  - Short inverter chains between clock source and destination
- Few, if any, other analog-to-digital conversion non-idealities have the same symptoms as sampling jitter:
  - RMS noise proportional to input frequency
  - RMS noise proportional to input amplitude
- In cases where clock jitter limits the dynamic range, it’s easy to tell, but may be difficult to fix...
Evaluation Board

- Planning begins with converter pin-out
  - Example of poor pin-out → clock pin right next to a digital output...
- Not "Black Magic", but weeks of design time and studying
- Key aspects
  - Supply/ground routing, bypass capacitors
  - Coupling between signals
- Good idea to look at ADC vendor datasheets for example layouts/schematics/application notes

Vendor Eval Board Layout

[Analog Devices AD9235 Data Sheet]
One thing to remember...

- A converter does not just have one "input" pin but:
  - Clock
  - Power Supply, Ground
  - Reference Voltage
- For good practices on how to avoid issues see e.g.:
  - Analog Devices Application Note 345: "Grounding for Low-and-High-Frequency Circuits"
  - Maxim Application Note 729: "Dynamic Testing of High-Speed ADCs, Part 2"

How to Get the Bits Off Chip?

- "Full swing" CMOS signaling works well for $f_{\text{CLK}} < 100\text{MHz}$
- But we want to build faster ADCs...
- Alternative to CMOS: LVDS – Low Voltage Differential Signaling
- LVDS vs. CMOS:
  - Higher speed, more power efficient at high speed
  - Two pins/bit!