DAC Converters (continued)
- Reconstruction filter
- DAC self calibration techniques
  - Current copiers
  - Dynamic element matching

ADC Converters
- Sampling
  - Sampling switch induced distortion
  - Sampling switch charge injection
    - Complementary switch
    - Use of dummy device
    - Bottom-plate switching

DAC Reconstruction Filter
- Need for and requirements depend on application

- Tasks:
  - Correct for sinc distortion
  - Remove “aliases” (stair-case approximation)
Reconstruction Filter Options

- Digital and SC filter possible only in combination with oversampling (signal bandwidth $B << f_s/2$)
- Digital filter
  - Band limits the input signal → prevent aliasing
  - Could also provide high-frequency pre-emphasis to compensate in-band sinc amplitude droop associated with the inherent DAC ZOH function

DAC Implementation Examples

- Untrimmed segmented

- Current copiers:

- Dynamic element matching:
Two sources of systematic error:
- Finite current source output resistance
- Voltage drop due to finite ground bus resistance
Current-Switched DACs in CMOS

\[ I_j = k\left( V_{GSS} - V_{th}\right)^2 \]

\[ V_{GSS} = V_{DD} - 4RI, \quad V_{GSS} = V_{DD} - 7RI \]

\[ I_2 = k\left( V_{GSS} - V_{th}\right)^2 = I_1 \left( 1 - \frac{4RI}{V_{GSS} - V_{th}} \right)^2 \]

\[ R_{on} = \frac{2I_1}{V_{GSS} - V_{th}} \]

\[ \to I_2 = I_1 \left( \frac{4R_{on}}{2} \right)^2 = I_1 \left( 1 - 4R_{on} \right) \]

\[ \to I_1 = I_1 \left( \frac{7R_{on}}{2} \right)^2 = I_1 \left( 1 - 7R_{on} \right) \]

\[ \to I_2 = I_1 \left( \frac{9R_{on}}{2} \right)^2 = I_1 \left( 1 - 9R_{on} \right) \]

\[ \to I_3 = I_1 \left( \frac{10R_{on}}{2} \right)^2 = I_1 \left( 1 - 10R_{on} \right) \]

**Assumption:** \( R_I \) is small compared to transistor gate overdrive

\[ \Rightarrow \text{Desirable to have } g_m \text{ small} \]

Current-Switched DACs in CMOS
Example: INL of 7 unit element DAC

Example: 7 unit element current source DAC- assume \( g_m \cdot R = 1/100 \)

- If switching of current sources sequential (1-2-3-4-5-6-7)
  \[ \Rightarrow \text{INL} = +0.25\text{LSB} \]

- If switching of current sources symmetrical (4-3-5-2-6-7)
  \[ \Rightarrow \text{INL} = +0.09, -0.058\text{LSB} \]
Current-Switched DACs in CMOS

Example: DNL of 7 unit element DAC

<table>
<thead>
<tr>
<th>Input</th>
<th>DNL [LSB]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>-0.2</td>
</tr>
<tr>
<td>2</td>
<td>-0.1</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0.1</td>
</tr>
<tr>
<td>5</td>
<td>0.2</td>
</tr>
<tr>
<td>6</td>
<td>-0.2</td>
</tr>
<tr>
<td>7</td>
<td>-0.1</td>
</tr>
</tbody>
</table>

Example: 7 unit element current source DAC- assume \( g_m x R = 1/100 \)

- If switching of current sources sequential (1-2-3-4-5-6-7)
  \( \rightarrow DNL_{max} = +0.15\text{LSB} \)
- If switching of current sources symmetrical (4-3-5-2-6-7 )
  \( \rightarrow DNL = +0.15\text{LSB} \)

More recent published DAC using symmetrical switching built in 0.35\( \mu \)m/3V analog/1.9V digital, area x10 smaller compared to previous example.
A Self-Calibration Technique for Monolithic High-Resolution D/A Converters

D. WOUTER J. GROENEVELD, HANS J. SCHOUWENAARS, SENIOR MEMBER, IEEE, HENK A. H. TERMEER, AND CORNELIS A. A. BASTIAANSEN

Fig. 2. Calibration principle. (a) Calibration. (b) Operation.

16-bit DAC (6+10)- MSB DAC uses calibrated current sources
Current Divider Accuracy

\[ I_d = \frac{I_{d1} + I_{d2}}{2} \]

\[ dI_d = \frac{I_{d1} - I_{d2}}{I_d} \]

\[ dI_d = \frac{2}{I_d} \left( \frac{dW/\omega}{W/L} + dV_{th} \right) \]

Ideal Current Divider

Real Current Divider

M1 & M2 mismatched

→ Problem: Device mismatch could severely limit DAC accuracy
Dynamic Element Matching for High-Accuracy Monolithic D/A Converters

RUDY J. VAN DE PLASSCHE

Fig. 2. (a) New current divider schematic diagram. (b) Time dependence of various currents in the new divider.

Dynamic Element Matching

During $\Phi_1$

\[
\begin{align*}
I_1^{(1)} &= \frac{1}{2}I_o(1+\Delta_I) \\
I_1^{(2)} &= \frac{1}{2}I_o(1-\Delta_I)
\end{align*}
\]

During $\Phi_2$

\[
\begin{align*}
I_2^{(1)} &= \frac{1}{2}I_o(1+\Delta_I) \\
I_2^{(2)} &= \frac{1}{2}I_o(1-\Delta_I)
\end{align*}
\]

\[
\langle I_2 \rangle = \frac{I_2^{(1)} + I_2^{(2)}}{2} = I_o(I-\Delta_I) + (1+\Delta_I)
\]

\[
= \frac{I_o}{2} \text{ for } \Delta_I \text{ small}
\]

During $\Phi_2$

\[
\begin{align*}
I_1 &= I_2 \\
I_2 &= \text{error } \Delta_I
\end{align*}
\]
Dynamic Element Matching

During $\Phi_1$

\[
I_1^{(1)} = \frac{1}{2} I_o (1 + \Delta_1)
\]

\[
I_1^{(2)} = \frac{1}{2} I_o (1 - \Delta_1)
\]

\[
I_2^{(1)} = \frac{1}{4} I_o (1 + \Delta_2)
\]

\[
I_2^{(2)} = \frac{1}{4} I_o (1 - \Delta_2)
\]

\[
\langle I_0 \rangle = \frac{I_1^{(1)} + I_1^{(2)}}{2}
\]

\[
= \frac{1}{4} I_o (1 + \Delta_2)(1 + \Delta_1) + (1 - \Delta_2)(1 - \Delta_1)
\]

\[
= \frac{1}{4} I_o (1 + \Delta_1 \Delta_2)
\]

During $\Phi_2$

\[
I_1^{(1)} = \frac{1}{4} I_o (1 - \Delta_1)
\]

\[
I_1^{(2)} = \frac{1}{4} I_o (1 + \Delta_1)
\]

\[
I_2^{(1)} = \frac{1}{4} I_o (1 - \Delta_2)
\]

\[
I_2^{(2)} = \frac{1}{4} I_o (1 + \Delta_2)
\]

\[
\langle I_0 \rangle = \frac{I_2^{(1)} + I_2^{(2)}}{2}
\]

\[
= \frac{1}{4} I_o (1 + \Delta_1)(1 + \Delta_2) + (1 - \Delta_2)(1 - \Delta_1)
\]

\[
= \frac{1}{4} I_o (1 + \Delta_1 \Delta_2)
\]

E.g. $\Delta_1 = \Delta_2 = 1\% \rightarrow$ matching error is $(1\%)^2 = 0.01\%$
Summary
D/A Converter

- D/A architecture
  - Unit element – complexity proportional to $2^B$ - excellent DNL
  - Binary weighted - complexity proportional to $B$ - poor DNL
  - Segmented - unit element MSB($B_1$) + binary weighted LSB($B_2$) → complexity proportional to $(2^{B_1} - 1) + B_2$ – DNL compromise between the two
- Static performance
  - Component matching
- Dynamic performance
  - Glitches
- DAC improvement techniques
  - Symmetrical DAC element switching rather than sequential switching
  - Current source self calibration
  - Dynamic element matching

MOS Sampling Circuits
Re-Cap

• How can we build circuits that "sample"

Ideal Sampling

• In an ideal world, zero resistance sampling switches would close for the briefest instant to sample a continuous voltage $v_{IN}$ onto the capacitor $C$
• Not realizable!
Ideal T/H Sampling

- $V_{out}$ tracks input when switch is closed
- Grab exact value of $V_{in}$ when switch opens
- "Track and Hold" (T/H) (often called Sample & Hold)

![Ideal T/H Sampling Diagram]

Continuous Time

T/H signal (SD Signal)

Clock

DT Signal
Practical Sampling

- Switch induced noise power $\rightarrow kT/C$
- Finite $R_{sw} \rightarrow$ limited bandwidth
- $R_{sw} = f(V_{in}) \rightarrow$ distortion
- Switch charge injection
- Clock jitter

$kT/C$ Noise

$$\frac{k_B T}{C} \leq \frac{\Lambda^2}{12}$$

$$C \geq 12k_B T \left(\frac{2^B - 1}{V_{FS}}\right)^2$$

In high resolution ADCs $kT/C$ noise usually dominates overall error (power dissipation considerations).

<table>
<thead>
<tr>
<th>$B$</th>
<th>$C_{\min}$ $(V_{FS} = 1\text{V})$</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>0.003 pF</td>
</tr>
<tr>
<td>12</td>
<td>0.8 pF</td>
</tr>
<tr>
<td>14</td>
<td>13 pF</td>
</tr>
<tr>
<td>16</td>
<td>206 pF</td>
</tr>
<tr>
<td>20</td>
<td>52,800 pF</td>
</tr>
</tbody>
</table>
Acquisition Bandwidth

- The resistance $R$ of switch $S1$ turns the sampling network into a lowpass filter with risetime $= RC = \tau$

- Assuming $V_{in}$ is constant during the sampling period and $C$ is initially discharged

$$V_{out}(t) = V_{in}(1 - e^{-t/\tau})$$

Switch On-Resistance

$$V_{in} - V_{out}\left(t = \frac{1}{2f_s}\right) << \Delta$$

$$V_{in}e^{-t/2f_s} << \Delta$$

Worst Case: $V_{in} = V_{FS}$

$$\tau << \frac{T}{2 \ln\left(2^B - 1\right)}$$

$$R << \frac{1}{2f_sC \ln\left(2^B - 1\right)}$$

Example:

- $B = 14$, $C = 13\text{pF}$, $f_s = 100\text{MHz}$
- $T/\tau >> 19.4$, $R << 40\Omega$
Switch On-Resistance

\[ I_{D_{\text{in,side}}} = \mu C_{ox} \frac{W}{L} \left( V_{GS} - V_{TH} - \frac{V_{DS}}{2} \right) V_{DS} \]

\[ R_{ON} = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{GS} - V_{th})} = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{DS} - V_{th} - V_{in})} \]

for \( R_o = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{DS} - V_{th})} \)

\[ R_{ON} = \frac{R_o}{V_{in}} \frac{V_{in}}{V_{DS} - V_{th}} \]

Sampling Distortion

\[ V_{out} = V_{in} \left( l - e^{\frac{-T}{2\pi (\frac{V_{in}}{V_{in} - V_{th}})}} \right) \]

10bit ADC & \( T/\tau = 10 \)

\[ V_{DS} - V_{th} = 2V \quad V_{FS} = 1V \]
Sampling Distortion

- SFDR is very sensitive to sampling distortion
- Solutions:
  - Overdesign → Larger switches
    → increased switch charge injection
    → increased switch drain & source C
  - Complementary switch
  - Maximize $V_{DD}/V_{FS}$ → decreased dynamic range
  - Constant $V_{GS}$? $(V_{in})$
    → ...

10bit ADC $T/\tau = 20$
$V_{DD} - V_{th} = 2V$  $V_{FS} = 1V$

Practical Sampling

- $kT/C$ noise
  $$C \geq 12kT \left( \frac{2^n - 1}{V_{FS}} \right)^2$$
- Finite $R_{sw}$ → limited bandwidth
  $$R \ll -\frac{1}{2f_c C \ln(2^n - 1)}$$
- $g_{sw} = f(V_{in})$ → distortion
  $$g_{ON} = g_o \left( 1 - \frac{V_{in}}{V_{DD} - V_{th}} \right)$$
  for $g_o = \mu C_m \frac{W}{L}(V_{DD} - V_{th})$
- Switch charge injection
- Clock jitter
Sampling Distortion
Effect of Supply Voltage

- HD3 increases by \((\frac{V_{DD1}}{V_{DD2}})^2\)
- HD2 increases by \((\frac{V_{DD1}}{V_{DD2}})\)

SFDR sensitive to sampling distortion - improve linearity by:
- Larger VDD
- Higher sampling bandwidth

Solutions:
- Overdesign - Larger switches
  - Increased switch charge injection
  - Increased nonlinear S&D junction cap.
- Maximize VDD/VFS
  - Decreased dynamic range if VDD constant.
- Complementary switch
- Constant & max. \(V_{GS} = f(V_p)\)

10bit ADC & \(T/\tau = 10\)
\(V_{DD} - V_{th} = 2V\) \(V_{FS} = 1V\)

10bit ADC & \(T/\tau = 10\)
\(V_{DD} - V_{th} = 4V\) \(V_{FS} = 1V\)
Complementary Switch

- Complementary n & p switch advantages:
  - Increases the overall conductance
  - Linearize the switch conductance for the range $V_{tp} < V_{in} < V_{dd} - V_{tn}$

Complementary Switch Issues
Supply Voltage Evolution

- Supply voltage scales down with technology scaling
- Threshold voltages do not scale accordingly

Complementary Switch
Effect of Supply Voltage Scaling

- As supply voltage scales down input voltage range for constant $g_o$ shrinks
  - Complementary switch not effective when $V_{dd}$ becomes comparable to $V_{th}$

Boosted & Constant $V_{GS}$ Sampling

- Increase gate overdrive voltage as much as possible + keep $V_{GS}$ constant
  - Switch overdrive voltage is independent of signal level
  - Error from finite $R_{on}$ is linear (to first order)
  - Lower $R_{on}$ achieved $\rightarrow$ lower time constant
**Constant $V_{GS}$ Sampling**

Input signal ($V_i$) boosts the clock ($V_g$) leading to $V_{dd}$.

**Constant $V_{GS}$ Sampling Circuit**

- VP1: 100ns
- VS1: 1.5V, 1MHz
- $V_{dd}$ = 3V
- $V_{dd}$ and $V_i$ are voltage levels at the switch source terminal.

This Example: All device sizes: 10µ/0.35µ
All capacitor size: 1pF

Sampling switch & C
Clock Voltage Doubler

- Clock period: 100ns
- $V_{DD}=3V$
- $R_1 \ & R_2 = 1\, \text{G} \Omega$
- *dummy resistors added for simulation only

Constant $V_{GS}$ Sampler: $\Phi$ LOW

- Sampling switch $M_{11}$ is OFF
- $C_3$ charged to $V_{DD}$
Constant $V_{GS}$ Sampler: $\Phi$ HIGH

- $C_3$ previously charged to $V_{DD}$
- $M_8$ & $M_9$ are on: $C_3$ across G-S of $M_{11}$
- $M_{11}$ on with constant $V_{GS} = V_{DD}$

Constant $V_{GS}$ Sampling

- Input Switch $V_{Gate}$
- Chold Signal
- Input Signal
Complete Circuit


Advanced Clock Boosting

Advanced Clock Boosting Technique

- Gate tracks average of input and output, reduces effect of I·R drop at high frequencies
- Bulk also tracks signal ⇒ reduced body effect (technology used allows connecting bulk to S)
- SFDR = 76.5dB at $f_{in}=200$MHz (measured)

Switch Off-Mode Feedthrough Cancellation

High-pass feedthrough paths past an open switch  Feedthrough cancellation with a dummy switch
Practical Sampling

- \( R_{sw} = f(V_{in}) \to \text{distortion} \)
- Switch charge injection

Sampling Switch Charge Injection

- First assume \( V_{in} \) is a DC voltage
- When switch turns off \( \to \) offset voltage induced on \( C_s \)
- Why?
Sampling Switch Charge Injection

MOS xtor operating in triode region
Cross section view

- Channel $\rightarrow$ distributed RC network
- Channel to substrate junction capacitance $\rightarrow$ distributed & variable
- Over-lap capacitance $C_{ov} = L_D \cdot W \cdot C_{ox}$ associated with GS & GD overlap

Switch Charge Injection

Slow Clock

- Since clock fall time $\gg$ device speed
  $\Rightarrow$ During the period ($t$- to $t_{off}$) current in channel discharges channel charge into low impedance signal source
- Only source of error $\Rightarrow$ Charge transfer from $C_{ov}$ into $C_s$
Switch Charge Injection
Slow Clock

\[
\Delta V = -\frac{C_{ov}}{C_{ov} + C_s} (V_i + V_{ih} - V_L)
\]
\[
= \frac{C_{ov}}{C_s} (V_i + V_{ih} - V_L)
\]
\[
V_o = V_i (1 + \varepsilon) + V_{os}
\]

where \( \varepsilon = \frac{C_{ov}}{C_s} \); 

\[
V_{os} = -\frac{C_{ov}}{C_s} (V_{ih} - V_L)
\]

Switch Charge Injection
Slow Clock- Example

\( V_{IN} \) to \( V_O \)

\( M1 \)

\( C_s = 1 \mu F \)

\( C_{ov} = 0.3 fF/\mu \)

\( C_{so} = 5 fF/\mu^2 \)

\( V_{ih} = 0.5 V \)

\( \varepsilon = -\frac{C_{so}}{C_s} = -\frac{12 \mu A \times 0.3 fF/\mu}{1 \mu F} = -36 \% \rightarrow 7 \text{-bit} \)

\( V_{os} = -\frac{C_{so}}{C_s} (V_{ih} - V_L) = -1.8 mV \)
Switch Charge Injection
Fast Clock

- Sudden gate voltage drop $\rightarrow$ no gate voltage to establish current in channel $\rightarrow$
  channel charge has no choice but to escape out towards S & D

\[
\Delta V = \frac{C_{ov}}{C_{ov} + C_s} (V_G - V_L) - \frac{1}{2} \frac{C_s}{C_c} \left( V_G - V_L \right) - \frac{1}{2} \frac{W C_{ov} L}{C_c} \left[ (V_G - V_L) \right] \approx \frac{1}{2} \frac{W C_{ov} L}{C_c} (V_G - V_L) - \frac{1}{2} \frac{W C_{ov} L (V_G - V_s)}{C_c}
\]

where $\epsilon = \frac{I}{2} \frac{W C_{ov} L}{C_c}$

- Assumption $\rightarrow$ channel charge divided equally between S & D
- Source of error $\rightarrow$ channel charge transfer + charge transfer from $C_{ov}$ into $C_s$
Switch Charge Injection
Fast Clock- Example

\[ C_{in} = 0.31 F/\mu \quad C_{in} = 5 F/\mu^2 \quad V_{th} = 0.5 V \quad V_{in} = 3 V \]

\[ \varepsilon = -\frac{1}{2} \frac{WLC_{ox}}{C_i} \times 12 \mu \times 0.35 x 5 F/\mu \times 1 pF = -2.1 \% \rightarrow 4.5 \rightarrow b \]

\[ V_{in} = \frac{C_{in}}{C_i} (V_{in} - V_L) \quad \frac{1}{2} \times \frac{W}{C_{ox}} (V_{in} - V_L) = -9 mV - 26.3 mV = -45.3 mV \]

→ Both errors are a function of clock fall time, input voltage level, source impedance & sampling capacitance
Switch Charge Injection
Error Reduction

• How do we reduce the error?
  → Reduce switch?

\[ \tau = R_{on} C_i = \frac{C_i}{\mu C_i W L (V_{GS} - V_{th})} \]
\[ \Delta V_s = \frac{Q_s}{2 C_i} \]
\[ FOM = \tau \times \Delta V_s = \frac{C_i}{\mu C_i W L (V_{GS} - V_{th})} \times \frac{W C_i L (V_{GS} - V_{th} - V_{th})}{C_i} \]
\[ FOM = \frac{L}{\mu} \]

→ Reducing switch size increases \( \tau \) → increased distortion → not a viable solution
→ Small \( \tau \) and \( \Delta V \) → use minimum channel length
→ For a given technology \( \tau \times \Delta V = \text{conts.} \)

Sampling Switch Charge Injection
Summary

• Extra charge injected onto sampling capacitor @ switch device turn-off
  – Charge sharing with \( C_{ov} \)
  – Channel charge transfer

• Issues:
  – DC offset
  – Input dependant error voltage → distortion

• Solutions:
  – Complementary switch?
  – Addition of dummy switches?
  – Bottom-plate sampling?
Switch Charge Injection
Complementary Switch

• In slow clock case if area of devices are equal → effect of overlap capacitor for n & p devices cancel to first order (matching n & p area)

Switch Charge Injection
Complementary Switch
Fast Clock

\[ Q_{b-n} = W_n C_n I_n \left( V_{ih} - V_l - V_{th,n} \right) \]
\[ Q_{b-p} = W_p C_p I_p \left( V_{ih} - V_l - V_{th,p} \right) \]
\[ \Delta V_o = \frac{I}{2} \left( \frac{Q_{b-p}}{C_p} - \frac{Q_{b-n}}{C_n} \right) \]
\[ V_o = V_i (1 + \epsilon) + V_{ref} \]
\[ \epsilon = \frac{1}{2} \frac{W_n C_n I_n + W_p C_p I_p}{C_i} \]

• In fast clock case
  • Offset cancelled for equal device area
  • Input voltage dependant error worse!
Switch Charge Injection

Dummy Switch

- Dummy switch same L as main switch but half W
- Main device clock goes low, dummy device goes high → dummy switch acquires same amount of channel charge main switch needs to lose
- Effective only if exactly half of the charge transferred to M2 and good matching between clock fall/rise

To guarantee half of charge goes to each side → create the same environment on both sides
- Add C equal to sampling capacitor to the other side of the switch + add fixed resistor
- Degrades sampling bandwidth
**Dummy Switch**

**Dummy Switch Effectiveness Test**

- Dummy switch
  \( \Rightarrow W = 1/2 W_{\text{main}} \)
- Note large \( Ls \)
  \( \Rightarrow \) good device area matching


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**Switch Charge Injection**

**Bottom Plate Sampling**

- Switches M2A@ B are opened slightly earlier compared to M1A&B
  \( \Rightarrow \) Injected charge by the opening of M2AB is constant & eliminated when used differentially
- Since bottom plate of \( C_s \) is open when M1A&B are opened \( \Rightarrow \) no charge injected on \( C_s \)