EE247 Lecture 19

ADC Converters

• Sampling (continued)
  – Sampling switch charge injection
    • Complementary switch
    • Use of dummy device
    • Bottom-plate switching
  – Track & hold circuits
    – T/H circuit incorporating gain & offset cancellation
• ESD protection impact on converter performance
• ADC architectures
  - Nyquist rate ADCs
  - Oversampled ADCs

Switch Charge Injection
Complementary Switch

• In slow clock case if area of n & p devices are equal \( \Rightarrow \) effect of overlap capacitor for n & p devices to first order cancel (matching n & p width and \( \Delta L \)
Switch Charge Injection

Complementary Switch

Fast Clock

- Offset cancelled for equal device width
- Input voltage dependant error worse!

\[ \Omega_{\text{b-a}} = W_e C_{\text{ox}} L_a (V_H - V_i - V'_{\text{th-a}}) \]
\[ \Omega_{\text{b-p}} = W_p C_{\text{ox}} L_p (V_i - V_L - V'_{\text{th-p}}) \]
\[ \Delta V = \frac{1}{2} \left( \frac{\Omega_{\text{b-p}}}{C_i} - \frac{\Omega_{\text{b-a}}}{C_i} \right) \]

\[ V_v = V_i (1 + \varepsilon) + V'_{\text{ox}} \]
\[ \varepsilon = \frac{1}{2} \frac{W_e C_{\text{ox}} L_a + W_p C_{\text{ox}} L_p}{C_i} \]

- In fast clock case
- Offset cancelled for equal device width
- Input voltage dependant error worse!

Switch Charge Injection

Dummy Switch

- Dummy switch same L as main switch but half W
- Main device clock goes low, dummy device goes high \( \Rightarrow \) dummy switch acquires same amount of channel charge main switch needs to lose
- Effective only if exactly half of the charge transferred to M2 and requires good matching between clock fall/rise
Switch Charge Injection
Bottom Plate Sampling

- Switches M2 opened slightly earlier compared to M1
  ⇒ Injected charge by the opening of M2 is constant & eliminated when used differentially
- Since $C_s$ bottom plate open when M1 opened ⇒ no charge injected on $C_s$

Flip-Around Track & Hold

• Concept based on bottom-plate sampling
Flip-Around T/H-Basic Operation

**φ₁ → high**

Flip-Around T/H-Basic Operation

**φ₂ → high**
Flip-Around T/H - Timing

S1 opens earlier than S1A
"Bottom Plate Sampling"

Charge Injection

- At the instant of sampling, some of the charge stored in sampling switch S1 is dumped onto C
- With "Bottom Plate Sampling", charge injection comes only from S1 and is to first-order independent of $v_{IN}$
  - Only a dc offset is added This dc offset can be removed with a differential architecture
Flip-Around T/H

- S1 is an n-channel MOSFET
- Since it always switches the same voltage, its on-resistance, $R_{S1}$, is signal-independent (to first order)
- Choosing $R_{S1} >> R_{S1A}$ minimizes the non-linear component of $R = R_{S1A} + R_{S1}$
  - S1A is a wide (much lower resistance than S1) & constant $V_{GS}$ switch
  - In practice size of S1A is limited by the (nonlinear) S/D capacitance that also adds distortion
  - If S1A’s resistance is negligible $\rightarrow$ delay depends only on S1 resistance
  - S1 resistance is independent of $V_{IN}$ $\rightarrow$ delay is independent of $V_{IN}$
Differential Flip-Around T/H

Offset voltage associated with charge injection of S11 & S12 cancelled by differential nature of the circuit


Gain = 1
Feedback factor = 1
\[ \Delta V_{\text{in,cm}} = V_{\text{out,cm}} + V_{\text{sig,cm}} \]

Amplifier needs to have large input common-mode compliance
Differential Flip-Around T/H
Choice of Sampling Switch Size

- THD simulated w/o sampling switch boosted clock → -45dB
- THD simulated with sampling switch boosted clock (see figure)

Ref: K. Vleugel et al., "A 2.5-V Sigma–Delta Modulator for Broadband Communications Applications"
IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 36, NO. 12, DECEMBER 2001, pp. 1887

Input Common-Mode Cancellation

Ref: R. Yen et al., "A MOS Switched-Capacitor Instrumentation Amplifier,"
IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-17, NO. 6, DECEMBER 1982, 1008
Input Common-Mode Cancellation

Track mode (ϕ high)
\[ V_{C1} = V_{I1}, \quad V_{C2} = V_{I2} \]
\[ V_{o1} = V_{o2} = 0 \]

Hold mode (ϕ low)
\[ V_{o1} + V_{o2} = 0 \]
\[ V_{o1} - V_{o2} = -(V_{I1} - V_{I2})(C_1/(C_1 + C_3)) \]

→ Input common-mode level removed

Differential T/H Combined with Gain Stage

Employs the previously discussed technique to eliminate the problem associated with high common-mode voltage excursion at the input of the opamp

Differential T/H Combined with Gain Stage

- Gain = 4C/C = 4
- Feedback factor = 1/(1+G) = 0.2
- Input voltage common-mode level removed
- Amplifier offset not removed

Differential T/H Including Offset Cancellation

- Operation during offset cancellation phase shown
- Auxiliary inputs added with \( A_{\text{main}}/A_{\text{aux}} = 10 \)


\[ V_{\text{out}} = g_m r_0 V_{\text{in}} + g_m r_0 V_{\text{in}} \]

• During offset cancellation phase AZ and S1 closed → main amplifier offset amplified by $g_{m1}/g_{m2}$ & stored on $C_{AZ}$
• Auxiliary amp chosen to have lower gain so that:
  - Aux. amp offset & charge injection associated with opening of switch AZ → reduced by $A_{aux}/A_{main}=1/10$
  - Minimize power dissipation
• Requires an extra auto-zero clock phase

Differential T/H Including Offset Cancellation Phase

\[ (V_{INAZ^+} - V_{INAZ^-}) = -g_{m1}/g_{m2} V_{offset} \]
What is ESD?

- Electrostatic discharge
- Example: Charge built up on human body while walking on carpet...
- Charged objects near or touching IC pins can discharge through on-chip devices
- Without dedicated protection circuitry, ESD events could be destructive

Model and Protection Circuit

![Diagram](http://www.ce-mag.com/archive/03/ARG/dunnihoo.html)

![Diagram](http://www.idt.com/docs/AN_123.pdf)
Equivalent Circuit

- Nonlinear capacitance causes distortion
- Distortion increases with frequency
  - Today's converters: High frequency, low distortion!


ESD Circuit Distortion

\[ C(V_{in}) = 2 \ldots 4 \text{pF} \text{ for } V_{in} = 2 \ldots 0 \text{V} \]
ESD Circuit Distortion

- Analysis:
  - Volterra Series
  - Or SPICE simulations

- Example:

\[
\begin{align*}
\text{R} & = 25\, \Omega \\
\text{C}_{j} & = 1\, \text{pF} \\
\text{C}_{L} & = 5\, \text{pF} \\
\text{V}_{\text{peak}} & = 0.5\, \text{V}
\end{align*}
\]
ESD Circuit Distortion

- Distortion from ESD circuits approaches state of-the-art ADC performance!
- If you are working on a new, record breaking ADC, better think about ESD now...
- Solutions still pre-mature
- Lots of company intellectual property! (IP)

ADC Architectures

- Slope Converters
- Successive approximation
- Flash
- Folding
- Time-interleaved / parallel converter
- Residue type ADCs
  - Two-step
  - Pipeline
  - Algorithmic
  - ...
- Oversampled ADCs
**Single Slope ADC**

- Low complexity
- Hard to generate precise ramp
- Better: Dual Slope, Multi-Slope

**Dual Slope ADC**

- Integrate $V_{in}$ for fixed time, de-integrate with $V_{ref}$ applied $\rightarrow T_{De-Int} \sim \frac{V_{in}}{V_{ref}}$
-Insensitive to most linear error sources

http://www.maxim-ic.com/appnotes.cfm/appnote_number/1041
Successive Approximation ADC

- Binary search over DAC output

Successive Approximation ADC

Example: 6-bit ADC & $V_{in} = \frac{5}{8}V_{REF}$

- High accuracy achievable (16+ Bits)
- Moderate speed proportional to B (MHz range)
Flash Converter

- B-bit flash ADC:
  - DAC generates all possible $2^B - 1$ levels
  - $2^B-1$ comparators compare $V_{IN}$ to DAC outputs
  - Comparator output:
    - If $V_{DAC} < V_{IN}$ → 0
    - If $V_{DAC} > V_{IN}$ → 1
  - Comparator outputs form thermometer code
  - Encoder converts thermometer to binary code

Flash ADC Converter
Example: 3-bit Conversion

Encoder

Time

V_IN

V_REF

V_IN

V_REF

f_s

2^B-1 → B

Encoder

B-bits

0

1

0

1

1

1

1

1

0
Flash Converter

- Very fast: only 1 clock cycle per conversion
  - Half cycle → VIN & VDAC comparison
  - Half cycle → 2^B-1 to B encoding
- High complexity: 2^B-1 comparators
- High capacitance @ input node

Folding Converter

- Significantly fewer comparators than flash
- Fast
- Nonidealities in folder limit resolution to ~10-bits
Time Interleaved Converter

- Extremely fast:
  Limited by speed of S/H

- Accuracy limited by mismatch in individual ADCs (timing, offset, gain, …)

Residue Type ADC

- Quantization error output ("residuum") enables cascading for higher resolution
- Great flexibility for stages: flash, oversampling ADC, …
- Optional S/H enables parallelism (pipelining)
- Fast: one clock per conversion (with S/H), latency
Pipelined ADC

- Approaches speed of flash, but much lower complexity
- One clock per conversion, but K clocks latency
- Efficient digital calibration possible
- Versatile: from 16Bits / 1MS/s to 14Bits / 100MS/s

Algorithmic ADC

- Essentially same as pipeline, but a single stage is used for all partial conversions
- K clocks per conversion
Oversampled ADC

- Hard to comprehend … “easy” to build
- Input is oversampled (M times faster than output rate)
- Reduces Anti-Aliasing filter requirements and capacitor size
- Accuracy independent of component matching
- Very high resolution achievable (> 20 Bits)

\[ H(z) \]

Digital
Decimation
Filter
DAC

Vin

Throughput Rate Comparison

<table>
<thead>
<tr>
<th>Resolution [Bit]</th>
<th>Clock Cycles per Conversion</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>(10^0)</td>
</tr>
<tr>
<td>2</td>
<td>(10^1)</td>
</tr>
<tr>
<td>3</td>
<td>(10^2)</td>
</tr>
<tr>
<td>4</td>
<td>(10^3)</td>
</tr>
<tr>
<td>5</td>
<td>(10^4)</td>
</tr>
<tr>
<td>6</td>
<td>(10^5)</td>
</tr>
</tbody>
</table>

- Flash, Pipeline-1 to 2
- Successive Approximation
- Second Order 1-Bit
- Oversampled ~2(B-0.4B+1)
- Serial ~2B
Speed-Resolution Map

[www.v-corp.com]