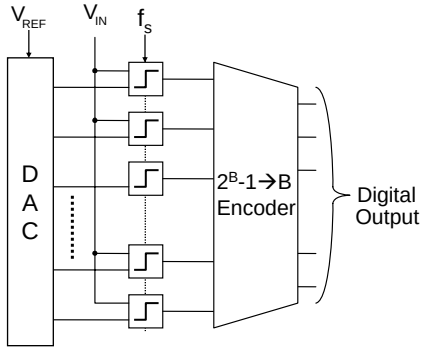
EE247
Lecture 20

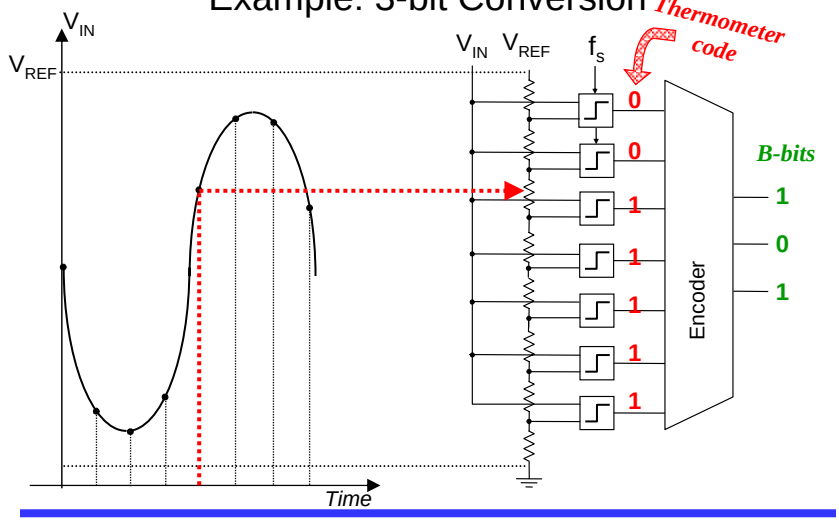
- ADC Converters
  - ADC architectures (continued)
  - Comparator architectures
    - Latched comparators
    - Latched comparators incorporating preamplifier
    - Sample-data comparators
      - Offset cancellation
  - Comparator architecture examples
  - Flash ADC sources of error
    - Sparkle code
    - Meta-stability

Flash Converter

- B-bit flash ADC:
  - DAC generates all possible 2^B -1 levels
  - 2^B-1 comparators compare V_{IN} to DAC outputs
  - Comparator output:
    - If $V_{DAC} < V_{IN} \rightarrow 0$
    - If $V_{DAC} > V_{IN} \rightarrow 1$
  - Comparator outputs form thermometer code
  - Encoder converts thermometer to binary code

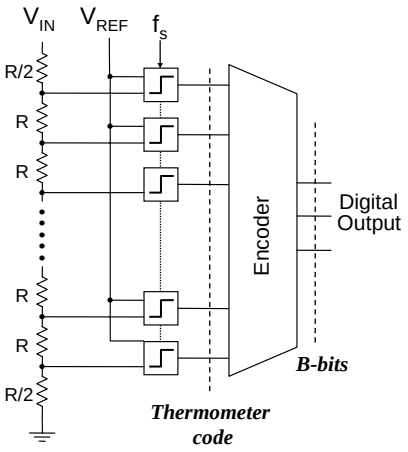


Flash ADC Converter
Example: 3-bit Conversion

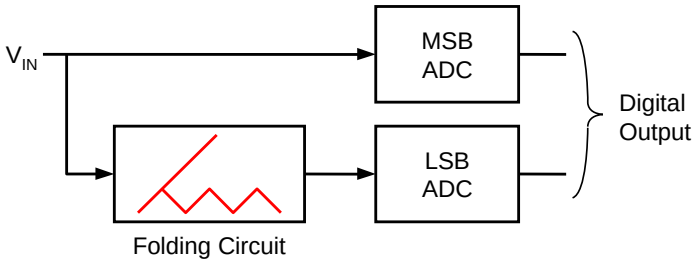


Flash Converter

- Very fast: only 1 clock cycle per conversion
  - Half cycle→ VIN & VDAC comparison
  - Half cycle→ 2^B-1 to B encoding
- High complexity: 2^B-1 comparators
- High capacitance @ input node

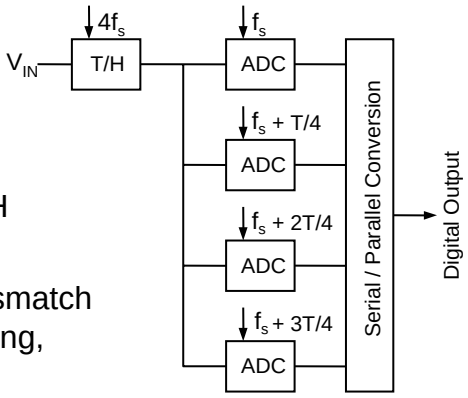


Folding Converter



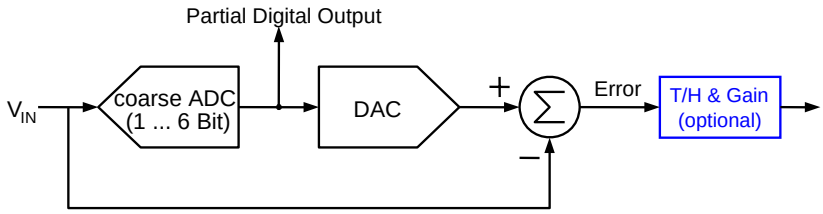
- Significantly fewer comparators than flash
- Fast
- Nonidealities in folder limit resolution to ~10-bits

Time Interleaved Converter



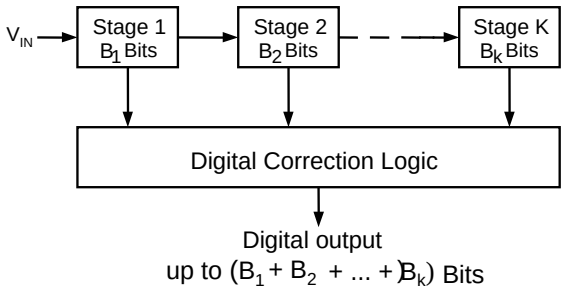
- Extremely fast:
  Limited by speed of T/H
- Accuracy limited by mismatch in individual ADCs (timing, offset, gain, …)

Residue Type ADC



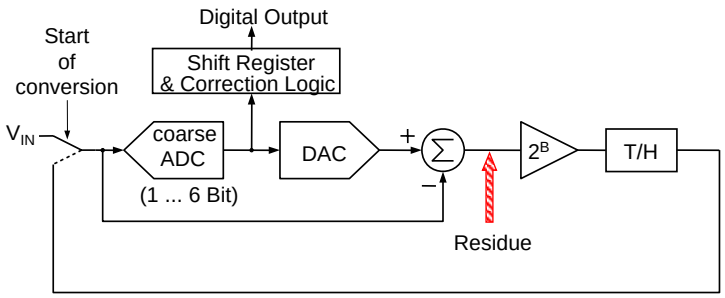
- Quantization error output ("residuum") enables cascading for higher resolution
- Great flexibility for stages: flash, oversampling ADC, …
- Optional T/H enables parallelism (pipelining)
- Fast: one clock per conversion (with T/H), latency

Pipelined ADC



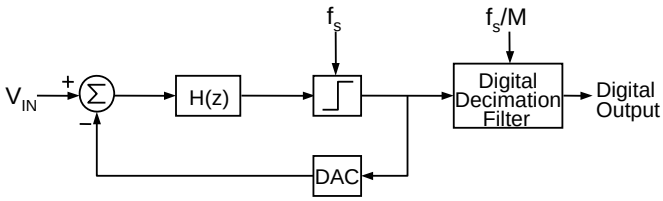
- Approaches speed of flash, but much lower complexity
- One clock per conversion, but K clocks latency
- Efficient digital calibration possible
- Versatile: from 16Bits / 1MS/s to 14Bits / 100MS/s

Algorithmic ADC



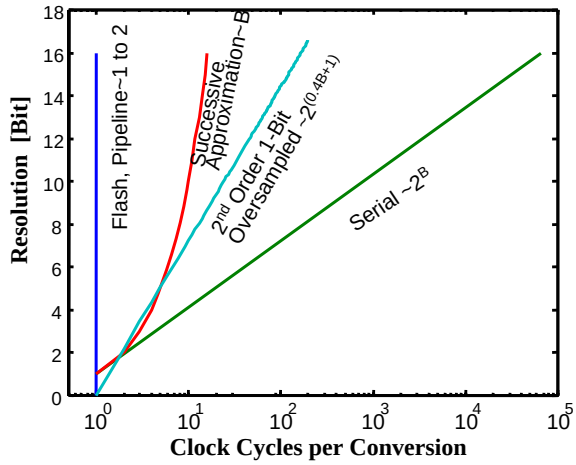
- Essentially same as pipeline, but a single stage is used for all partial conversions
- K clocks per conversion

Oversampled ADC

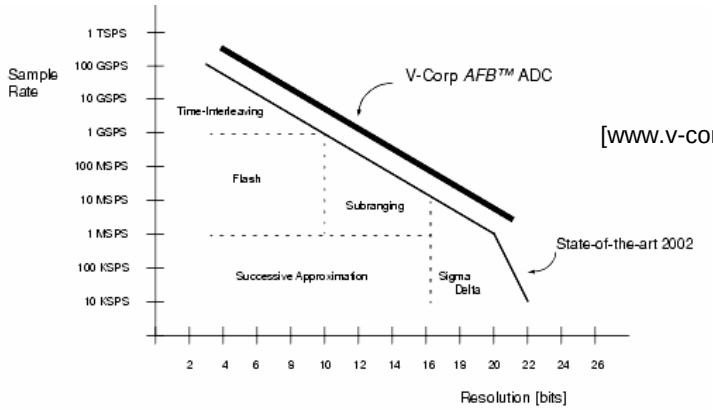


- Hard to comprehend … “easy” to build
- Input is oversampled (M times faster than output rate)
- Reduces Anti-Aliasing filter requirements and capacitor size
- Accuracy independent of component matching
- Very high resolution achievable (> 20 Bits)

Throughput Rate Comparison



Speed-Resolution Map



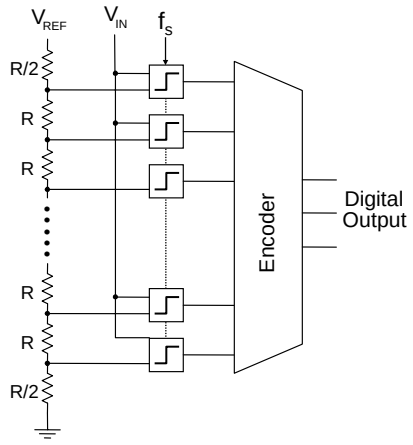
[www.v-corp.com]

High-Speed A/D Converters

- Flash Converter
  - Comparator design considerations
  - Binary Encoder
- Interpolation
- Folding
- Pipelined ADCs

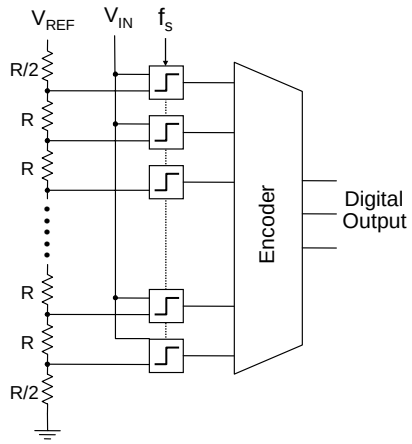
Flash Converter

- Very fast: only 1 clock cycle per conversion
- High complexity: 2^B-1 comparators
- High input capacitance



Flash Converter
Example: 8-bits ADC

- 8-bits→ 255 comparators
- V_{REF}=1V → 1LSB=4mV
- DNL<1/2LSB → Comparator input referred offset < 2mV
- 2mV =6σ_{offset}
  → σ_{offset} < 0.33mV



Flash ADC Converter
Example: 8-bits ADC (continued)

→ $1\sigma_{Offset} < 0.33mV$

- Let us assume in the technology used:
  - Voffset-per-unit-sqrt(WxL)=5mV

$$V_{0\,ffset} = \frac{5mV}{\sqrt{W \times L}} = 0.33mV \quad \rightarrow W \times L = 230\mu^2$$

$$\text{Assuming: } C_{ox} = 5\,fF/\mu^2 \quad \rightarrow C_{GS} = \frac{2}{3} C_{ox} W \times L = 765\,fF$$

$$\rightarrow \text{Total input capacitance: } 255 \times 0.765 = 195\,pF\,!$$

  - Issues:
    - Si area quite large
    - Large input capacitance
    - Since depending on input voltage different number of comparator input transistors would be on/off- input capacitance varies as input varies

    → Nonlinear input capacitance could give rise to signal distortion

Ref: M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE Journal of Solid-State Circuits,* vol. 24, pp. 1433 - 1439, October 1989.

Flash ADC Converter
Example (continued)

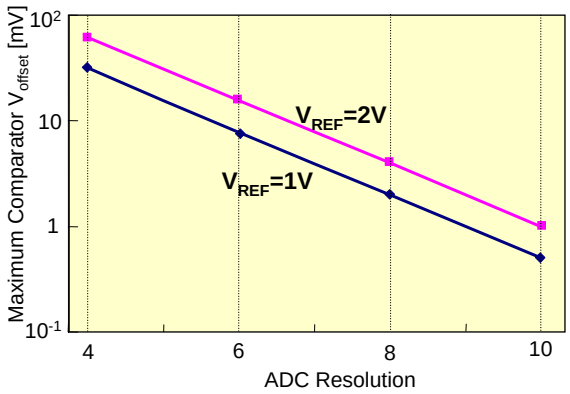
Trade-offs:

- Allowing larger DNL of 1LSB instead of 0.5LSB:
  - Increases the maximum allowable input-referred offset voltage by a factor of 2
  - Decreases the required device WxL by a factor of 4
  - Reduces the input device area by a factor of 4
  - Reduces the input capacitance by a factor of 4!
- Reducing the ADC resolution by 1-bit
  - Increases the maximum allowable input-referred offset voltage by a factor of 2
  - Decreases the required device WxL by a factor of 4
  - Reduces the input device area by a factor of 4
  - Reduce the input capacitance by a factor of 4

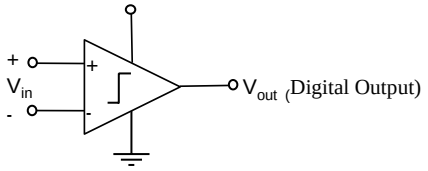
Flash Converter
Comparator Maximum Offset versus ADC Resolution

Assumption:
DNL=0.5LSB

Note:
Depending on min acceptable yield, numbers associated with 2σ to 7σ offset voltage



Voltage Comparators



Function: compare the instantaneous value of two analog signals

Important features:

- Maximum clock rate f_s → settling time, slew rate, small signal bandwidth
- Resolution→ gain, offset
- Overdrive recovery
- Input capacitance (and linearity of input capacitance!)
- Power dissipation
- Common-mode rejection
- Kickback noise
- …

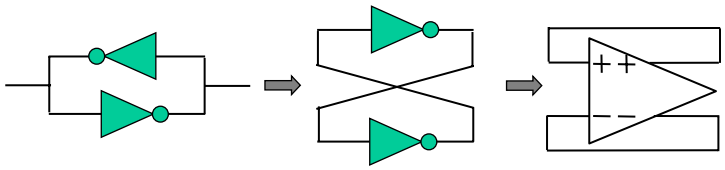
Voltage Comparator Architectures

Comparator architectures

- High gain amplifier with differential analog input & single-ended large swing output
  - Output swing compatible with driving digital logic circuits
  - Open-loop amplification→ no frequency compensation required
  - Precise gain not required
- Latched comparators; in response to a strobe, input stage disabled & digital output stored in a latch till next strobe
  - Two options for implementation :
    - Latch-only comparator
    - Low-gain amplifier + a high-sensitivity latch
- Sample-data comparators
  - T/H input
  - Offset cancellation

CMOS Latched Comparators

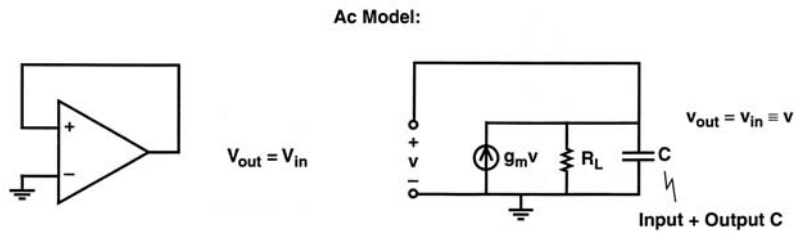
Comparator amplification need not be linear
→can use a latch → regeneration



→ Amplification + positive feedback

CMOS Latched Comparators

Latch can be modeled as a single-pole amp + positive feedback



CMOS Latched Comparator Delay

$$g_m V = \frac{V}{R_L} + C\frac{dV}{dt}$$

$$\frac{g_m}{C}\left(1 - \frac{1}{g_m R_L}\right)V = \frac{dV}{dt}$$

$$\frac{g_m}{C}\left(1 - \frac{1}{g_m R_L}\right)\int_{t1}^{t2} dt = \int_{V1}^{V2} \frac{1}{V} dV$$

Latch Delay:

$$\tau_D = t_2 - t_1 = \frac{C}{g_m}\left(\frac{1}{1 - \frac{1}{g_m R_L}}\right)\ln\left(\frac{V_2}{V_1}\right)$$

For $g_m R_L >> 1$

$$\boxed{\tau_D \approx \frac{C}{g_m}\ln\left(\frac{V_2}{V_1}\right)}$$

Latch-Only Comparator

- Problem with latch-only comparator topology:
  - High input-referred offset voltage (as high as 100mV!)
    - Solution:
      - Use preamplifier to amplify the signal and reduce overall input-referred offset

Comparator Preamplifier Gain-Speed Tradeoffs

- Amplifier maximum Gain-Bandwidth product for a given technology, typically a function of maximum device f_t

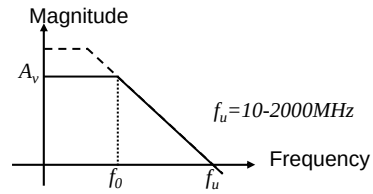
f_u =unity gain frequency, f_0 $= -3dB$ frequency & τ_0 $=$ settling time

$$f_0 = \frac{f_u}{A_{preamp}} =$$

For example:

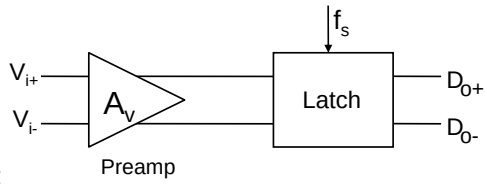
$$f_0 = \frac{f_u}{A_{preamp}} = \frac{1GHz}{10} = 100MHz$$

$$\tau_0 = \frac{1}{2\pi f_0} = 1.6n\sec$$



→ Tradeoff:
- To reduce the effect of latch offset → high preamp gain desirable
- Fast comparator → low preamp gain

Pre-Amplifier Tradeoffs



- Example:
  - Latch offset 50 to 100mV
  - Preamp DC gain 10X
  - Preamp input-referred latch offset 5 to 10mV
  - Input-referred preamplifier offset 2 to 10mV
  - Overall input-referred offset 5.5 to 14mV

→ Overall input-referred noise reduced by ~7 to 9X → ~extra 3-bit resolution!

CMOS Latched Comparator Including Preamplifier Delay

Latch delay found previously:

$$\tau_D \approx \frac{C}{g_m} \ln\left(\frac{V_2}{V_1}\right)$$

Assuming gain of A_v for the preamplifier:

$$\boxed{\tau_D \approx \frac{C}{g_m} \ln\left(A_v \frac{V_0}{V_{in}}\right)}$$

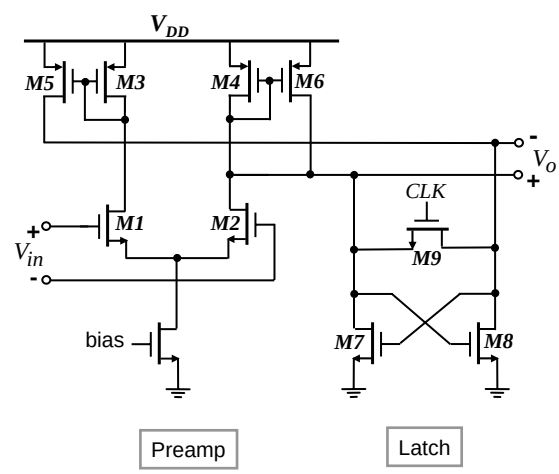
Latched Comparator Including Preamplifier Example

Preamplifier gain:

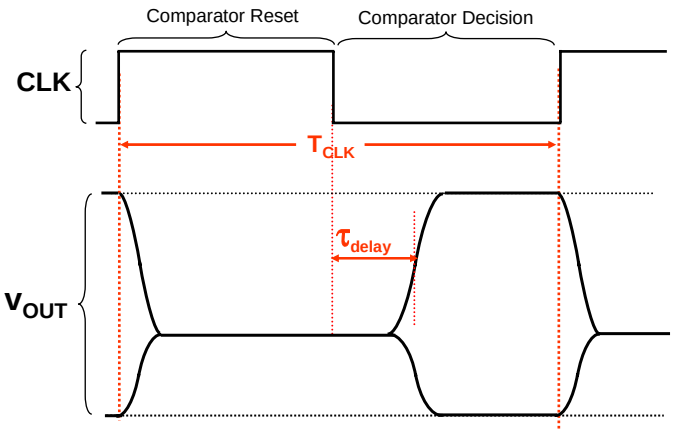
$$A_v = \frac{g_m^{M1}}{g_m^{M3}} = \frac{\left(V_{GS}^{M3} - V_{th}^{M3}\right)}{\left(V_{GS}^{M1} - V_{th}^{M1}\right)}$$

Comparator delay:

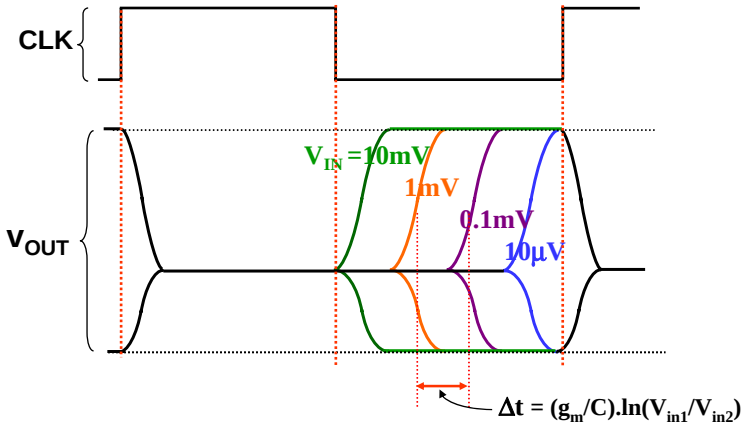
$$\tau_D \approx \frac{C}{g_m} \ln\left(A_v \frac{V_0}{Vin}\right)$$



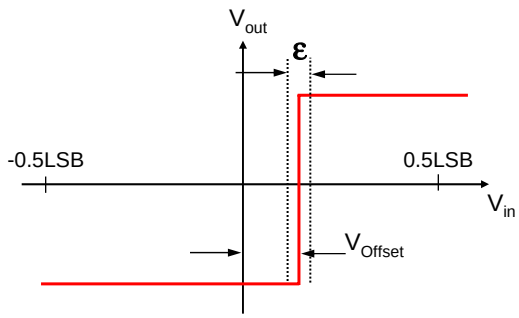
Comparator Dynamic Behavior



Comparator Resolution



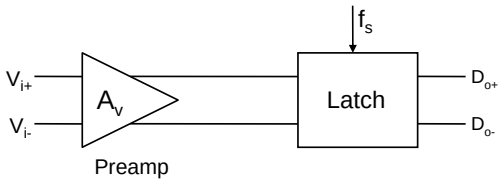
Comparator Voltage Transfer Function Non-Idealities



V_{Offset} → Comparator offset voltage

ε → Meta-Stable region (output ambiguous)

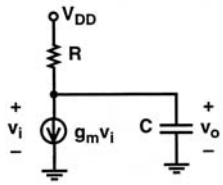
Latched Comparator

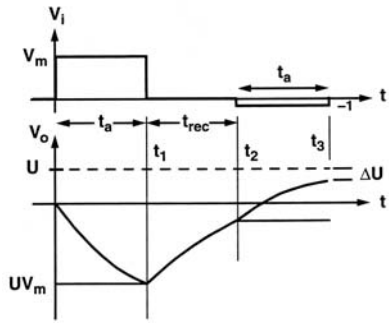


- Clock rate f_s
- Resolution
- Overload recovery
- Input capacitance (and linearity!)
- Power dissipation
- Common-mode rejection
- Kickback noise
- …

Comparators Overdrive Recovery

Linear model for a single-pole amplifier:





U→ amplification after time t_a

During reset amplifier settles exponentially to its zero input condition with τ_0=RC

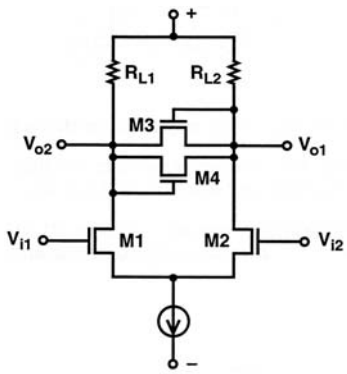
Assume Vm → maximum input normalized to 1/2lsb (=1)

Example: Worst case input/output waveforms

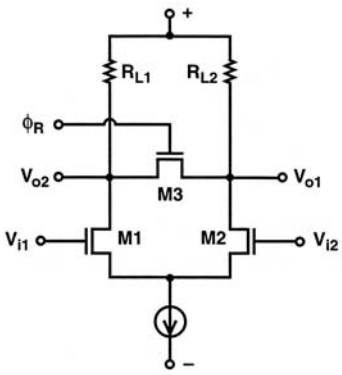
→ Limit output voltage swing by

1. Passive clamp
2. Active restore
3. Low gain/stage

Comparators Overdrive Recovery Limiting Output

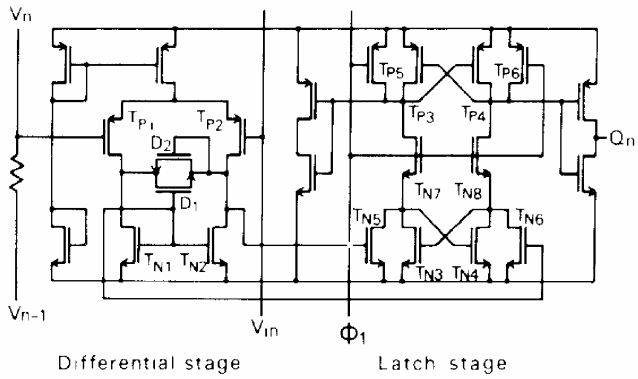


Clamp
Adds parasitic capacitance



Active Restore
After outputs are latched→ Activate ϕ_R & equalize output nodes

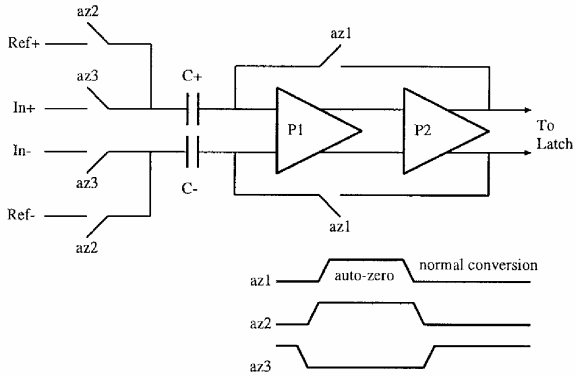
CMOS Comparator Example



•Flash ADC: 8bits, +-1/2LSB INL @ fs=15MHz (Vref=3.8V, LSB~15mV)
•No offset cancellation

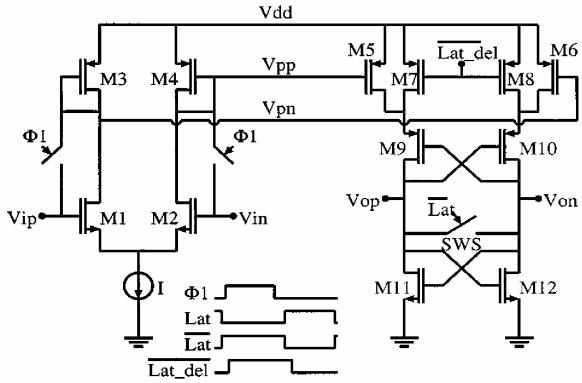
Ref: A. Yukawa, "A CMOS 8-Bit High-Speed A/D Converter IC," JSSC June 1985, pp. 775-9

Comparator with Auto-Zero



Ref: I. Mehr and L. Singer, "A 500-Msample/s, 6-Bit Nyquist-Rate ADC for Disk-Drive Read-Channel Applications," JSSC July 1999, pp. 912-20.

Auto-Zero Implementation



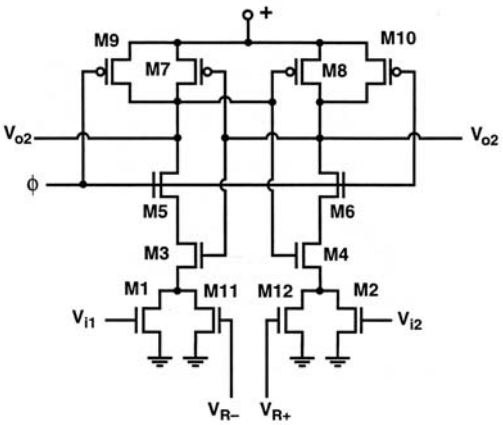
Ref:I. Mehr and L. Singer, "A 55-mW, 10-bit, 40-Msample/s Nyquist-Rate CMOS ADC," JSSC March 2000, pp. 318-25

Comparator Example

- Variation on Yukawa latch used w/o preamp
- No dc power when ϕ high
- Good for low resolution ADCs
- M11 & M12 added to vary comparator threshold
- To 1st order, for W1=W2 & W11=W12

  $V_{th}^{latch} = W11/W1 \times V_R$

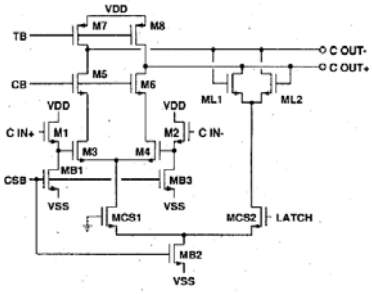
  where $V_R = V_{R+} - V_{R-}$

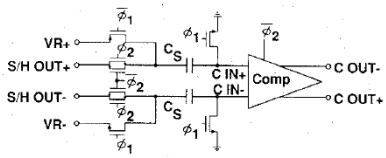


Ref: T. B. Cho and P. R. Gray, "A 10 b, 20 Msample/s, 35 mW pipeline A/D converter," *IEEE Journal of Solid-State Circuits,* vol. 30, pp. 166 - 172, March 1995

Comparator Example

- Used in a pipelined ADC with digital correction
  →no offset cancellation
- Note differential reference
- M7, M8 operate in triode region
- Preamp gain ~10
- Input buffers suppress kick-back

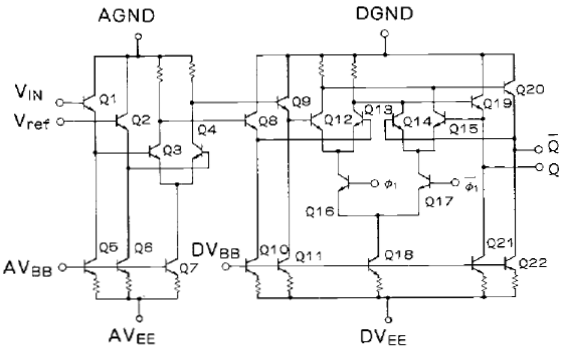




Ref: S. Lewis, et al., "A Pipelined 5-Msample/s 9-bit Analog-to-Digital Converter" IEEE JSSC ,NO. 6, Dec. 1987

Bipolar Comparator Example

- Used in 8bit 400Ms/s & 6bit 2Gb/s flash ADC
- Signal amplification during $\phi 1$ high, latch operates when $\phi 1$ low
- Input buffers suppress kick-back & input current
- Separate ground and supply buses for front-end preamp → kick-back noise reduction

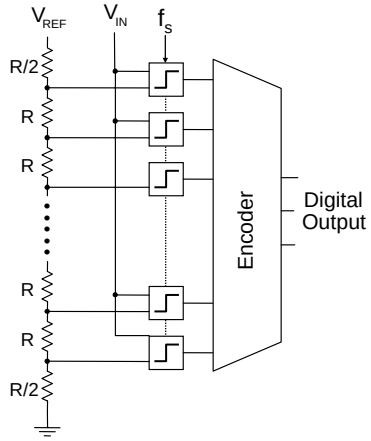


Preamp ***Latched Comparator***

Ref: Y. Akazawa, et al., "A 400MSPS 8b flash AD conversion LSI," *IEEE International Solid-State Circuits Conference,* vol. XXX, pp. 98 - 99, February 1987

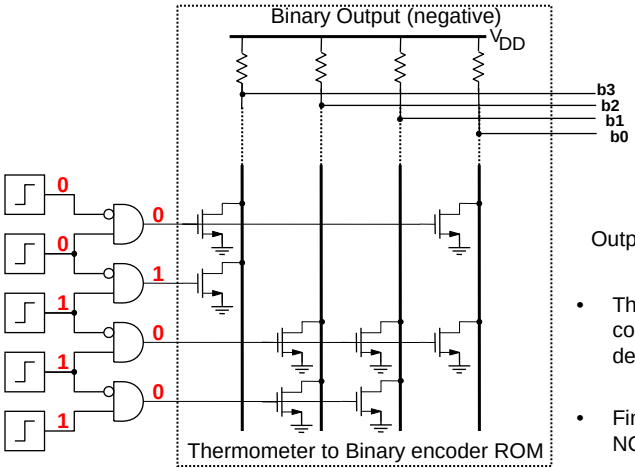
Ref: T. Wakimoto, et al, "Si bipolar 2GS/s 6b flash A/D conversion LSI," *IEEE International Solid-State Circuits Conference,* vol. XXXI, pp. 232 - 233, February 1988

Flash Converter Sources of Error



- Comparator input:
  - Offset
  - Nonlinear input capacitance
  - Kickback noise (disturbs reference)
  - Signal dependent sampling time
- Comparator output:
  - Sparkle codes (… 111101000 …)
  - Metastability

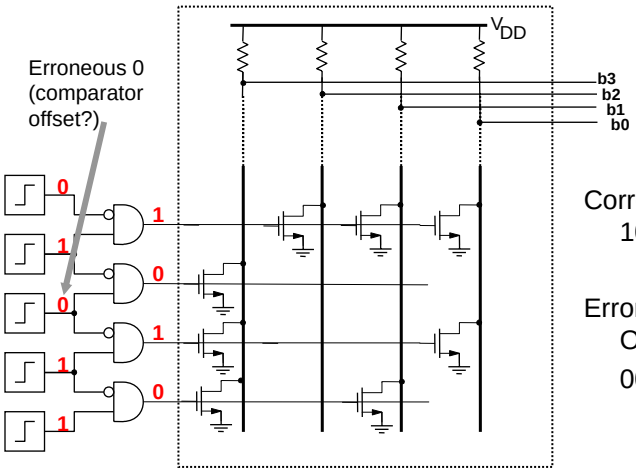
Typical Flash Output Encoder



	b3	b2	b1	b0
Output→	0	1	1	1

- Thermometer code → 1-of-n decoding
- Final encoding → NOR ROM

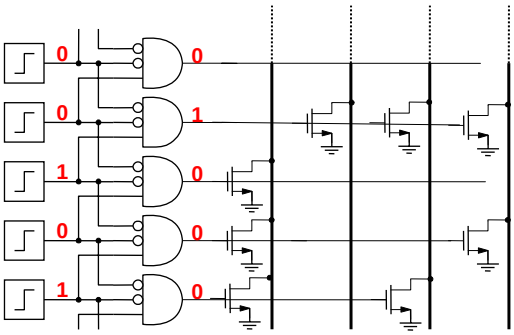
Sparkle Codes



Correct Output:
1000

Erroneous
Output:
0000

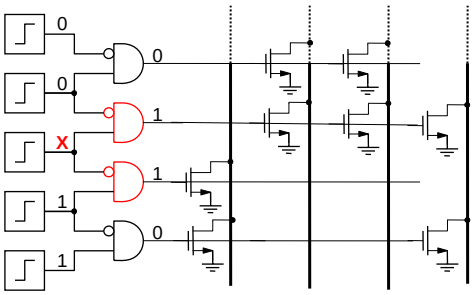
Sparkle Tolerant Encoder



Protects against a *single* sparkle.

Ref: C. Mangelsdorf et al, "A 400-MHz Flash Converter with Error Correction," JSSC February 1990, pp. 997-1002

Meta-Stability



Different gates interpret metastable output X differently

Correct output: 1000

Erroneous output: 0000

Solutions:
- –Latches (high power)
- –Gray encoding

Ref: C. Portmann and T. Meng, "Power-Efficient Metastability Error Reduction in CMOS Flash A/D Converters," JSSC August 1996, pp. 1132-40

Gray Encoding

Thermometer Code							Gray			Binary		
T_1	T_2	T_3	T_4	T_5	T_6	T_7	G_3	G_2	G_1	B_3	B_2	B_1
0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	1	0	0	1
1	1	0	0	0	0	0	0	1	1	0	1	0
1	1	1	0	0	0	0	0	1	0	0	1	1
1	1	1	1	0	0	0	1	1	0	1	0	0
1	1	1	1	1	0	0	1	1	1	1	0	1
1	1	1	1	1	1	0	1	0	1	1	1	0
1	1	1	1	1	1	1	1	0	0	1	1	1

$$G_1 = T_1\overline{T_3} + T_5\overline{T_7}$$

$$G_2 = T_2\overline{T_6}$$

$$G_3 = T_4$$

- Each T_i affects only one G_i
  → Avoids disagreement of interpretation by multiple gates
- Protects also against sparkles
- Follow Gray encoder by (latch and) binary encoder