EECS 247
Lecture 7

• Summary last lecture
• Automatic on-chip filter tuning (continued from last lecture)
  • Continuous tuning
    – Reference integrator locked to a reference frequency
    – DC tuning of resistive timing element
  • Periodic digitally assisted tuning
    – Systems where filter is followed by ADC & DSP, existing hardware
      can be used to periodically update filter freq. response
• Continuous-time filters
  – Bandpass filters
    • Example: Gm-C BP filter using simple diff. pair
    – Linearity & noise issues
  – Various Gm-C Filter implementations
  – Comparison of continuous-time filter topologies

Summary last lecture

• Continuous-time filters
  – Opamp MOSFET-C filters
  – Opamp MOSFET-RC filters
  – Gm-C filters
• Frequency tuning for continuous-time filters
  – Trimming via fuses
  – Automatic on-chip filter tuning
    • Continuous tuning
      – Utilizing VCF built with replica integrators
      – Use of VCO built with replica integrators
Master-Slave Frequency Tuning
Reference Integrator Locked to Reference Frequency

- Replica of main filter integrator e.g. Gm-C building block used
- Utilizes the fact that a DC voltage source connected to the input of the Gm cell generates a constant current proportional to the transconductance and the voltage reference

\[ I = Gm \cdot V_{ref} \]

Reference Integrator Locked to Reference Frequency

- Consider the following sequence:
  - Integrating capacitor is fully discharged @ \( t=0 \)
  - At \( t=0 \) the integrator input is connected to the output of the Gm cell then:

\[ V_{C1} = \frac{Gm \cdot V_{ref} \cdot T}{C1} \]
Reference Integrator Locked to Reference Frequency

Since at the end if the period $T$:

$$V_{C1} = Gm \times V_{ref} \times T / C_1$$

If $V_{C1}$ is forced to be equal to $V_{ref}$ then:

$$\frac{C}{Gm} = T = \frac{N}{f_{clk}}$$

How do we manage to force $V_{C1}=V_{ref}$?

→ Use feedback!

Reference Integrator Locked to Reference Frequency

- Three clock phase operation
- To analyze → study one phase at a time

Reference Integrator Locked to Reference Frequency
P1 high $\rightarrow$ S1 closed

$\text{\textbullet \, C1 \rightarrow \text{discharged}}$
$\text{\textbullet \, C2 \rightarrow \text{retains its previous charge}}$

Reference Integrator Locked to Reference Frequency
P2 high $\rightarrow$ S2 closed

$\text{\textbullet \, C1 \rightarrow \text{charged with constant current: } I = G_m \times V_{\text{ref}}}$
$\text{\textbullet \, C2 \rightarrow \text{retains its previous charge}}$

$V_{C1} = G_m \times V_{\text{ref}} \times T_2 / C_1$
Reference Integrator Locked to Reference Frequency

P3 high $\rightarrow$ S3 closed

$C_1$ charge shares with $C_2$

Few cycles following startup $\rightarrow$ Feedback forces $C_1/G_m$ to assume:

$V_{C1} = V_{C2} = V_{ref}$

since: $V_{C1} = G_m V_{ref} \times T_2 / C_1$

then: $V_{ref} = G_m V_{ref} \times T_2 / C_1$

or: $C_1/G_m = T_2 = N/f_{clk}$

Summary

Reference Integrator Locked to Reference Frequency

- Integrator time constant locked to an accurate frequency
- Tuning signal used to adjust the time constant of the main filter integrators

Feedback forces $G_m$ to vary so that:

$\tau_{int} = C_1/G_m = N/f_{clk}$

or

$\omega_{int} = G_m / C_1 = f_{clk} / N$
Issues
Reference Integrator Locked to Reference Frequency

Problems to be aware of:

\[ \omega_0^{int} = \frac{G_m}{C_1} = \frac{f_{clk}}{N} \]

→ Tuning error due to master integrator DC offset

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What is DC offset?

Simple example:

For the differential pair shown here, any mismatch in input device characteristics would cause DC offset: \( V_o = 0 \) requires a non-zero input voltage

Offset could be modeled as a small DC voltage source at the input

Example: Differential Pair
**Gm-Cell Offset Induced Error**

- **Effect of Gm-cell DC offset:**

  \[ V_{C1} = V_{C2} = V_{ref} \]

  - Ideal: \[ V_{C1} = G_m \times V_{ref} \times T_2 / C_1 \]
  - With offset: \[ V_{C1} = G_m \times (V_{ref} - V_{os}) \times T_2 / C_1 \]

  or:

  \[ \frac{C_1}{G_m} = \frac{T_2}{1 - \frac{V_{os}}{V_{ref}}} \]

- **Example:**

  \[ \frac{C_1}{G_m} = T_2 \left( 1 - \frac{V_{os}}{V_{ref}} \right) \]

  for \[ \frac{V_{os}}{V_{ref}} = 1/10 \]

  10% error in tuning!
Issues
Gm-Cell Offset Induced Error

• Assume differential integrator

• Add a pair of auxiliary inputs to the input stage for offset cancellation purposes

Reference Integrator Locked to Reference Frequency
Offset Cancellation Incorporated

Gm-cell \( \rightarrow \) two sets of input pairs
Aux. input pair + \( C_{3a,b} \) \( \rightarrow \) Offset cancellation
Same clock timing
Reference Integrator Locked to Reference Frequency
P3 High (Update & Store offset)

Gm-cell $\rightarrow$ Unity gain configuration via aux. inputs
$C3a,b \rightarrow$ Store Gm-cell offset
$C1, C2 \rightarrow$ Charge sharing

Reference Integrator During Offset Cancellation Phase

Gm-cell $\rightarrow$ Unity gain configuration via aux. inputs, main input shorted
$\rightarrow V_{out} = V_{os}$

$C3a,b$ acquire charge equal to $V_{os} \rightarrow$ Store Gm-cell offset

*Note: This technique can be used in various other applications
Reference Integrator Locked to Reference Frequency

P1 High (Reset)

$V_{C3a,b} = -V_{os}$

- $+V_{ref}/2$
- $-V_{ref}/2$
- $V_{cm}$

Gm-cell $\rightarrow$ Reset,
$C1$ $\rightarrow$ Discharge
$C2$ $\rightarrow$ Hold Charge
$C3a,b$ $\rightarrow$ Hold Charge
$\rightarrow$ Offset stored on $C3a,b$ cancels gm-cell offset

Reference Integrator Locked to Reference Frequency

P2 High (Charge)

$V_{C3a,b} = -V_{os}$

- $+V_{ref}/2$
- $-V_{ref}/2$
- $V_{cm}$

Gm-cell $\rightarrow$ Charging $C1$
$C3a,b$ $\rightarrow$ Store Gm-cell offset
$C2$ $\rightarrow$ Hold charge
Summary
Reference Integrator Locked to Reference Frequency

Key point: Tuning error due to Gm-cell offset cancelled

\[ V_{cm} = \frac{V_{ref}}{2} - \frac{V_{ref}}{2} \]

Tuning error due to gm-cell offset voltage resolved

Advantage over previous schemes:

\[ f_{clk} \] can be chosen to be at much higher frequencies compared to filter bandwidth \((N > 1)\)

\[ \text{Feedback forces } Gm \text{ to vary so that:} \]

\[ \tau_{int} = \frac{C_1}{Gm} = \frac{N}{f_{clk}} \]

or

\[ \omega_0^{int} = \frac{Gm}{C_1} = \frac{f_{clk}}{N} \]
DC Tuning of Resistive Timing Element

R_{ext} used to lock G_{m} or on-chip R

Feedback forces $G_{m} = I / R_{ext}$

Issues with DC offset

Account for capacitor variations in the gm-C implementation by trimming


Digitally Assisted Frequency Tuning

Example: Wireless Receiver Baseband Filters

- Systems where filter is followed by ADC & DSP
  - Take advantage of existing digital signal processor to periodically update the filter critical frequency
  - Filter tuned only at the outset of each data transmission session (off-line tuning)
Example: Seventh Order Tunable Low-Pass OpAmp-RC Filter

Digitally Assisted Filter Tuning Concept

Tuning Cycle:
Connect the filter input to DC source.
DSP measures the DC power level.
Connect the filter input to AC source (freq. -> desired -3dB freq.)
DSP measures the AC signal power level.
If DC = 4\textsuperscript{th} AC
Then filter is tuned.
Else if DC > 4\textsuperscript{th} AC
Then widen the filter bandwidth & repeat.
Else narrow the filter bandwidth & repeat.
Practical Implementation of Frequency Tuning

AC Measurement

DC Measurement

Digital Signal Processor
DSP1616
40MHz

A/D
4bit
10MHz

Register

Practical Implementation of Frequency Tuning

AC Signal Generation

V_{out} = +\Delta

Clock = high

V_{out} = -\Delta

ClockB = high

AC Measurement

V_{out}

2\Delta

\Delta

\Delta
**Practical Implementation of Frequency Tuning**

\[ f(t) = \frac{\Delta}{\pi} \sin(\omega_0 t) \times \frac{1}{\sqrt{2}} \]

- Input signal chosen to be a square wave due to ease of generation
- Filter input signal comprises a sinusoidal waveform @ the fundamental frequency + its odd harmonics:

**Key Point**: The filter itself attenuates the unwanted odd harmonics \( \Rightarrow \) Inaccuracy incurred by the harmonics negligible

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**Simplified Frequency Tuning Flowchart**

1. **Start Tuning**
2. **DC Measure**
   - \([AD1] = \sum_{n=1}^{\infty} [AD1]^2\)
   - Output Settled? NO
   - [AD1] - [AD2] \(\geq\) err?
      - YES, Output Settled?
      - NO, \(\text{CONT} \leftarrow \text{CONT} \pm 1\)
3. **AC Measure**
   - \([AD2] = \sum_{m=1}^{2} [AD2]^2\)
   - Output Settled? YES
   - \(\text{CONT} \leftarrow \text{CONT} \pm 1\) NO
4. **Store CONT**

\[ \frac{n}{m} = \left( \frac{4}{\pi} \right)^2 \times \frac{|H(f = f_{\text{ref}})|^2}{2 \times |H(f = 0)|^2} \]
Offset Compensation

In cases where the filter DC offset cause significant error in tuning (i.e. high passband gain)
- Offset compensation needed:
  - DC measurement performed in two steps:

\[
\begin{align*}
\text{Vout1} &= A \ (\Delta + V_{os}) \\
\text{Vout2} &= A \ (-\Delta + V_{os}) \\
\end{align*}
\]

**Passband Gain**

- DSP extracts: Offset component \( \rightarrow \frac{1}{2}(\text{Vout1} + \text{Vout2}) = A \cdot V_{os} \)
- DC component \( \rightarrow \frac{1}{2}(\text{Vout1} - \text{Vout2}) = A \cdot \Delta \)

- DSP substracts \( V_{os} \) from all subsequent AC measurement

Filter Tuning Prototype Diagram
Measured Frequency Response

-9 dB
100 kHz

21 dB
618 kHz

1.3 MHz

3 dB/div.

Tuning bits varied from all 0's to all 1's

Automatically tuned response

Chip Photo
Measured Tuning Characteristics

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Tunable frequency range (nom. process)</td>
<td>370kHz to 1.1MHz</td>
</tr>
<tr>
<td>Variations due to process</td>
<td>±50%</td>
</tr>
<tr>
<td>I/Q bandwidth imbalance</td>
<td>0.1%</td>
</tr>
<tr>
<td>Tuning resolution (620kHz frequency range)</td>
<td></td>
</tr>
<tr>
<td>Measured</td>
<td>3.8%</td>
</tr>
<tr>
<td>Expected</td>
<td>2-5%</td>
</tr>
<tr>
<td>Tuning time</td>
<td></td>
</tr>
<tr>
<td>Coarse+Fine</td>
<td>max. 800μsec</td>
</tr>
<tr>
<td>Fine only</td>
<td>min. 50μsec</td>
</tr>
<tr>
<td>Memory space required for tuning routine</td>
<td>250 byte</td>
</tr>
</tbody>
</table>

Off-line Digitally Assisted Tuning

- **Advantages:**
  - No reference signal feedthrough since tuning does not take place during data transmission (off-line)
  - Minimal additional hardware
  - Small amount of programming

- **Disadvantages:**
  - If acute temperature change during data transmission, filter may slip out of tune!
    - Can add fine tuning cycles during dead periods of data transmission

Summary: Continuous-Time Filter Frequency Tuning

- **Trimming**
  - Expensive & does not account for temperature and supply etc… variations

- **Automatic frequency tuning**
  - Continuous tuning
    - Master VCF used in tuning loop
      - Tuning quite accurate
      - Issue $\rightarrow$ reference signal feedthrough to the filter output
    - Master VCO used in tuning loop
      - Design of reliable & stable VCO challenging
      - Issue $\rightarrow$ reference signal feedthrough
  - Single integrator in negative feedback loop forces time-constant to be a function of accurate clock frequency
    - More flexibility in choice of reference frequency $\rightarrow$ less feedthrough issues
  - DC locking of a replica of the integrator to an external resistor
    - DC offset issues & does not account for integrating capacitor variations
  - Periodic tuning
    - Requires digital capability + minimal additional hardware
    - Advantage of no reference signal feedthrough since tuning performed off-line

Bandpass Filters

- **Bandpass Filters:**
  - $Q < 5 \rightarrow$ Combination of lowpass & highpass
  - $Q > 5 \rightarrow$ Direct implementation
Direct Implementation
Narrow-Band Bandpass Filters

- Design based on lowpass prototype for narrow band filters
- Same lowpass tables used

\[ s \mapsto Q \times \frac{s - \Omega_L}{s - \Omega_C} \]

\[ \Omega_S = \frac{\Omega_{B2} - \Omega_{B1}}{\Omega_{S2} - \Omega_{S1}} \]

Lowpass to Bandpass Transformation

Lowpass to Bandpass Transformation Table

Lowpass filter structures & tables used to derive bandpass filters

\[ Q = Q_{\text{filter}} \]


<table>
<thead>
<tr>
<th>LP</th>
<th>BP</th>
<th>BP Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>( C' )</td>
<td>( C )</td>
<td>( C = QC' \times \frac{1}{R \omega_0} )</td>
</tr>
<tr>
<td>( L' )</td>
<td>( L )</td>
<td>( L = \frac{1}{QC'} \times \frac{R}{\omega_0} )</td>
</tr>
<tr>
<td>( L' )</td>
<td>( C )</td>
<td>( C = \frac{1}{QC'} \times \frac{1}{R \omega_0} )</td>
</tr>
</tbody>
</table>

\( C' \) & \( L' \) are normalized LP values

Lowpass to Bandpass Transformation

- Each capacitor replaced by parallel L & C
- Each inductor replaced by series L & C
Lowpass to Bandpass Transformation

\[ C_1 = Q C_1 \times \frac{1}{R_0 \omega_0} \]
\[ L_1 = \frac{1}{Q} C_1 \times \frac{R}{\omega_0} \]
\[ C_2 = \frac{1}{Q} L_2 \times \frac{1}{R_0 \omega_0} \]
\[ L_2 = Q L_2 \times \frac{R}{\omega_0} \]
\[ C_3 = Q C_3 \times \frac{1}{R_0 \omega_0} \]
\[ L_3 = \frac{1}{Q} C_3 \times \frac{R}{\omega_0} \]

Where:
- \( C_1', L_2', C_3' \rightarrow \) normalized lowpass values
- \( Q \rightarrow \) bandpass filter quality factor &
- \( \omega_0 \rightarrow \) filter center frequency

Signal Flowgraph

6th Order Bandpass Filter

Note each C & L in the original lowpass prototype \( \rightarrow \) replaced by a resonator
Substituting the bandpass \( L_1, C_1, \ldots \) by their normalized lowpass equivalent previous page
The resulting SFG is:
• Note the integrators have different time constants
  • Ratio of time constants for each resonator $\sim 1/Q^2$
    → typically, requires high component ratios
    → poor matching
  • Desirable to convert SFG so that all integrators have equal time constants for optimum matching.
    • Scale nodes to obtain equal integrator time constant

• Note: Three resonators
  • All integrator time-constants are equal
  • Let us try to build this bandpass filter using the simple Gm-C structure
Second Order Gm-C Filter
Using Simple Source-Couple Pair Gm-Cell

- Center frequency:
  \[ \omega_c = \frac{g_m^{M/2}}{2 \times C_{int}} \]
- Q function of:
  \[ Q = \frac{g_m^{M/2}}{s M f} \]

To use this structure it is easier to couple resonators through capacitive coupling

Signal Flowgraph
6th Order Bandpass Filter

Modified signal flowgraph to have equal coupling between resonators
- In most filter cases \( C_i = C_i' \)
- Example: For a butterworth lowpass filter \( C_i' = C_i = 1 \) & \( L_2' = 2 \)
- Assume desired overall bandpass filter \( Q = 10 \)
Sixth Order Bandpass Filter Signal Flowgraph

\[ V_{in} \rightarrow \frac{1}{Q} s \omega_0 \rightarrow \frac{1}{Q} s \omega_0 \rightarrow -s \omega_0 \rightarrow \frac{1}{Q} s \omega_0 \rightarrow \frac{1}{Q} s \omega_0 \rightarrow V_{out} \]

- Where for a Butterworth shape \( \gamma = \frac{1}{Q\sqrt{2}} \)
- Since \( Q = 10 \) then: \( \gamma = \frac{1}{14} \)

**Coupling paths (\( \gamma \)) between resonators can be implemented with extra differential input pairs**

**Or modify SFG as shown in next page:**
Sixth Order Bandpass Filter Signal Flowgraph

For narrow band filters (high Q) where frequencies within the passband are close to $\omega_0$, narrow-band approximation can be used:
The resulting SFG:

Bidirectional coupling paths, can easily be implemented with coupling capacitors

Sixth Order Gm-C Bandpass Filter
Utilizing Simple Source-Coupled Pair Gm-Cell

\[ \gamma = \frac{C_k}{2 \times C_{int} \times g} \]
\[ \gamma = \frac{1}{14} \]
\[ C_k = \frac{1}{7 \times C_{int} \times g} \]

Parasitic C at integrator output, if unaccounted for, will result in inaccuracy in $\gamma$
Sixth Order Gm-C Bandpass Filter
Frequency Response Simulation

Simplest Form of CMOS Gm-Cell
Nonidealities

- DC gain (integrator Q)
  \[ a = \frac{g_{M1,2} M_{1,2}}{g_{o} M_{1,2} + g_{load}} \]
  \[ a = \frac{2L}{\theta (V_{gs} - V_{th}) M_{1,2}} \]

- Where \( a \) denotes DC gain & \( \theta \) is related to channel length modulation by:
  \[ \lambda = \frac{\theta}{L} \]
- Seems no extra poles!
CMOS Gm-Cell High-Frequency Poles

- Distributed nature of gate capacitance & channel resistance results in infinite no. of high-frequency poles

\[ P_2^{\text{effective}} = \frac{I}{\sum_{i=2}^{\infty} P_i} \]

\[ P_2^{\text{effective}} = 2.5\omega_i M_{1.2} \]

\[ \omega_i M_{1.2} = \frac{g_m M_{1.2}}{C_{ox} WL} = \frac{3}{2} \frac{\mu (V_{gs} - V_{th}) M_{1.2}}{L^2} \]

- Distributed nature of gate capacitance & channel resistance results in an effective pole at 2.5 times input device cut-off frequency
CMOS Gm-Cell Quality Factor

\[ a = \frac{2L}{\theta (V_{gs} - V_{th})_{M1,2}} \]

\[ p_{\text{effective}} = \frac{15}{4} \frac{\mu (V_{gs} - V_{th})_{M1,2}}{L^2} \]

\[ Q_{\text{real}}^{\text{intg}} = \frac{1}{d - \omega_0 \sum_j L_j} \]

\[ Q_{\text{real}}^{\text{intg}} = \frac{1}{2L} \theta \frac{(V_{gs} - V_{th})_{M1,2}}{\omega_0 L} \cdot \frac{4 \omega_0 L^2}{\mu (V_{gs} - V_{th})_{M1,2}} \]

- Note that the phase lead associated with DC gain is inversely prop. to L
- The phase lag due to high-freq. poles directly prop. to L
  - For a given \( \omega_0 \), there exists an optimum \( L \) which cancel the lead/lag phase error resulting in high integrator \( Q \)

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CMOS Gm Cell Channel Length for Optimum Integrator Quality Factor

\[ L_{opt} = \left[ \frac{15}{4} \frac{\theta \mu (V_{gs} - V_{th})^2_{M1,2}}{\omega_0} \right]^{1/3} \]

- Optimum channel length computed based on process parameters