# EE247
# Lecture 7

- Summary last lecture
- Automatic on-chip filter tuning (continued from last lecture)
  - Continuous tuning
    - Reference integrator locked to a reference frequency
    - DC tuning of resistive timing element
  - Periodic digitally assisted tuning
    - Systems where filter is followed by ADC & DSP, existing hardware can be used to periodically update filter freq. response
- Continuous-time filters
  - Bandpass filters
    - Example: Gm-C BP filter using simple diff. pair
      - Linearity & noise issues
  - Various Gm-C Filter implementations
  - Comparison of continuous-time filter topologies


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# Summary last lecture

- Continuous-time filters
  - Opamp MOSFET-C filters
  - Opamp MOSFET-RC filters
  - Gm-C filters
- Frequency tuning for continuous-time filters
  - Trimming via fuses
  - Automatic on-chip filter tuning
    - Continuous tuning
      - Utilizing VCF built with replica integrators
      - Use of VCO built with replica integrators


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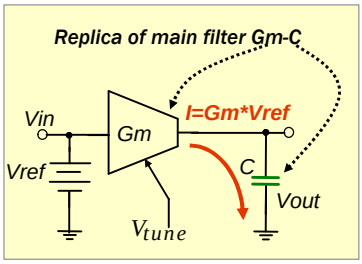
# Master-Slave Frequency Tuning
# Reference Integrator Locked to Reference Frequency




•Replica of main filter integrator e.g. Gm-C building block used

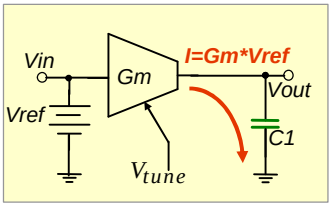
•Utilizes the fact that a DC voltage source connected to the input of the Gm cell generates a constant current proportional to the transconductance and the voltage reference

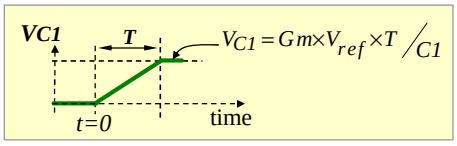
$$I = Gm.Vref$$



# Reference Integrator Locked to Reference Frequency

•Consider the following sequence:
- Integrating capacitor is fully discharged @ $t=0$
- At $t=0$ the integrator input is connected to the output of the Gm cell then:



## Reference Integrator Locked to Reference Frequency

Since at the end if the period T:

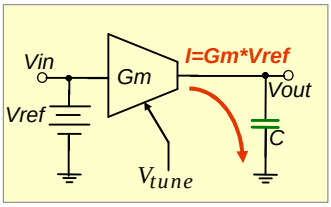
$$V_{C1} \approx Gm \times V_{ref} \times T \,/\, C1$$

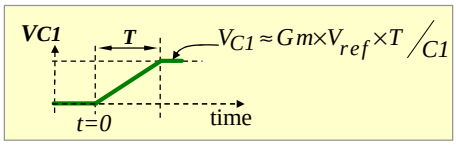
If *VC1* is forced to be equal to *Vref* then:

$$\frac{C}{Gm} = T = \frac{N}{f_{clk}}$$

How do we manage to force VC1=Vref?

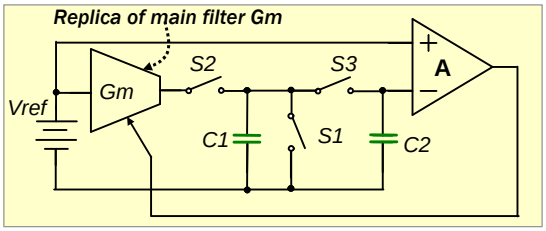
→ Use feedback!



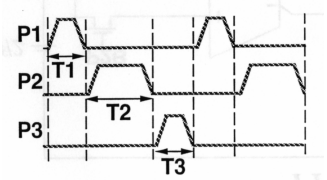






## Reference Integrator Locked to Reference Frequency

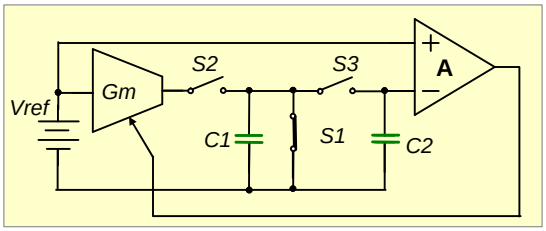


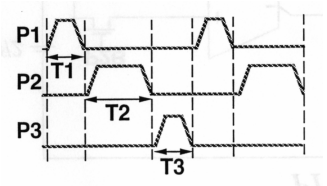

- Three clock phase operation
- To analyze → study one phase at a time




Ref: A. Durham, J. Hughes, and W. Redman- White, "Circuit Architectures for High Linearity Monolithic Continuous-Time Filtering," *IEEE Transactions on Circuits and Systems*, pp. 651-657, Sept. 1992.

## Reference Integrator Locked to Reference Frequency
## P1 high→ S1 closed

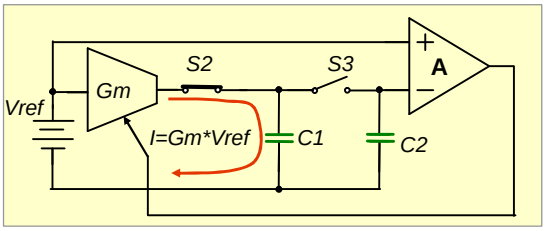


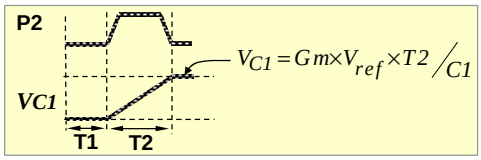

***C1*** → discharged
***C2*** → *retains its previous charge*



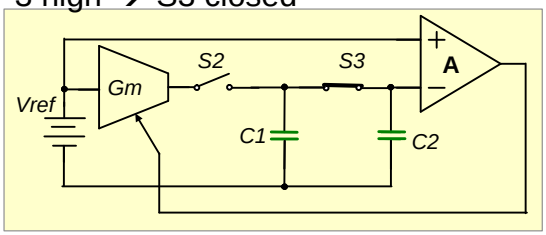
## Reference Integrator Locked to Reference Frequency
## P2 high → S2 closed

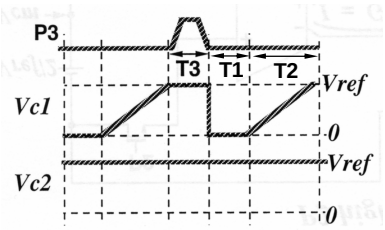



***C1*** → charged with constant current: I=Gm*Vref
***C2*** → *retains its previous charge*



## Reference Integrator Locked to Reference Frequency
## P3 high → S3 closed




*C1 charge shares with C2*
*Few cycles following startup*
*→ Feedback forces C1/Gm to assume:*

$$V_{C1} = V_{C2} = Vref$$

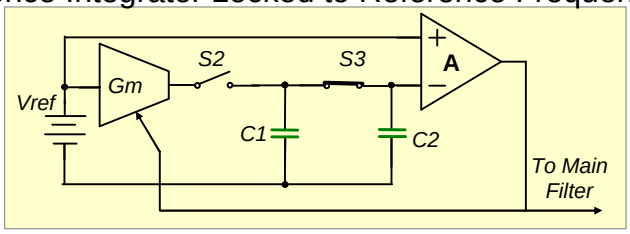
$$since: V_{C1} = Gm \times V_{ref} \times T2 / C1$$

$$then: V_{ref} = Gm \times V_{ref} \times T2 / C1$$

$$or: \quad C1/Gm = T2 = N / fclk$$



## Summary
## Reference Integrator Locked to Reference Frequency




- Integrator time constant locked to an accurate frequency
- Tuning signal used to adjust the time constant of the main filter integrators

*Feedback forces Gm to vary so that :*

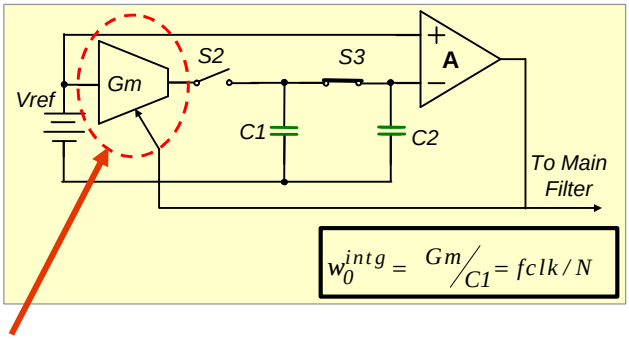
$$t_{intg} = C1/Gm = N / fclk$$

$$or$$

$$w_0^{intg} = Gm/C1 = fclk / N$$

# Issues
## Reference Integrator Locked to Reference Frequency

Problems to be aware of:




→ **Tuning error due to master integrator DC offset**



# Issues
## Reference Integrator Locked to Reference Frequency

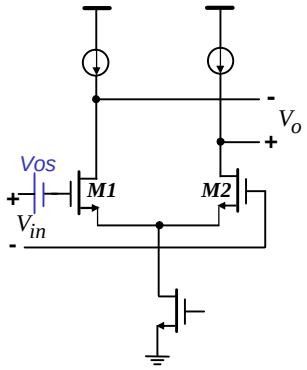
What is DC offset?

Simple example:

For the differential pair shown here, any mismatch in input device characteristics would cause DC offset:

→ ***Vo = 0*** requires a non-zero input voltage

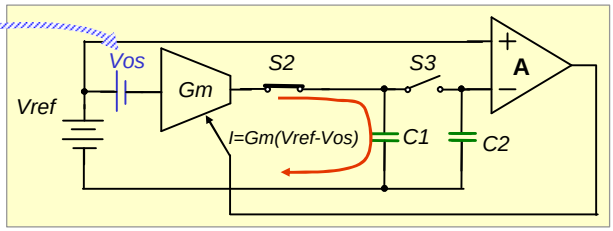
Offset could be modeled as a small DC voltage source at the input




**Example: Differential Pair**

# Gm-Cell Offset Induced Error

Voltage source representing DC offset




•Effect of Gm-cell DC offset:

$$V_{C1} = V_{C2} = Vref$$

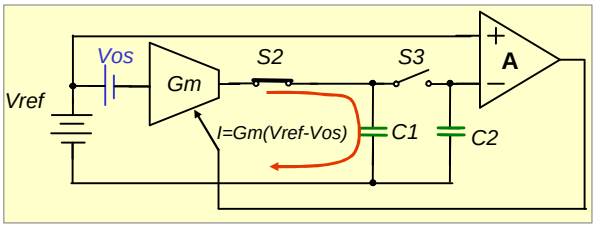
$$Ideal: V_{C1} = Gm \times V_{ref} \times T2 / C1$$

$$with\ offset: V_{C1} = Gm \times \left(V_{ref} - V_{os}\right) \times T2 / C1$$

$$or: \quad C1/Gm = T2\left(1 - \frac{V_{os}}{V_{ref}}\right)$$



# Gm-Cell Offset Induced Error




•Example:

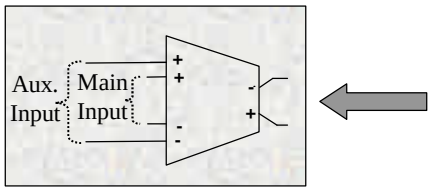
$$C1/Gm = T2\left(1 - \frac{V_{os}}{V_{ref}}\right)$$

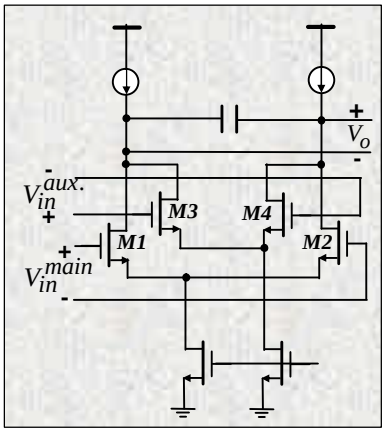
$$for\ \frac{V_{os}}{V_{ref}} = 1/10$$

$$10\%\ error\ in\ tuning!$$

# Issues
## Gm-Cell Offset Induced Error

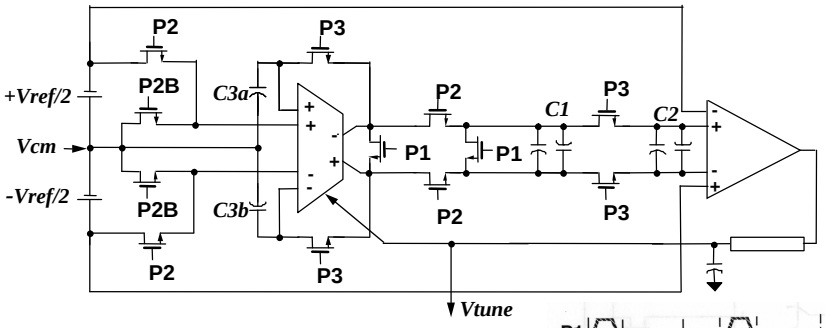
- Assume differential integrator
- Add a pair of auxiliary inputs to the input stage for offset cancellation purposes

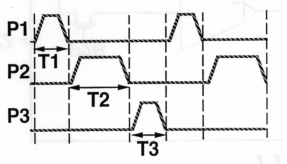




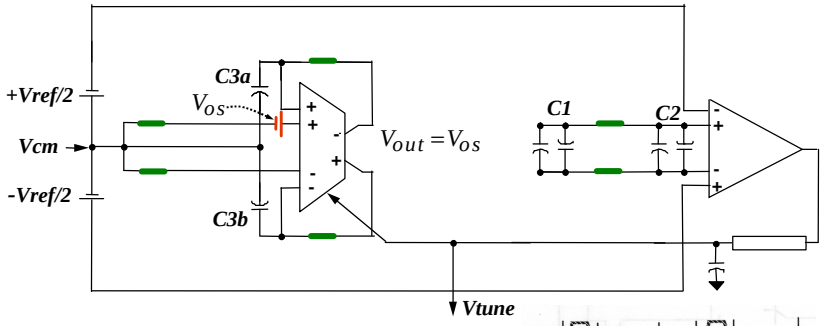

# Reference Integrator Locked to Reference Frequency
## Offset Cancellation Incorporated

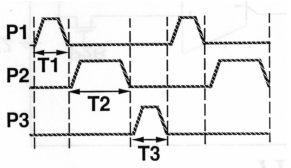



**Gm-cell → two sets of input pairs**
**Aux. input pair + *C3a,b* → Offset cancellation**
**Same clock timing**

## Reference Integrator Locked to Reference Frequency
## P3 High (Update & Store offset)




Gm-cell → Unity gain configuration via aux. inputs
*C3a,b* → Store Gm-cell offset
*C1, C2* → Charge sharing



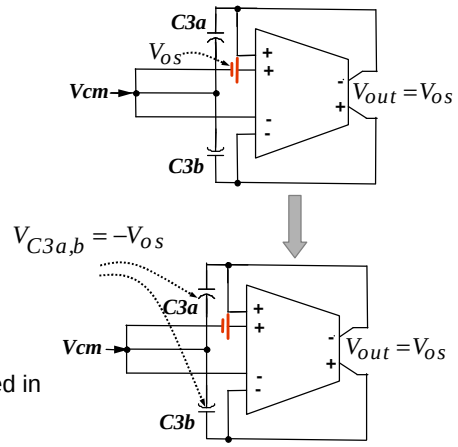
## Reference Integrator During Offset Cancellation Phase

Gm-cell → Unity gain configuration via aux. inputs, main input shorted

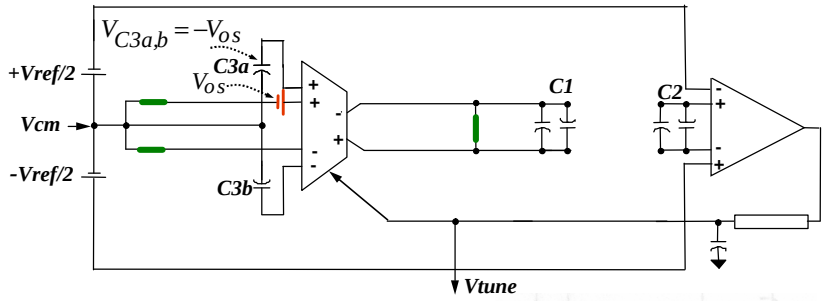
→ $V_{out} = V_{os}$

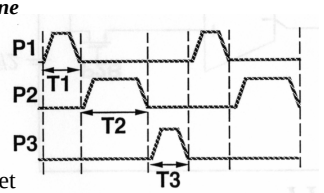
*C3a,b* acquire charge equal to $V_{os}$ → Store Gm-cell offset

*Note: This technique can be used in various other applications



## Reference Integrator Locked to Reference Frequency
## P1 High (Reset)

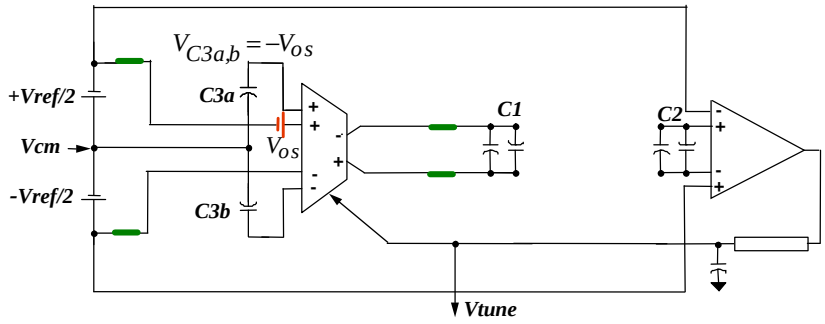



Gm-cell → Reset.
*C1* → Discharge
*C2* → Hold Charge
C3a,b → Hold Charge
→ Offset stored on C3a,b cancels gm-cell offset

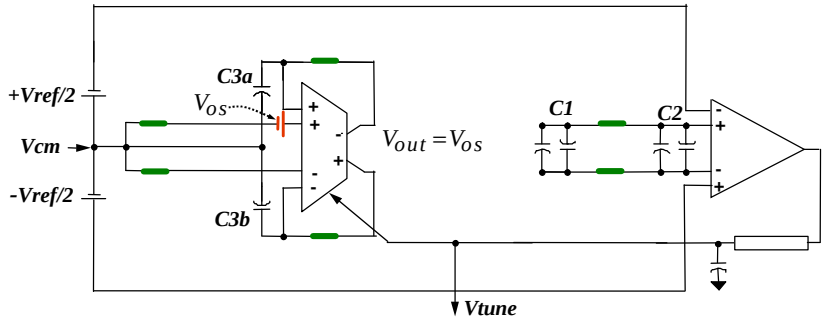


## Reference Integrator Locked to Reference Frequency
## P2 High (Charge)




Gm-cell → Charging C1
*C3a,b* → Store Gm-cell offset
*C2* → Hold charge

## Summary
## Reference Integrator Locked to Reference Frequency




***Key point: Tuning error due to Gm-cell offset cancelled***



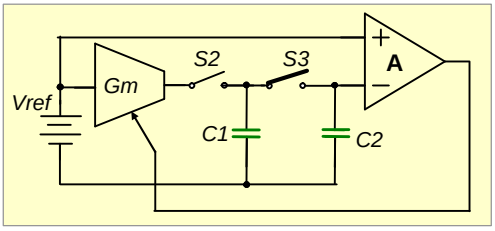
## Summary
## Reference Integrator Locked to Reference Frequency

Tuning error due to gm-cell offset voltage resolved

Advantage over previous schemes:

→ $f_{clk}$ can be chosen to be at much higher frequencies compared to filter bandwidth ($N>1$)

→ Feedthrough of clock attenuated by filter




*Feedback forces Gm to vary so that :*

$$t_{intg} = \frac{C1}{Gm} = N / fclk$$
$$or$$
$$w_0^{intg} = \frac{Gm}{C1} = fclk / N$$

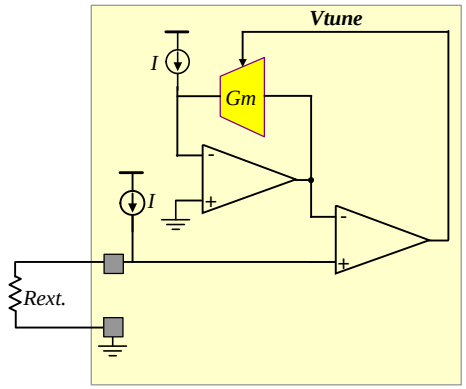
## DC Tuning of Resistive Timing Element

Rext used to lock Gm or on-chip R

Feedback forces *Gm=1/Rext*

Issues with DC offset

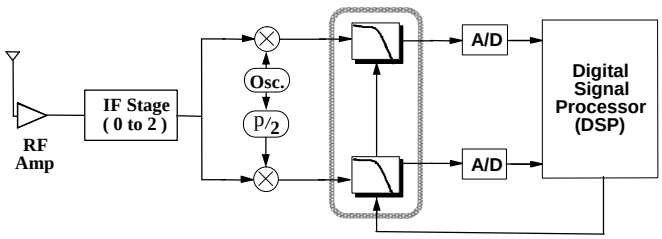
Account for capacitor variations in the gm-C implementation by trimming




Ref: C. Laber and Gray, "A 20MHz 6th Order BiCMOS Parasitic Insensitive Continuous-time Filter and Second Order Equalizer Optimized for Disk Drive Read Channels," *IEEE Journal of Solid State Circuits*, Vol. 28, pp. 462-470, April 1993

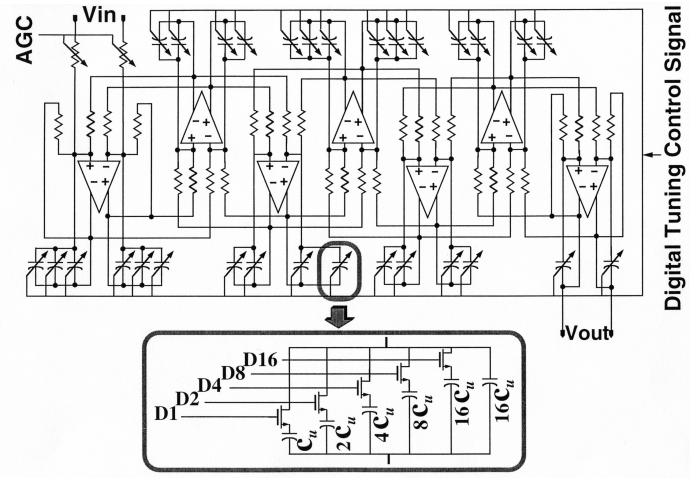


## Digitally Assisted Frequency Tuning Example:Wireless Receiver Baseband Filters



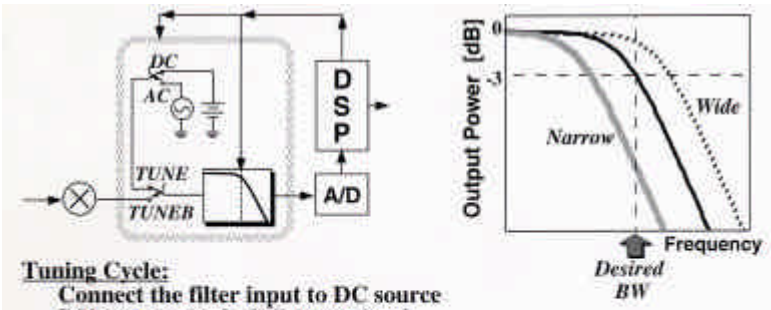

- Systems where filter is followed by ADC & DSP
  - Take advantage of existing digital signal processor to periodically update the filter critical frequency
  - Filter tuned only at the outset of each data transmission session (off-line tuning)

## Example: Seventh Order Tunable Low-Pass OpAmp-RC Filter





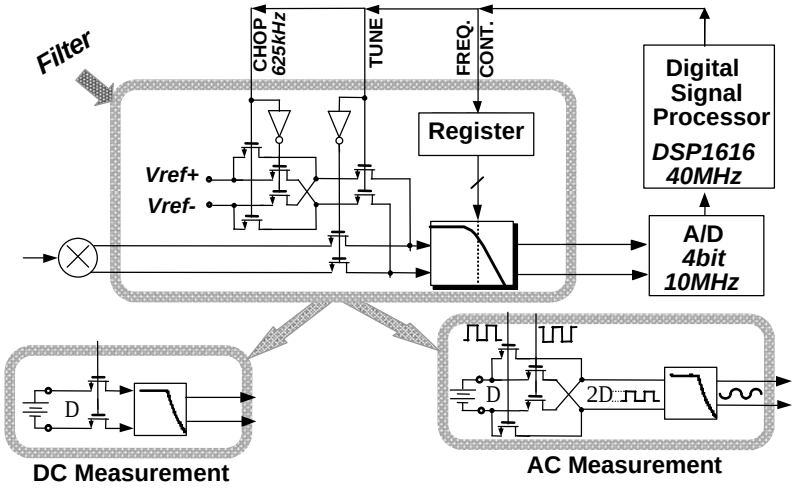

## Digitally Assisted Filter Tuning Concept




**Tuning Cycle:**

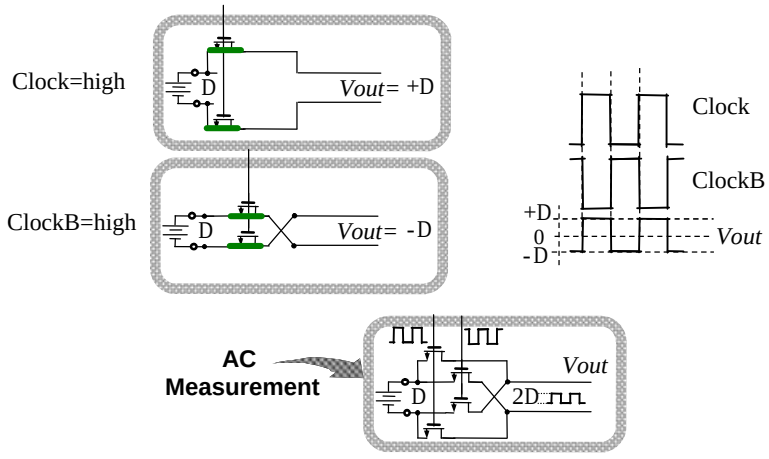
Connect the filter input to DC source
DSP measures the DC power level
Connect the filter input to AC souce (freq. -> desired -3dB freq.)
DSP measures the AC signal power level
If DC = 4*AC
Then filter is tuned
Else If DC > 4*AC
Then widen the filter bandwidth & repeat
Else narrow the filter bandwidth & repeat

## Practical Implementation of Frequency Tuning

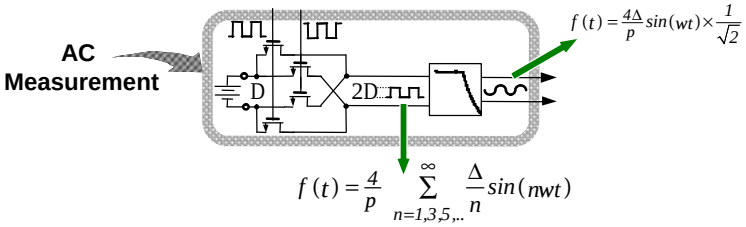





## Practical Implementation of Frequency Tuning
## AC Signal Generation



## Practical Implementation of Frequency Tuning

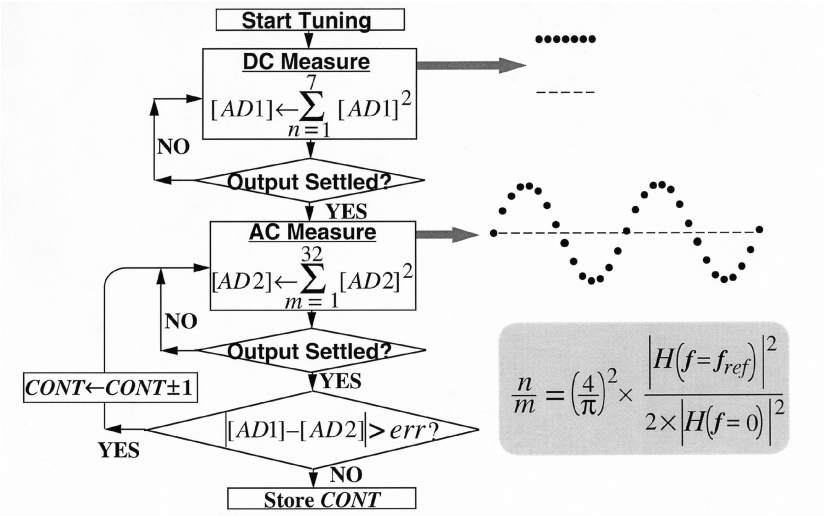



- Input signal chosen to be a square wave due to ease of generation
- Filter input signal comprises a sinusoidal waveform @ the fundamental frequency + its odd harmonics:

*Key Point: The filter itself attenuates the unwanted odd harmonics → Inaccuracy incurred by the harmonics negligible*



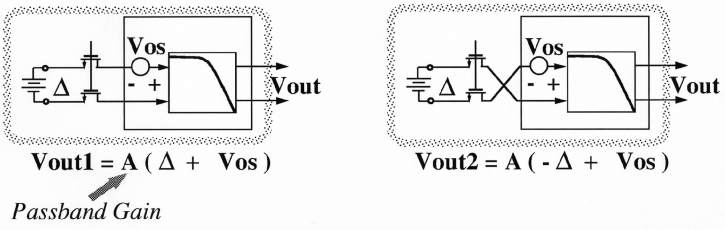
## Simplified Frequency Tuning Flowchart



# Offset Compensation

**In cases where the filter DC offset cause significant error in tuning (i.e. high passband gain)**

- **Offset compensation needed:**
  - ⇨**DC measurement performed in two steps:**



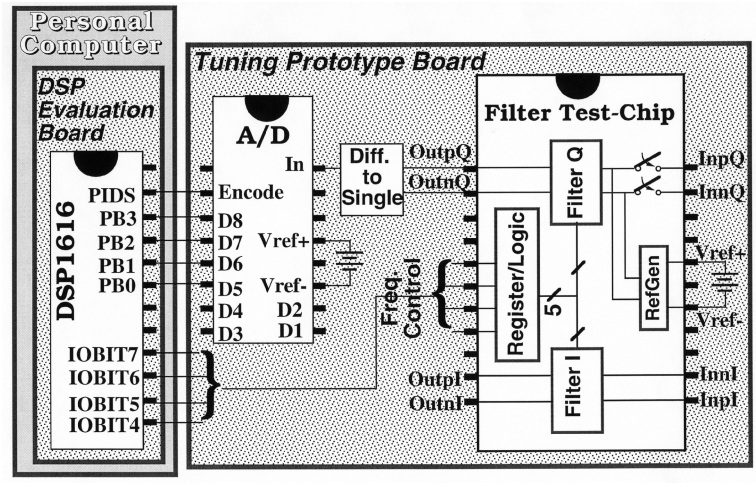

⇨**DSP extracts: Offset component ➡ 1/2(Vout1 + Vout2) = A . Vos**

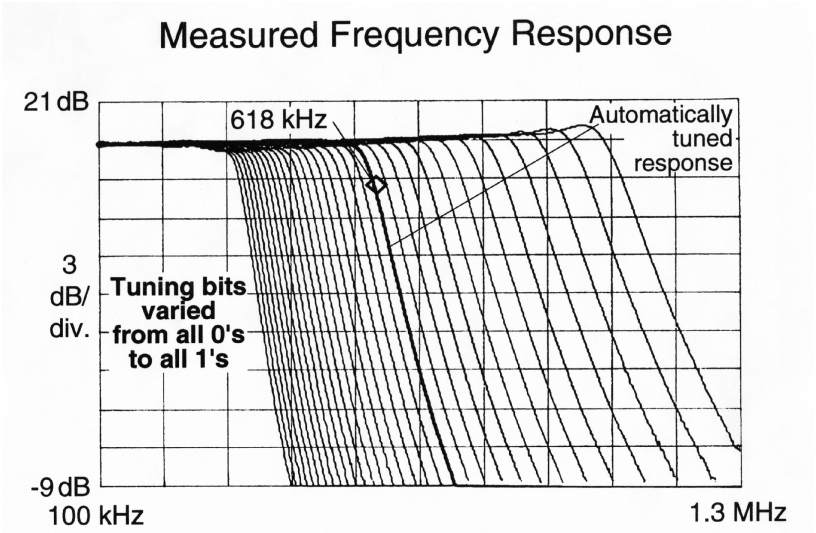
**DC component ➡ 1/2(Vout1 - Vout2) = A . Δ**

⇨**DSP substracts Vos from all subsequent AC measurement**



# Filter Tuning Prototype Diagram




Measured Frequency Response
21 dB
618 kHz
Automatically tuned response
3 dB/ div.
Tuning bits varied from all 0's to all 1's
-9 dB
100 kHz
1.3 MHz



# Chip Photo

## Measured Tuning Characteristics

| | | |
|---|---|---|
| **Tunable frequency range (nom. process)** | | **370kHz to 1.1Ml** |
| **Variations due to process** | | **±50%** |
| **I/Q bandwidth imbalance** | | **0.1%** |
| **Tuning resolution** | ***Measured*** | **3.8%** |
| **(620kHz frequency range)** | ***Expected*** | **2-5%** |
| **Tuning time** | ***Coarse+Fine*** | **max. 800µsec** |
| | ***Fine only*** | **min. 50µsec** |
| **Memory space required for tuning routine** | | **250 byte** |



## Off-line Digitally Assisted Tuning

- Advantages:
  - No reference signal feedthrough since tuning does not take place during data transmission (off-line)
  - Minimal additional hardware
  - Small amount of programming
- Disadvantages:
  - If acute temperature change during data transmission, filter may slip out of tune!
    - Can add fine tuning cycles during dead periods of data transmission

Ref: H. Khorramabadi, M. Tarsia and N.Woo, "Baseband Filters for IS-95 CDMA Receiver Applications Featuring Digital Automatic Frequency Tuning," *1996 International Solid State Circuits Conference*, pp. 172-173.

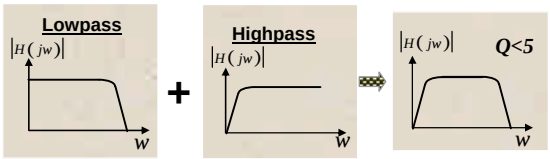
## Summary: Continuous-Time Filter Frequency Tuning

- Trimming
  - Expensive & does not account for temperature and supply etc… variations
- Automatic frequency tuning
  - Continuous tuning
    - Master VCF used in tuning loop
      - Tuning quite accurate
      - Issue → reference signal feedthrough to the filter output
    - Master VCO used in tuning loop
      - Design of reliable & stable VCO challenging
      - Issue → reference signal feedthrough
    - Single integrator in negative feedback loop forces time-constant to be a function of accurate clock frequency
      - More flexibility in choice of reference frequency → less feedthrough issues
    - DC locking of a replica of the integrator to an external resistor
      - DC offset issues & does not account for integrating capacitor variations
  - Periodic tuning
      - Requires digital capability + minimal additional hardware
      - Advantage of no reference signal feedthrough since tuning performed off-line

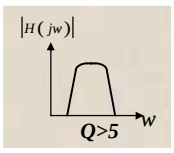


## Bandpass Filters

- Bandpass Filters:
  - $Q < 5$ → Combination of lowpass & highpass

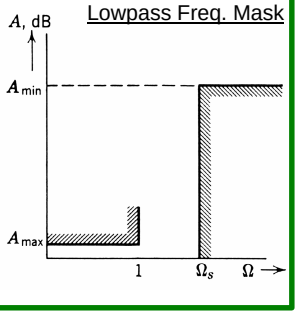



  - $Q > 5$ → Direct implementation

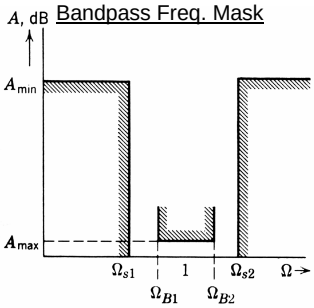


# Direct Implementation
# Narrow-Band Bandpass Filters

Lowpass Freq. Mask




Bandpass Freq. Mask



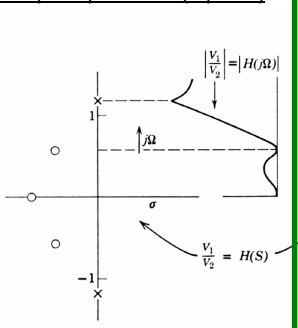

$$s \Longrightarrow = Q \times \left[ \frac{s}{w_c} + \frac{w_c}{s} \right] \qquad \frac{\Omega_s}{\Omega_c} = \frac{\Omega_{s2} - \Omega_{s1}}{\Omega_{B2} - \Omega_{B1}}$$

- Design based on lowpass prototype for narrow band filters
- Same lowpass tables used

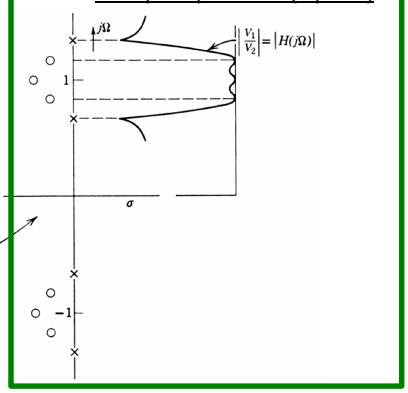


# Lowpass to Bandpass Transformation

Lowpass pole/zero (s-plane)




Bandpass pole/zero (s-plane)




From: Zverev, *Handbook of filter synthesis*, Wiley, 1967- p.156.

# Lowpass to Bandpass Transformation Table

Lowpass filter structures & tables used to derive bandpass filters

$$Q = Q_{filter}$$

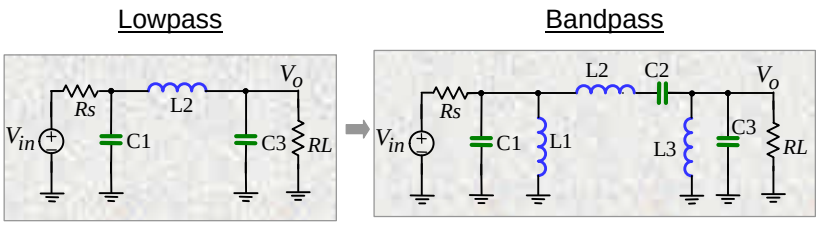
From:
Zverev,
*Handbook of filter synthesis*,
Wiley, 1967- p.157.

| LP | BP | BP Values |
|---|---|---|
| $C'$ | $C$ in parallel with $L$ | $C = QC' \times \frac{1}{R_r w_r}$, $L = \frac{1}{QC'} \times \frac{R_r}{w_r}$ |
| $L'$ | $L$ in series with $C$ | $L = QL' \times \frac{R_r}{w_r}$, $C = \frac{1}{QC'} \times \frac{1}{R_r w_r}$ |

$C'$ & $L'$ *are normilzed LP values*



# Lowpass to Bandpass Transformation




- Each capacitor replaced by parallel L& C
- Each inductor replaced by series L&C

# Lowpass to Bandpass Transformation

$$C_1 = QC_1' \times \frac{1}{Rw_0}$$

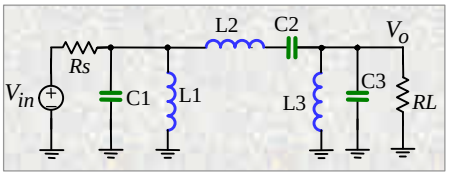
$$L_1 = \frac{1}{QC_1'} \times \frac{R}{w_0}$$

$$C_2 = \frac{1}{QL_2'} \times \frac{1}{Rw_0}$$

$$L_2 = QL_2' \times \frac{R}{w_0}$$

$$C_3 = QC_3' \times \frac{1}{Rw_0}$$

$$L_3 = \frac{1}{QC_3'} \times \frac{R}{w_0}$$




Where:

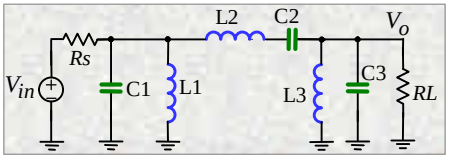
$C_1'$ , $L_2'$ , $C_3'$ , → normalized lowpass values

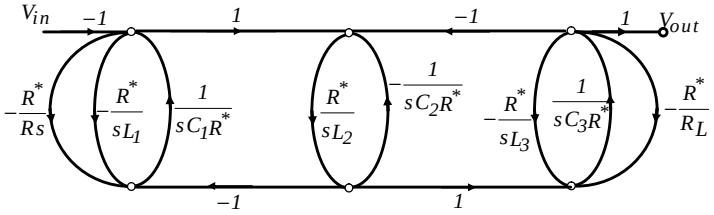
$Q$ → bandpass filter quality factor &

$w_0$ → filter center frequency



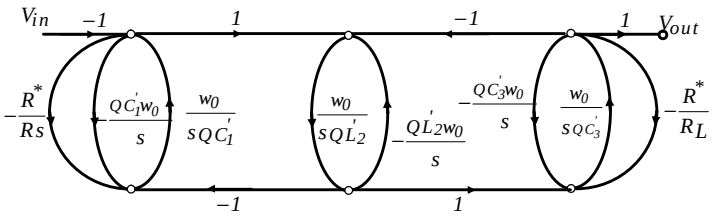
# Signal Flowgraph
# 6th Order Bandpass Filter




Note each C & L in the original lowpass prototype → replaced by a resonator
Substituting the bandpass L1, C1,….. by their normalized lowpass equivalent previous page
The resulting SFG is:

# Signal Flowgraph
# 6th Order Bandpass Filter

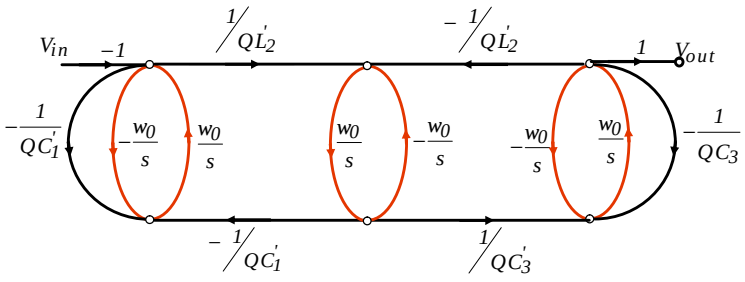



•Note the integrators have different time constants
- Ratio of time constants for each resonator ~$1/Q^2$
  - → typically, requires high component ratios
  - → poor matching

•Desirable to convert SFG so that all integrators have equal time constants for optimum matching.
- •Scale nodes to obtain equal integrator time constant

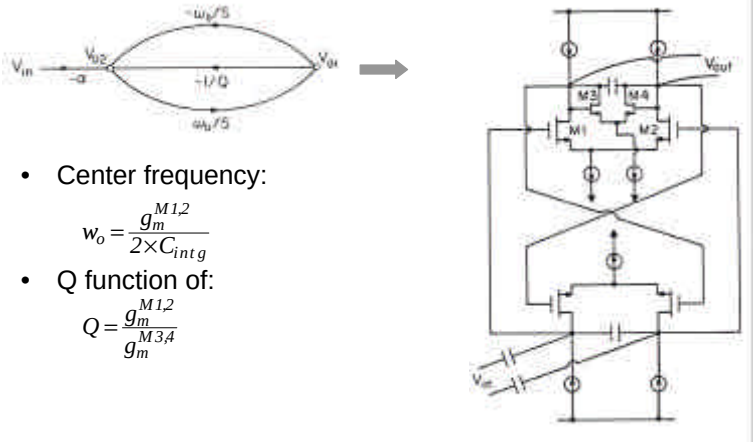


# Signal Flowgraph
# 6th Order Bandpass Filter




•Note: Three resonators
•All integrator time-constants are equal
•Let us try to build this bandpass filter using the simple Gm-C structure

## Second Order Gm-C Filter
## Using Simple Source-Couple Pair Gm-Cell




- Center frequency:

$$w_o = \frac{g_m^{M1,2}}{2 \times C_{intg}}$$

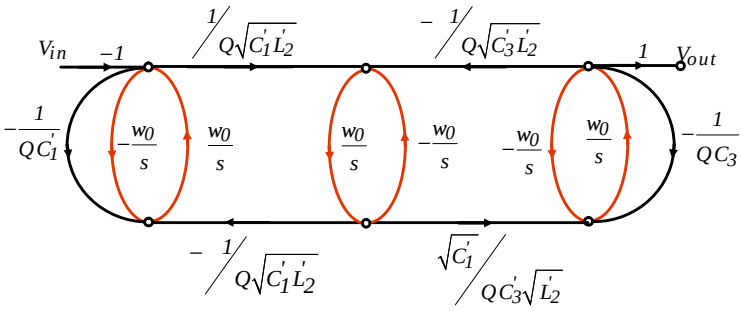
- Q function of:

$$Q = \frac{g_m^{M1,2}}{g_m^{M3,4}}$$

To use this structure it is easier to couple resonators through capacitive coupling

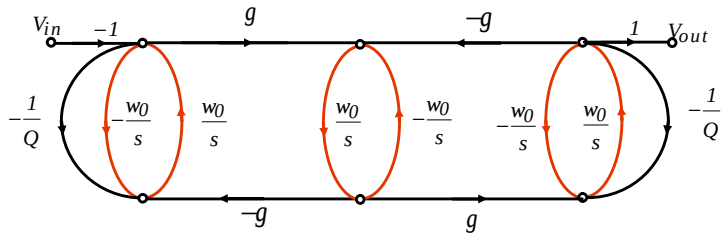


## Signal Flowgraph
## 6th Order Bandpass Filter




Modified signal flowgraph to have equal coupling between resonators
•In most filter cases $C_1' = C_3'$
•Example: For a butterworth lowpass filter $C_1' = C_3' = 1$ & $L_2' = 2$
•Assume desired overall bandpass filter $Q=10$

# Sixth Order Bandpass Filter Signal Flowgraph

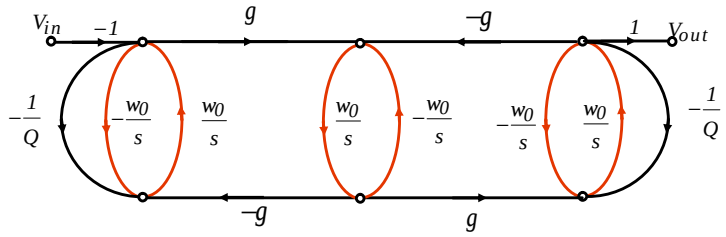



•Where for a Butterworth shape $g = \frac{1}{Q\sqrt{2}}$

•Since $Q=10$ then: $g \approx \frac{1}{14}$



# Sixth Order Bandpass Filter Signal Flowgraph

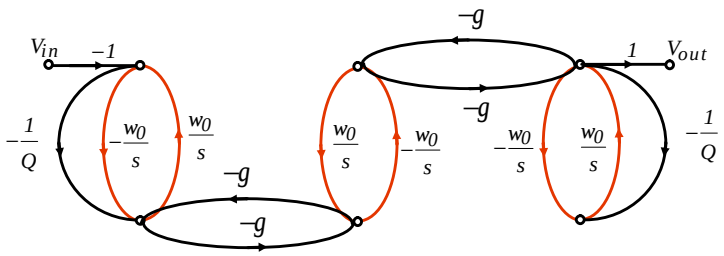



• Coupling paths (γ) between resonators can be implemented with extra differential input pairs

•Or modify SFG as shown in next page:

# Sixth Order Bandpass Filter Signal Flowgraph

For narrow band filters (high Q) where frequencies within the passband are close to $\omega_0$ narrow-band approximation can be used:
The resulting SFG:




→ Bidirectional coupling paths, can easily be implemented with coupling capacitors



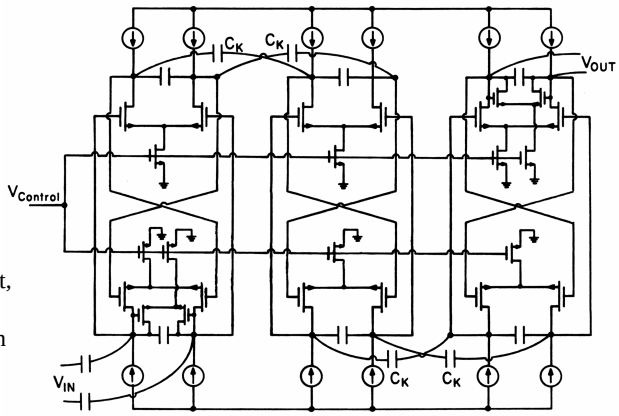
# Sixth Order Gm-C Bandpass Filter Utilizing Simple Source-Coupled Pair Gm-Cell

$$g = \frac{C_k}{2 \times C_{int\,g}}$$

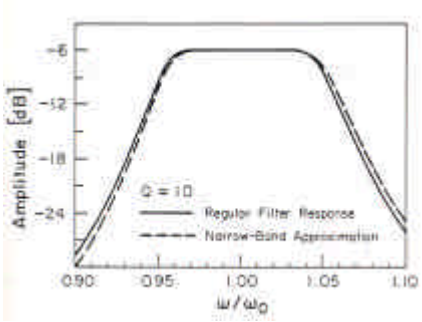
$$g = 1/14$$

$$\rightarrow C_k = \frac{1}{7 \times C_{int\,g}}$$

Parasitic C at integrator output, if unaccounted for, will result in inaccuracy in g



# Sixth Order Gm-C Bandpass Filter Frequency Response Simulation



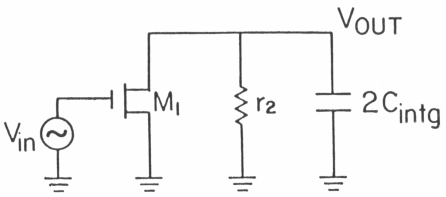



# Simplest Form of CMOS Gm-Cell Nonidealities

- DC gain (integrator Q)

$$a = \frac{g_m^{M1,2}}{g_0^{M1,2} + g_{load}}$$

$$a = \frac{2L}{q\left(V_{gs} - V_{th}\right)_{M1,2}}$$




Small Signal Differential Mode Half-Circuit

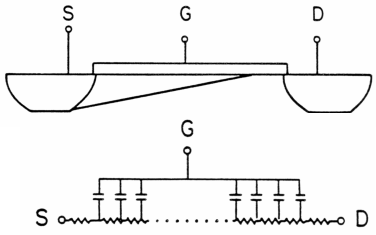
- Where a denotes DC gain & θ is related to channel length modulation by:

$$l = \frac{q}{L}$$

- Seems no extra poles!

# CMOS Gm-Cell High-Frequency Poles

Cross section view of a MOS transistor operating in saturation



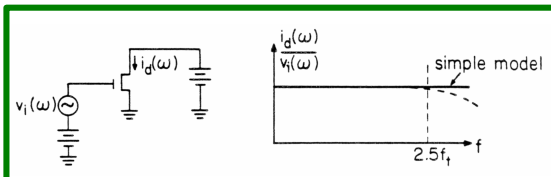

Distributed channel resistance & gate capacitance

- Distributed nature of gate capacitance & channel resistance results in infinite no. of high-frequency poles



# CMOS Gm-Cell High-Frequency Poles

$$P_2^{effective} = \frac{1}{\sum_{i=2}^{\infty} \frac{1}{P_i}}$$




High frequency behavior of an MOS transistor

$$P_2^{effective} \approx 2.5\omega_t^{M1,2}$$

$$\omega_t^{M1,2} = \frac{g_m^{M1,2}}{C_{ox}WL} = \frac{3}{2}\frac{\mu\left(V_{gs}-V_{th}\right)_{M1,2}}{L^2}$$

- Distributed nature of gate capacitance & channel resistance results in an effective pole at 2.5 times input device cut-off frequency

# CMOS Gm-Cell Quality Factor

$$a = \frac{2L}{q\left(V_{gs} - V_{th}\right)_{M1,2}} \qquad P_2^{effective} = \frac{15}{4}\frac{m\left(V_{gs} - V_{th}\right)_{M1,2}}{L^2}$$

$$Q_{real}^{intg.} \approx \frac{1}{\frac{1}{a} - w_o \sum_{i=2}^{\infty}\frac{1}{p_i}}$$

$$\frac{1}{Q_{real}^{intg.}} \approx \frac{q\left(V_{gs} - V_{th}\right)_{M1,2}}{2L} - \frac{4}{15}\frac{w_o L^2}{m\left(V_{gs} - V_{th}\right)_{M1,2}}$$

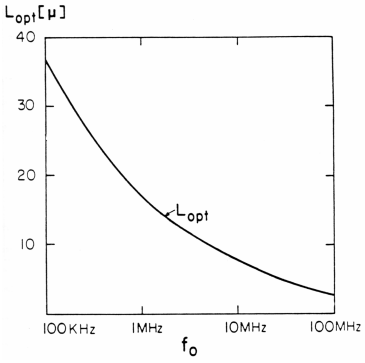
- Note that the phase lead associated with DC gain is inversely prop. to L
- The phase lag due to high-freq. poles directly prop. to L

→ For a given $\omega_o$ there exists an optimum *L* which cancel the lead/lag phase error resulting in high integrator *Q*



# CMOS Gm Cell Channel Length for Optimum Integrator Quality Factor

$$L_{opt.} \approx \left[\frac{15}{4}\,\frac{qm\left(V_{gs} - V_{th}\right)^2_{M1,2}}{w_o}\right]^{1/3}$$




- Optimum channel length computed based on process parameters