EECS 247
Lecture 10

• Switched-capacitor filters
  – Switched-capacitor network electronic noise
  – Switched-capacitor integrators
    • DDI integrators
    • LDI integrators
    • Effect of parasitic capacitance
    • Bottom-plate integrator topology
  – Resonators
  – Bandpass filters
  – Lowpass filters
    • Termination implementation
    • Transmission zero implementation
  – Switched-capacitor filter design considerations
  – Switched-capacitor filters utilizing double sampling technique
  – Effect of non-idealities

Summary of last lecture

• Continuous-time filters continued
  – Various Gm-C filter implementations
  – Comparison of continuous-time filter topologies

• Switched-capacitor filters
  – Emulating resistor via switched-capacitor network
  – 1st order switched-capacitor filter
  – Switch-capacitor filter considerations:
    • Issue of aliasing and how to avoid it
      – Sample at high enough frequency so that the entire range of signals including the parasitics are at freqs < \( f_s/2 \)
      – Use of anti-aliasing prefilters
    • Effect of sample and hold
Switched-Capacitor Network Noise

- During $\phi_1$ high: Resistance of switch $S1$ ($R_{on,S1}$) produces a noise voltage on $C$ with variance $kT/C$ (lecture 1- first order filter noise)

- The corresponding noise charge is:

  $$ Q^2 = C^2V^2 = C^2 \cdot kT/C = kTC $$

- $\phi_1$ low: S1 opens $\Rightarrow$ This charge is sampled

Switched-Capacitor Noise

- During $\phi_2$ high: Resistance of switch $S2$ contributes to an uncorrelated noise charge on $C$ at the end of $\phi_2$ : with variance $kT/C$

- Mean-squared noise charge transferred from $v_{in}$ to $v_{out}$ per sample period is:

  $$ Q^2 = 2kTC $$
Switched-Capacitor Noise

- The mean-squared noise current due to S1 and S2's kT/C noise is:
  \[ i = \frac{Q}{t} \quad \text{then} \quad i^2 = \left(\frac{Qf_s}{C}\right)^2 = 2k_BT C f_s^2 \]

- This noise is approximately white and distributed between 0 and \( f_s/2 \) (noise spectra → single sided by convention)
  The spectral density of the noise is:
  \[ \frac{i^2}{\Delta f} = \frac{2k_BT C f_s^2}{f_s/2} = 4k_BT C f_s \]

  \[ \text{Since } \frac{1}{R_{EQ}} = \frac{f_s}{C} \quad \text{then:} \quad \frac{i^2}{\Delta f} = \frac{4k_BT}{R_{EQ}} \]

  → S.C. resistor noise = a physical resistor noise with same value!

Periodic Noise Analysis

SpectreRF

Sampling Noise from SC S/H

SpectreRF PNOISE: check noisetype=timedomain noisetimepoints=[...] as alternative to ZOH, noiseskipcount=large might speed up things in this case.
Sampled Noise Spectrum

Density of sampled noise including sinc distortion

Sampled noise normalized density corrected for sinc distortion

Total Noise

Sampled simulated noise in 0 … f_s/2: 62.2μV rms

(expect 64μV for 1pF)
Switched-Capacitor Integrator

\[ V_0 = \frac{f_s \times C_s}{C_I} \int V_{in} \, dt \]

Main advantage: No tuning needed
- critical frequency function of ratio of capacitors & clock freq.
**Continuous-Time versus Discrete Time Analysis Approach**

<table>
<thead>
<tr>
<th>Continuous-Time</th>
<th>Discrete-Time</th>
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</thead>
<tbody>
<tr>
<td>• Write differential equation</td>
<td>• Write difference equation ( \rightarrow ) relates output sequence to input sequence</td>
</tr>
<tr>
<td>• Laplace transform ( (F(s)) )</td>
<td>( V_o(nT_s) = V_i\left[\left(n-I\right)T_s\right] ) ( \cdots \cdots \cdot )</td>
</tr>
<tr>
<td>• Let ( s = j\omega ) ( \rightarrow F(j\omega) )</td>
<td>• Use delay operator ( z^{-l} ) to transform the recursive realization to algebraic equation in ( z ) domain</td>
</tr>
<tr>
<td>• Plot (</td>
<td>F(j\omega)</td>
</tr>
<tr>
<td></td>
<td>• Set ( z = e^{j\omega T} )</td>
</tr>
<tr>
<td></td>
<td>• Plot mag./phase versus frequency</td>
</tr>
</tbody>
</table>

**Discrete Time Design Flow**

- Transforming the recursive realization to algebraic equation in \( z \) domain:
  - Use delay operator \( z \):  
    \[
    nT_s \rightarrow 1 \\
    \left[(n-1)T_s\right] \rightarrow z^{-1} \\
    \left[(n-1/2)T_s\right] \rightarrow z^{-1/2} \\
    \left[(n+1)T_s\right] \rightarrow z^{+1} \\
    \left[(n+1/2)T_s\right] \rightarrow z^{+1/2}
    \]

* Note: \( z = e^{j\omega T_s} = \cos(\omega T_s) + j \sin(\omega T_s) \)
Switched-Capacitor Integrator

Output Sampled on $\phi_1$

\[
\begin{align*}
\Phi_1 \rightarrow & \quad Q_i[(n-1)T_s] = C_i V_i[(n-1)T_s] \, , \quad Q_i[(n-1)T_s] = Q_i[(n-3/2)T_s] \\
\Phi_2 \rightarrow & \quad Q_i[(n-1/2)T_s] = 0 \, , \quad Q_i[(n-1/2) T_s] = Q_i[(n-3/2) T_s] + Q_i[(n-1) T_s] \\
\Phi_3 \rightarrow & \quad Q_i[nT_s] = C_i V_i[nT_s] \, , \quad Q_i[nT_s] = Q_i[(n-1) T_s] + Q_i[(n-1) T_s] \\
\end{align*}
\]

Since $V_{ol} = Q_i/C_i$ & $V_i = Q_i/C_i \rightarrow C_i V_{oi}(nT_s) = C_i V_{oi}[(n-1)T_s] - C_i V_i[(n-1)T_s]$

$\Phi_1 \rightarrow \quad Q_i[(n-1)T_s] = C_i V_i[(n-1)T_s] \, , \quad Q_i[(n-1)T_s] = Q_i[(n-3/2)T_s]$

$\Phi_2 \rightarrow \quad Q_i[(n-1/2)T_s] = 0 \, , \quad Q_i[(n-1/2) T_s] = Q_i[(n-3/2) T_s] + Q_i[(n-1) T_s]$

$\Phi_3 \rightarrow \quad Q_i[nT_s] = C_i V_i[nT_s] \, , \quad Q_i[nT_s] = Q_i[(n-1) T_s] + Q_i[(n-1) T_s]$

Since $V_{ol} = Q_i/C_i$ & $V_i = Q_i/C_i \rightarrow C_i V_{oi}(nT_s) = C_i V_{oi}[(n-1)T_s] - C_i V_i[(n-1)T_s]$
Switched-Capacitor Integrator
Output Sampled on $\phi_1$

$$C_I \ V_o(nT_s) = C_I \ V_o[(n-1)T_s] - C_s \ V_{in}[(n-1)T_s]$$

$$V_o(nT_s) = V_o[(n-1)T_s] - C_s \ V_{in}[(n-1)T_s]$$

$$V_o(Z) = Z^{-1}V_o(Z) - Z^{-1}C_s \ V_{in}(Z)$$

$$\frac{V_o(Z)}{V_{in}} = -\frac{C_s}{C_I} \times \frac{Z^{-1}}{1-Z^{-1}}$$

DDI (Direct-Transform Discrete Integrator)

z-Domain Frequency Response

- LHP singularities in s-plane map into inside of unit-circle in z-domain
- RHP singularities in s-plane map into outside of unit-circle in z-domain
- The j$\omega$ axis maps onto the unit-circle
- Particular values:
  - $f = 0$ $\Rightarrow$ $z = 1$
  - $f = f_s/2$ $\Rightarrow$ $z = -1$
z-Domain Frequency Response

- The frequency response is obtained by evaluating $H(z)$ on the unit circle at:
  
  $$z = e^{j\omega T} = \cos(\omega Ts) + j \sin(\omega Ts)$$

- Once $z=-1$ ($f_s/2$) is reached, the frequency response repeats, as expected.

- The angle to the pole is equal to $360^\circ$ (or $2\pi$ radians) times the ratio of the pole frequency to the sampling frequency.

Switched-Capacitor Direct-Transform Discrete Integrator

\[
\frac{V_o(z)}{V_{in}} = -\frac{C_s}{C_I} \times \frac{z^{-1}}{1-z^{-1}}
\]

\[
= -\frac{C_s}{C_I} \times \frac{1}{z-1}
\]
DDI Integrator
Pole-Zero Map in z-Plane

\[ z - l = 0 \Rightarrow z = l \]
on unit circle

Pole from \( f \) \( \Rightarrow 0 \)
in s-plane mapped to \( z = +l \)

As frequency increases \( z \) domain pole moves on unit circle (CCW)

Once pole gets to:
\( z = -1 \) \( (f = f_s / 2) \)
\( \Rightarrow \) frequency response repeats

DDI Switched-Capacitor Integrator

\[ \frac{V_D(z)}{V_{in}} = -\frac{C_s}{C_t} \times \frac{e^{-jz}}{1-z} \]
\( z = e^{j\omega t} \)

\[ = -\frac{C_s}{C_t} \times \frac{1}{1-e^{j\omega t}} \times \frac{e^{-j\omega t/2}}{2j} \times e^{-j\omega t} / 2 \]
\[ = -\frac{C_s}{C_t} \times \frac{1}{2j} \times e^{-j\omega t} / 2 \times \sin(\omega t / 2) \]

Ideal Integrator
Magnitude Error
Phase Error
Example: Mag. & phase error for:
1. $f/f_s = 1/12 \Rightarrow$ Mag. error = 1% or 0.1dB
   Phase error = 15 degree
   $Q_{mag} = -3.8$
2. $f/f_s = 1/32 \Rightarrow$ Mag. error = 0.16% or 0.014dB
   Phase error = 5.6 degree
   $Q_{mag} = -10.2$

DDI Integrator:
- magnitude error no problem
- phase error major problem

5th Order Low-Pass Switched Capacitor Filter
Built with DDI Integrators

Example:
5th Order Elliptic Filter
Singualrities pushed towards RHP due to integrator excess phase
Switched Capacitor Filter Build with DDI Integrator

Continuous-Time Prototype

Switched-Capacitor Integrator Output Sampled on $\phi_2$

Sample output $\frac{1}{2}$ clock cycle earlier
$\rightarrow$ Sample output on $\phi_2$
Switched-Capacitor Integrator
Output Sampled on $\phi_2$

$\Phi_1 \rightarrow Q_s[(n-1)T_s] = C_s V_i[(n-1)T_s]$,

$Q_i[(n-1)T_s] = Q_i[(n-3/2)T_s]$,

$\Phi_2 \rightarrow Q_s[(n-1/2)T_s] = 0$,

$Q_i[(n-1/2)T_s] = Q_i[(n-3/2)T_s] + Q_s[(n-1)T_s]$,

$\Phi_1 \rightarrow Q_s[nT_s] = C_s V_i[nT_s]$,

$Q_i[nT_s] = Q_i[(n-1)T_s] + Q_s[(n-1)T_s]$,

$\Phi_2 \rightarrow Q_s[(n+1/2)T_s] = 0$,

$Q_i[(n+1/2)T_s] = Q_i[(n-1/2)T_s] + Q_s[nT_s]$.

Using the $z$ operator rules:

$V_{\alpha_2}(z) = -\frac{C_s}{C_i} \times \frac{z^{-1/2}}{1-z^{-1}}$

$V_{\alpha_2} = C_i V_{\alpha_2} z^{1/2} - C_s V_i$
LDI Switched-Capacitor Integrator

LDI (Lossless Discrete Integrator) \( \rightarrow \)

same as DDI but output is sampled \( \frac{1}{2} \) clock cycle earlier

\[
\frac{V_{o2}(z)}{V_{in}} = \frac{C_i}{C_f} \times \frac{z^{-1/2}}{1 - z^{-1}}, \quad z = e^{j \omega f}
\]

\[
= \frac{C_i}{C_f} \times \frac{1}{1 - e^{-j \omega f / 2}}
\]

\[
= -j \frac{C_i}{C_f} \times \frac{1}{2 \sin(\omega f / 2)}
\]

Ideal Integrator

Magnitude Error

No Phase Error!

For signals at frequencies \( \ll \) sampling freq.

\( \rightarrow \) Magnitude error negligible

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Frequency Warping

- \textbf{Frequency response}
  - Continuous time (s-plane): imaginary axis
  - Sampled time (z-plane): unit circle
- \textbf{Continuous to sampled time transformation}
  - Should map imaginary axis onto unit circle
  - How do S.C. integrators map frequencies?

\[
H_{S.C.}(z) = \frac{C_s}{C_{int}} \frac{z^{-1/2}}{1 - z^{-1}}
\]

\[
= -\frac{C_s}{C_{int}} \frac{1}{2j \sin \pi f T}
\]
CT – SC Integrator Comparison

CT Integrator

\[ H_{RC}(s) = \frac{1}{s\tau} = -\frac{1}{2\pi f_{RC}\tau} \]

SC Integrator

\[ H_{SC}(z) = \frac{C_s}{C_{int} (1 - z^{-1})^2} = -\frac{C_s}{C_{int} 2js\sin(\pi f_{SC} T_s)} \]

Identical time constants:

\[ \tau = RC = \frac{C_{int}}{f_s C_s} \]

Set: \( H_{RC}(f_{RC}) = H_{SC}(f_{SC}) \)

\[ f_{RC} = \frac{f_s}{\pi} \sin \left( \pi \frac{f_{SC}}{f_s} \right) \]

LDI Integration

\[ f_{RC} = \frac{L}{\pi} \sin \left( \pi \frac{f_{SC}}{f_s} \right) \]

- "RC" frequencies up to \( f_s / \pi \) map to physical (real) "SC" frequencies
- Frequencies above \( f_s / \pi \) do not map to physical frequencies
- Mapping is symmetric about \( f_s / 2 \) (aliasing)
- “Accurate” only for \( f_{RC} \ll f_s \)
Switched-Capacitor Filter
Built with LDI Integrators

\[ |H(j\omega)| \]

Zeros Preserved

Frequency (Hz)

\( f_s/2 \)

\( f_s \)

\( 2f_s \)

\( f \)

---

Switched-Capacitor Integrator
Parasitic Sensitivity

Effect of parasitic capacitors:

1. \( C_{p1} \) - driven by opamp o.k.
2. \( C_{p2} \) - at opamp virtual gnd o.k.
3. \( C_{p3} \) – Charges to \( V_{in} \) & discharges into \( C_i \)

\[ \text{Problem parasitic sensitivity} \]
Parasitic Insensitive
Bottom-Plate Switched-Capacitor Integrator

Sensitive parasitic cap. → \( C_{p1} \) → rearrange circuit so that \( C_{p1} \) does not charge/discharge

\[ \phi_1 = 1 \rightarrow C_{p1} \text{ grounded} \]

\[ \phi_2 = 1 \rightarrow C_{p1} \text{ at virtual ground} \]

Solution: Bottom plate capacitor integrator

Note:
Different delay from \( V_{i+} \) & \( V_{i-} \) to either output
→ Special attention needed for input/output connections

Bottom Plate Switched-Capacitor Integrator

\[
\begin{align*}
\text{Output/Input} & \quad \text{z-Transform} \\
\text{Vo1} & \quad \text{Vo2} \\
\text{on } \phi_1 & \quad \text{on } \phi_2 \\
V_{i+} & \quad \frac{C_s}{C_I} \frac{z^{-1}}{1-z^{-1}} & \frac{C_s z^{-1/2}}{C_I} \frac{1}{1-z^{-1}} \\
V_{i-} & \quad -\frac{C_s z^{-1/2}}{C_I} \frac{1}{1-z^{-1}} & \frac{C_s}{C_I} \frac{1}{1-z^{-1}}
\end{align*}
\]
Bottom Plate Switched-Capacitor Integrator

\[ \text{z-Transform Model} \]

\[ \frac{1}{z-1} \]

\[ \frac{1}{z+1} \]

\[ \text{Input/Output z-transform} \]

\[ V_i^+ \]

\[ V_i^- \]

\[ C_I \]

\[ \phi_1 \]

\[ \phi_2 \]

\[ C_s \]

\[ \text{Delay around integrator loop is} \ (z^{-1/2} \cdot z^{1/2} = 1) \]

LDI Switched-Capacitor Ladder Filter

\[ \text{Delay around integrator loop is} \ (z^{-1/2} \cdot z^{1/2} = 1) \Rightarrow \text{LDI function} \]
Switched-Capacitor LDI Resonator

\[ \frac{\omega_1}{s} \quad \frac{\omega_2}{s} \]

\[ \omega_1 = \frac{1}{R_{eq1}C_2} = f_s \times \frac{C_1}{C_2} \]

\[ \omega_2 = \frac{1}{R_{eq3}C_4} = f_s \times \frac{C_3}{C_4} \]

Fully Differential Switched-Capacitor Resonator
Switched-Capacitor LDI Bandpass Filter
Utilizing Continuous-Time Termination

\[ \omega_0 s \sqrt{C_1 C_4} = \frac{f_s}{Q} \times \frac{C_1}{C_2} \]

\[ Q = \frac{C_2}{C_1} \]

s-Plane versus z-Plane
Example: 2\textsuperscript{nd} Order LDI Bandpass Filter
Switched-Capacitor LDI Bandpass Filter
Continuous-Time Termination

\[ f_0 = \frac{1}{2\pi f_s C_1 C_2} \]

\[ \Delta f = \frac{f_0}{Q} \]

Both accurately determined by cap ratios & clock frequency

Fifth Order All-Pole LDI Low-Pass Ladder Filter
Complex Conjugate Terminations

Fifth-Order All-Pole Low-Pass Ladder Filter Termination Implementation


Sixth-Order Elliptic LDI Bandpass Filter

Use of T-Network

High Q filter $\Rightarrow$ large cap. ratio for Q & transmission zero implementation
To reduce large ratios required $\Rightarrow$ T-networks utilized


Sixth Order Elliptic Bandpass Filter
Utilizing T-Network

$\bullet$ T-networks utilized for:
  $\bullet$ Q implementation
  $\bullet$ Transmission zero implementation

Switched-Capacitor Resonator

**Regular sampling**
Each opamp busy settling only during one of the two clock phases
→ Idle during the other clock phase

Switched-Capacitor Resonator Using Double-Sampling

**Double-sampling:**
- 2nd set of switches & sampling caps added to all integrators
- While one set of switches/caps sampling the other set transfers charge into the intg. cap
- Opamps busy during both clock phases
- Effective sampling freq. twice clock freq. while opamp bandwidth requirement remains the same
Double-Sampling Issues

Issues to be aware of:
- Jitter in the clock
- Unequal clock phases
- Mismatch in sampling caps. → parasitic passbands


Double-Sampled Fully Differential S.C. 6th Order All-Pole Bandpass Filter

Sixth Order Bandpass Filter Signal Flowgraph

\[ \begin{align*}
V_{in} & \quad -I \quad \gamma \quad -\gamma \quad I \quad V_{out} \\
\frac{-I}{Q} & \quad \frac{\omega_0}{s} \quad \frac{\omega_0}{s} \quad \frac{-\omega_0}{s} \quad \frac{-\omega_0}{s} \quad \frac{\omega_0}{s} \quad \frac{-I}{Q}
\end{align*} \]

Double-Sampled Fully Differential 6th Order S.C. All-Pole Bandpass Filter

- Cont. time termination (Q) implementation
- Folded-Cascode opamp with \( f_c = 100\, \text{MHz} \) used
- Center freq. 3.1 MHz, filter Q=55
- Clock freq. 12.83 MHz \( \rightarrow \) effective oversampling ratio 8.27
- Measured dynamic range 46 dB (IM3=1%)

Effect of Opamp Nonidealities on Switched Capacitor Filter Behaviour

- Opamp finite gain
- Opamp finite bandwidth
- Finite slew rate of the opamp

Effect of Opamp Non-Idealities

Finite DC Gain

Finite DC gain same effect in S.C. filters as for C.T. filters
Effect of Opamp Non-Idealities
Finite Opamp Bandwidth

Assumption-
Opamp → does not slew (will be revisited)
Opamp has only one pole → exponential settling


Effect of Opamp Non-Idealities
Finite Opamp Bandwidth

\[ H_{actual}(Z) = H_{ideal}(Z) \left[ 1 - e^{-k} + e^{-k} \times \frac{C_l}{C_l + C_s} \right] \]

where \( k = \pi \times \frac{C_l}{C_l + C_s} \times f_{t} \)

\( f_t \rightarrow \text{Opamp unity-gain-frequency} \), \( f_s \rightarrow \text{Clock frequency} \)

Effect of Opamp Finite Bandwidth on Filter Magnitude Response

\[ |T|_{\text{non-ideal}} / |T|_{\text{ideal}} \ (\text{dB}) \]

Magnitude deviation due to finite opamp unity-gain-frequency

Example: 2nd order bandpass with Q=25

Effect of Opamp Finite Bandwidth
Maximum Achievable Q

Max. allowable biquad Q for peak gain change <10%


Example:
For Q of 40 required
Max. allowable biquad Q for peak gain change <10%

1- \( \frac{f_c}{f_s} = \frac{1}{32} \)
\( \frac{f_c}{f_t} \approx 0.02 \)
\( f_t > 50f_c \)

2- \( \frac{f_c}{f_s} = \frac{1}{12} \)
\( \frac{f_c}{f_t} \approx 0.035 \)
\( f_t > 28f_c \)

3- \( \frac{f_c}{f_s} = \frac{1}{6} \)
\( \frac{f_c}{f_t} \approx 0.05 \)
\( f_t > 20f_c \)

Effect of Opamp Finite Bandwidth on Filter Critical Frequency

Critical frequency deviation due to finite opamp unity-gain-frequency

Example: 2nd order filter

\[
\Delta \omega_c / \omega_c = \frac{fc}{fs} - 1
\]

Example:
For maximum critical frequency shift of <1%

1- \( \frac{fc}{fs} = \frac{1}{32} \), \( \frac{f_c}{f_s} = 0.028 \)
   \( f_s > 36f_c \)

2- \( \frac{fc}{fs} = \frac{1}{12} \), \( \frac{f_c}{f_s} = 0.046 \)
   \( f_s > 22f_c \)

3- Active RC
   \( \frac{f_c}{f_s} = 0.008 \)
   \( f_s > 125f_c \)

Sources of Distortion in Switched-Capacitor Filters

- Distortion induced by finite slew rate of the opamp
- Opamp output/input transfer characteristic non-linearity
- Capacitor non-linearity
- Distortion incurred by finite setting time of the opamp
- Distortion due to switch clock feed-through and charge injection

What is Slewing?

Assumption:
Integrator opamp is a simple class A transconductance type differential pair with fixed tail current $I_{ss}$
What is Slewing?

$V_{Cs} > V_{max}$
- Output current constant $I_o = I_{ss}$
- $V_o$ ramps up/down → Slewing

After $V_{Cs}$ is discharged enough to have:
$V_{Cs} < V_{max}$ → $I_o = g_m V_{Cs}$ → Exponential or overshoot settling

Distortion Induced by Opamp Finite Slew Rate
Ideal Switched-Capacitor Output Waveform

\[ \phi_1 \]
\[ \phi_2 \]
\[ V_{in} \]
\[ V_{out} \]
\[ V_{cs} \]

\[ C_I \]
\[ C_s \]

\[ \phi_2 \] High \( \rightarrow \) Charge transferred from \( C_s \) to \( C_I \)

Slew Limited Switched-Capacitor Output Settling

\[ \phi_1 \]
\[ \phi_2 \]
\[ V_{out-ideal} \]
\[ V_{out-real} \]

Slewing Linear
Linear Settling
Slewing Linear Settling
Distortion Induced by Finite Slew Rate of the Opamp


Distortion Induced by Opamp Finite Slew Rate

- Error due to exponential settling changes linearly with signal amplitude
- Error due to slew-limited settling changes non-linearly with signal amplitude (doubling signal amplitude X4 error)
  
\[ HD_k = \frac{V_o}{S_T} \frac{8\left(\sin \frac{a_k T_i}{2}\right)^2}{\pi k (k^2 - 4)} \]

\[ \rightarrow HD_3 = \frac{V_o}{S_T} \frac{8\left(\sin \frac{a_3 T_i}{2}\right)^2}{15\pi} \]

Distortion Induced by Opamp Finite Slew Rate Example

Distortion Induced by Finite Slew Rate of the Opamp

- Note that for a high order switched capacitor filter → only the last stage slewing will affect the output linearity (as long as the previous stages settle to the required accuracy)
  - Can reduce slew limited linearity by using an amplifier with a higher slew rate only for the last stage
  - Can reduce slew limited linearity by using class A/B amplifiers
    - Even though the output/input characteristics is non-linear the significantly higher slew rate compared to class A amplifiers helps improve slew rate induced distortion
- In cases where the output is sampled by another sampled data circuit (e.g. an ADC or a S/H) → no issue with the slewing of the output as long as the output settles to the required accuracy & is sampled at the right time