EE247
Lecture 11

• Switched-Capacitor Filters (continued)
  – Effect of non-idealities
  – Bilinear switched-capacitor filters
  – Filter design summary
• Comparison of various filter topologies
• Data Converters

Summary
Last Lecture

• Switched-capacitor filter design considerations
  – DDI & LDI Integrator characteristics
  – Bottom-plate LDI integrator overcomes parasitic sensitivity issues
  – Continuous-time and complex conjugate terminations
  – Use of T-networks to implement high capacitor ratios
• Switched-capacitor filters utilizing double sampling technique
• Effect of non-idealities
  – Opamp finite gain
  – Opamp finite bandwidth
  – Finite slew rate of the opamp (this lecture)
Switched-Capacitor Direct-Transform Discrete (DDI) Integrator

\[
\frac{V_o(z)}{V_{in}} = -C_s \times \frac{z^{-1}}{1-z^{-1}}
\]

DDI Switched-Capacitor Integrator

\[
\frac{V_o(z)}{V_{in}} = -C_s \times \frac{1}{1-e^{j\alpha}}
\]

\[
= -C_s \times \frac{1}{1-e^{j\alpha}} \times \frac{e^{-j\alpha/2}}{2\sin(\alpha/2)} \times e^{-j\alpha/2}
\]

since: \( \sin \alpha = e^{j\alpha} - e^{-j\alpha} \)
DDI Switched-Capacitor Integrator

Example: Mag. & phase error for:
1. \( f_{\text{max}} \frac{\sin}{f_s} = 1/12 \) → Mag. error \( = 1\% \) or 0.1dB
   
   Phase error \( = \omega T/2 = -\pi f_s = -\pi/12 \) [radian] → 15 [degree]
   
   \( Q_{\text{intg}} \) → 1/ phase error @ \( \omega_0 \) [radian] (Lecture 5 page 1)
   
   \( Q_{\text{intg}} = -12/\pi = -3.8 \)

2. \( f_s = 1/32 \) → Mag. error \( = 0.16\% \) or 0.014dB
   
   Phase error \( = \omega T/2 = -\pi f_s = -\pi/32 \) [radian] → 5.6 [degree]
   
   \( Q_{\text{intg}} = -32/\pi = -10.2 \)

LDI Switched-Capacitor Integrator

LDI (Lossless Discrete Integrator) → same as DDI but output is sampled ½ clock cycle earlier

\[
\frac{V_o(z)}{V_{in}} = -\frac{C_s}{C_f} \times \frac{z^{-1/2}}{1-z^{-1}} 
\]

\( z = e^{j\omega T} \)

\[
= -\frac{C_s}{C_f} \times \frac{e^{-j\omega T/2}}{1-e^{-j\omega T/2}} = \frac{C_s}{C_f} \times \frac{1}{e^{-j\omega T/2} - e^{j\omega T/2}} 
\]

\[
= -\frac{C_s}{C_f} \times \frac{1}{2 \sin(j\omega T/2)} 
\]

\( \sin(j\omega T/2) \)

\[
= \frac{C_s}{C_f} \times \frac{e^{j\omega T/2}}{2 \sin(j\omega T/2)} \]

No Phase Error!
For signals at frequencies << sampling freq. → Magnitude error negligible

Ideal Integrator

Magnitude Error

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Switched-Capacitor Integrator
Parasitic Sensitivity

Effect of parasitic capacitors:
1- $C_{p1}$ - driven by opamp o.k.
2- $C_{p2}$ - at op amp virtual gnd o.k.
3- $C_{p3}$ – Charges to $V_{in}$ & discharges into $C_i$

→ Problem parasitic sensitivity

Parasitic Insensitive
Bottom-Plate Switched-Capacitor Integrator

Sensitive parasitic cap. → $C_{p1}$ → rearrange circuit so that $C_{p1}$ does not charge/discharge

$\phi 1=1$ → $C_{p1}$ grounded

$\phi 2=1$ → $C_{p1}$ at virtual ground
$C_{p2}$ → driven by a low impedance source

Solution: Bottom plate capacitor integrator
Bottom Plate Switched-Capacitor Integrator

Note:
Different delay from Vi+ & Vi- to either output
→ Special attention needed for input/output connections

\[
\begin{array}{c|c|c}
\text{Output/Input} & \text{Vo1} & \text{Vo2} \\
\text{z-Transform} & \text{on } \phi_1 & \text{on } \phi_2 \\
\hline
\text{Vi+ on } \phi_1 & \frac{C_s}{C_t} \frac{z^{-1}}{1-z^{-1}} & \frac{C_s}{C_t} \frac{z^{-1/2}}{1-z^{-1}} \\
\text{Vi- on } \phi_2 & -\frac{C_s}{C_t} \frac{z^{-1/2}}{1-z^{-1}} & -\frac{C_s}{C_t} \frac{1}{1-z^{-1}} \\
\end{array}
\]

Bottom Plate Switched-Capacitor Integrator
z-Transform Model

\[
\begin{array}{c}
\text{Input/Output z-transform} \\
\text{Vo+} & \text{Vo-} \\
\frac{C_s}{C_t} \frac{z^{-1/2}}{1-z^{-1}} & \frac{z^{-1/2}}{1-z^{-1}} \\
\end{array}
\]

LDI
LDI Switched-Capacitor Ladder Filter

Delay around integrator loop is \( \frac{z^{-1/2}}{z^{1/2}} = 1 \) \( \Rightarrow \) LDI function

Effect of Opamp Nonidealities on Switched Capacitor Filter Behaviour

- Opamp finite gain
- Opamp finite bandwidth
- Finite slew rate of the opamp
- Non-linearities associated with opamp output/input characteristics
Effect of Opamp Non-Idealities

Finite DC Gain

\[ H(s) = -f_s \frac{C_s}{C_I} \frac{l}{s + f_s \frac{C_s \times \frac{1}{a}}{a}} \]

\[ H(s) = -\frac{\alpha_b}{s + \alpha_b \times \frac{1}{a}} \]

⇒ \[ Q = a \]

→ Finite DC gain same effect in S.C. filters as for C.T. filters
→ If DC gain not high enough → causes lowing of overall Q & droop in passband

Effect of Opamp Non-Idealities

Finite Opamp Bandwidth

Assumption-

Opamp → does not slew (will be revisited)
Opamp has only one pole → exponential settling

Effect of Opamp Non-Idealities
Finite Opamp Bandwidth

\[ H_{\text{actual}}(Z) = H_{\text{ideal}}(Z) \left[ 1 - e^{-k} + e^{-k} \times \frac{C_f}{C_f + C_s} Z^{-1} \right] \]

where \( k = \pi \times \frac{C_f}{C_f + C_s} \cdot \frac{f_t}{f_s} \)

\( f_t \rightarrow \) Opamp unity-gain frequency, \( f_s \rightarrow \) Clock frequency


Effect of Opamp Finite Bandwidth on Filter Magnitude Response

Example:
For 1dB magnitude response deviation:

1. \( f_c/f_t = 1/12 \)
   \( f_c/f_t = 0.04 \)
   \( f_t > 25f_c \)

2. \( f_c/f_t = 1/32 \)
   \( f_c/f_t = 0.022 \)
   \( f_t > 45f_c \)

3. Cont.-Time
   \( f_c/f_t = 1/700 \)
   \( f_t > 700f_c \)

Active RC

\( f_c/f_t = 1/32 \)
Effect of Opamp Finite Bandwidth on Filter Critical Frequency

Example:
For maximum critical frequency shift of <1%
1. $f_c/f_s = 1/32$
   $f_c/f_s = 0.028$
   $\Rightarrow f_c > 36f_t$
2. $f_c/f_s = 1/12$
   $f_c/f_s = 0.046$
   $\Rightarrow f_c > 22f_t$
3. Active RC
   $f_c/f_s = 0.008$
   $\Rightarrow f_c > 125f_t$


Opamp Bandwidth Requirements for Switched-Capacitor Filters Compared to Continuous-Time Filters

- Finite opamp bandwidth causes phase lag at the unity-gain frequency of the integrator for both type filters
  - Results in negative intg. Q & thus increases overall Q and gain
  - @ results in peaking in the passband of interest

- For given filter requirements, opamp bandwidth requirements much less stringent for S.C. filters compared to cont. time filters
  - lower power dissipation for S.C. filters (at low freq.s only)

- Finite opamp bandwidth causes down shifting of critical frequencies in both type filters
  - Since cont. time filters are usually tuned → tuning accounts for frequency deviation
  - S.C. filters are untuned and thus frequency shift could cause problems specially for narrow-band filters
Sources of Distortion in Switched-Capacitor Filters

- Distortion induced by finite slew rate of the opamp
- Opamp output/input transfer function non-linearity- similar to cont. time filters
- Distortion incurred by finite setting time of the opamp
- Capacitor non-linearity- similar to cont. time filters
- Distortion due to switch clock feed-through and charge injection

What is Slewing?

Assumption:
Integrator opamp is a simple class A transconductance type differential pair with fixed tail current $I_{ss}$
What is Slewing?

| VC| > V_{max} \rightarrow \text{Output current constant } I_o = \pm \frac{I_{ss}}{2} \text{ or } -\frac{I_{ss}}{2} \rightarrow \text{Vo ramps down/up} \rightarrow \text{Slewing}

After Vcs is discharged enough to have:

| VC| < V_{max} \rightarrow I_o = \text{gm} \frac{V_C}{C_s} \rightarrow \text{Exponential or over-shoot settling}

Distortion Induced by Opamp Finite Slew Rate
Ideal Switched-Capacitor Output Waveform

- During phase $\phi_1$, the input $V_{in}$ is connected to the input of the operational amplifier.
- During phase $\phi_2$, the output of the operational amplifier is connected to the capacitor $C_I$.
- Charge is transferred from $C_s$ to $C_I$ during $\phi_2$.

Slew Limited Switched-Capacitor Integrator

- Output slewing & settling:
  - $V_{real}$ and $V_{ideal}$ are the real and ideal output voltages, respectively.
  - $\phi_1$ and $\phi_2$ are the clock phases.
  - The integrator goes through slewing and linear settling periods.

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Distortion Induced by Finite Slew Rate of the Opamp


Distortion Induced by Opamp Finite Slew Rate

• Error due to exponential settling changes linearly with signal amplitude

• Error due to slew-limited settling changes non-linearly with signal amplitude (doubling signal amplitude X4 error)

→ For high-linearity need to have either high slew rate or non-slewing opamp

\[
HD_2 = \frac{V_o}{S_f T_s} \frac{8 (\sin \frac{\alpha T_s}{2})^2}{\pi k (\frac{\alpha}{2} - q)}
\]

\[
\rightarrow HD_3 = \frac{V_o}{S_f T_s} \frac{8 (\sin \frac{\alpha T_s}{2})^2}{15\pi} \quad \text{for} \quad f_0 \gg f_s \quad \rightarrow \quad HD_3 = \frac{8\pi V_o f_o^2}{75 S_f f_s}
\]

Example:
Slew Related Harmonic Distortion

\[ HD_3 = \frac{V_o}{S_r T_s} \frac{8 \sin \alpha_b T_s / 2}{15\pi} \]
\[ HD_3 = \frac{8\pi V_o f_o^2}{15 S_r f_s} \]

Switched-capacitor filter with 4kHz bandwidth, \( f_s = 128kHz \), \( S_r = 1V/\mu sec \), \( V_o = 3V \)


Distortion Induced by Opamp Finite Slew Rate

Example

[Graph showing distortion vs. (slew-rate / f_s) in volts]
Distortion Induced by Finite Slew Rate of the Opamp

- Note that for a high order switched capacitor filter → only the last stage slewing will affect the output linearity (as long as the previous stages settle to the required accuracy)
  - Can reduce slew limited linearity by using an amplifier with a higher slew rate only for the last stage
  - Can reduce slew limited linearity by using class A/B amplifiers
    - Even though the output/input characteristics is non-linear as long as the DC open-loop gain is high, the significantly higher slew rate compared to class A amplifiers helps improve slew rate induced distortion

- In cases where the output is sampled by another sampled data circuit (e.g. an ADC or a S/H) → no issue with the slewing of the output as long as the output settles to the required accuracy & is sampled at the right time

More Realistic Switched-Capacitor Circuit Slew Scenario

At the instant $C_i$ connects to input of opamp ($t=0^+$)
- Opamp not yet active at $t=0^+$ due to finite opamp bandwidth → delay
- Feedforward path from input to output generates a voltage spike at the output with polarity opposite to final $Vo$ step- spike magnitude function of $C_p, C_L, C_i$
- Spike increases slewing period
- Eventually, opamp becomes active - starts slewing followed by subsequent settling
Switched-Capacitor Circuit

Opamp not Active @ \( t=0^+ \)

Charge sharing: \( C_I V_{I_C}^{0+} = V_{I_C}^{0+} (C_s + C_{eq}) \) where \( C_{eq} = \frac{C_I C_L}{C_I + C_L} \)

\[
\Delta V_{out}^{0+} = \frac{C_I}{C_I + C_L} V_{I_C}^{0+} - \frac{C_s}{C_s + C_{eq}} \frac{C_I}{C_I + C_s} \times \frac{C_L}{C_l + C_s} \]

Assuming \( C_L << C_s << C_I \) \( \rightarrow C_{eq} = C_L \rightarrow C_I V_{I_C}^{0+} = V_{I_C}^{0+} (C_s + C_L) \rightarrow V_{I_C}^{0+} = V_{I_C}^{0+} \)

\[
\rightarrow \Delta V_{out}^{0+} = \frac{C_L}{C_s + C_L} \times \frac{C_I}{C_I + C_s} = V_{I_C}^{0+} \]

Note that \( \Delta V_{out}^{0+} = \frac{C_L}{C_I} \frac{V_{I_C}^{0+}}{C_I} = \frac{C_L}{C_I} V_{I_C}^{0+} \)

More Realistic Switched-Capacitor Circuit Slew Scenario

Notice that if \( C_L \) is large \( \rightarrow \) some of the charge stored on \( C_s \) is lost prior to opamp becoming effective \( \rightarrow \) operation loses accuracy

Charge sharing: \( C_s V_{I_C}^{0+} = V_{I_C}^{0+} (C_s + C_{eq}) \) where \( C_{eq} = \frac{C_I C_L}{C_I + C_L} \)

\[
V_{I_C}^{0+} = \frac{C_s}{C_s + C_{eq}} = V_{I_C}^{0+} \frac{C_I C_L}{C_I + C_s} \frac{C_l}{C_s + C_l} \]

\( \rightarrow \) Partly responsible for S.C. filters only good for low-frequency applications
More Realistic S.C. Slew Scenario

Vo_ideal

Vo_real

Vo_real Including t=0+ spike

Slewing Linear Settling

Slewing Linear Settling

Slewing Linear Settling

Spike generated at t=0+


Sources of Noise in Switched-Capacitor Filters

• Opamp Noise
  – Thermal noise
  – 1/f (flicker) noise

• Thermal noise associated with the switching process (kT/C)
  – Same as continuous-time filters

• Precaution regarding aliasing of noise required
Other z domain Integrators

Example: Bilinear

- Bilinear integrator

\[ v_o(nT) = v_o(nT-T) + k \left[ v_i(nT) + v_i(nT-T) \right] \]

\[ \left[ 1 - z^{-1} \right] V_o(z) = k \left[ 1 + z^{-1} \right] V_i(z) \]

\[ H(z) = \frac{V_o(z)}{V_i(z)} = k \frac{1 + z^{-1}}{1 - z^{-1}} \]

Bilinear Integrator

- Not implemented by “standard” SC integrators
- Synthesis:
  Biquads: direct coefficient comparison

Example: Bilinear S.C. integrator:

\[ H(Z) = \frac{C_s}{C_l} \frac{l+Z^{-1}}{l-Z^{-1}} \]
\[ = \frac{C_s}{C_l} \frac{l e^{-j\omega T}}{l - e^{-j\omega T}} \]
\[ = \frac{C_s}{C_l} \frac{l}{j\omega T} \frac{\omega T}{1 + \tan(\omega T)/2} \]

No Phase Error!
For signals at frequency \( \ll \) sampling freq.
\( \rightarrow \) Magnitude error negligible

LDI & Bilinear Transformation
Frequency Warping

**LDI:**
\[
\frac{L}{s} \Rightarrow \frac{Z^{-1/2}}{1-Z^{-1}} = \frac{T_s}{2} j \sin \frac{\omega_T}{2}
\]
\[
s \Rightarrow \frac{2}{T_s} j \sin \frac{\omega_T}{2}
\]

**Bilinear**
\[
\frac{L}{s} \Rightarrow \frac{1+Z^{-1}}{1-Z^{-1}} = \frac{1+e^{-j\omega_T}}{1-e^{-j\omega_T}} = \frac{T_s}{2} j \tan \frac{\omega_T}{2}
\]
\[
s \Rightarrow \frac{2}{T_s} j \tan \frac{\omega_T}{2}
\]

**Other z domain Integrators**

- **Example: Bilinear**

\[
\frac{1}{s} = 2\pi j f_{RC} = H_{SC}(z)|_{z=e^{2\pi j f_{RC} T}}
\]

\[
f_{RC} = \frac{f_s}{\pi} \tan \left( \pi \frac{f_{SC}}{f_s} \right)
\]

\[
f_{SC} = \frac{f_s}{\pi} \sin \left( \pi \frac{f_{SC}}{f_s} \right)
\]
Bilinear Transform

\[ f_{RC} = \frac{f_s}{\pi} \tan \left( \pi \frac{f_{SC}}{f_s} \right) \]

- Entire \( j\omega \) axis maps onto the unit circle
- Mapping is nonlinear (tan distortion) → prewarp specifications of RC prototype
  Matlab filter design automates this (see, e.g. bilinear)

Bilinear & LDI Transformation Frequency Warping

As long as \( f << f_s \), error negligible
“Bilinear” Bandpass

\[ f_s = 100\text{kHz} \]
\[ f_c = \frac{f_s}{8} \]
\[ Q = 10 \]

Matlab:

\[
H(z) = \frac{0.0378 z^2 - 0.0378}{z^2 - 1.362 z + 0.9244}
\]

zero at \( f_s/2 \)

---

Martin-Sedra Biquad

Periodic AC Analysis

Magnitude Response

LDI vs Bilinear Transform

- **LDI transform**:
  - Realized by "standard" switched-capacitor integrators
  - Some high frequency zeros may get lost
  - Simple filter synthesis:
    - Replace RC integrators with SC integrators
    - Ensure clock phases chosen so that all integrators loops LDI type

- **Bilinear transform**
  - Not implemented by "standard" SC integrators
  - Synthesis:
    - Biquads: direct coefficient comparison
Switched-Capacitor Filter Application
Example: Voice-Band Codec (Coder-Decoder) Chip


CODEC Transmit Path
Lowpass Filter Frequency Response

Note: $f_c = 128kHz$
CODEC Transmit Path
Highpass Filter

Note: $f_s = 8$ kHz

Low Q bandpass ($Q < 1$) filter shape → Implemented with lowpass followed by highpass
CODEC Transmit Path
Clocking Scheme

First filter (1st order RC type) performs anti-aliasing for the next S.C. biquad

The first 2 stage filters form 3rd order elliptic with corner frequency @ 32kHz \( \rightarrow \) Anti-aliasing for the next lowpass filter

The stages prior to the high-pass perform anti-aliasing for high-pass

Notice gradual lowering of clock frequency \( \rightarrow \) Ease of anti-aliasing

SC Filter Summary

✓ Pole and zero frequencies proportional to
  – Sampling frequency \( f_s \)
  – Capacitor ratios
    ➢ High accuracy and stability in response
    ➢ Long time constants realizable without large R, C

✓ Compatible with transconductance amplifiers
  – Reduced circuit complexity, power dissipation

✓ Amplifier bandwidth requirements less stringent compared to CT filters (low frequencies only)

-disabled icon Issue: Sampled-data filters \( \rightarrow \) require anti-aliasing prefiltering
Switched-Capacitor Filters versus Continuous-Time Filter Limitations

Considering overall effects:
- Opamp finite unity-gain-bandwidth
- Opamp settling issues
- Opamp finite slew rate
- Clock feedthru
- Switch+ sampling cap. finite time-constant

\[ \text{Magnitude Error} \]

\[ 5-10\text{MHz} \]

\[ \text{Filter bandwidth} \]

\[ \text{Assuming constant opamp } f_u \]

\[ \rightarrow \text{Limited switched-capacitor filter performance frequency range} \]

---

Summary
Filter Performance versus Filter Topology

<table>
<thead>
<tr>
<th></th>
<th>Max. Usable Bandwidth</th>
<th>SNDR</th>
<th>Freq. tolerance w/o tuning</th>
<th>Freq. tolerance + tuning</th>
</tr>
</thead>
<tbody>
<tr>
<td>Opamp-RC</td>
<td>~10MHz</td>
<td>60-90dB</td>
<td>+30-50%</td>
<td>1-5%</td>
</tr>
<tr>
<td>Opamp-MOSFET-C</td>
<td>~5MHz</td>
<td>40-60dB</td>
<td>+30-50%</td>
<td>1-5%</td>
</tr>
<tr>
<td>Opamp-MOSFET-RC</td>
<td>~5MHz</td>
<td>50-90dB</td>
<td>+30-50%</td>
<td>1-5%</td>
</tr>
<tr>
<td>Gm-C</td>
<td>~100MHz</td>
<td>40-70dB</td>
<td>+40-60%</td>
<td>1-5%</td>
</tr>
<tr>
<td>Switched Capacitor</td>
<td>~10MHz</td>
<td>40-90dB</td>
<td>&lt;&lt;1%</td>
<td>--</td>
</tr>
</tbody>
</table>
Data Converters

Material Covered in EE247

Where are We?

✓ Filters
  – Continuous-time filters
    • Biquads & ladder type filters
    • Opamp-RC, Opamp-MOSFET-C, gm-C filters
    • Automatic frequency tuning
  – Switched capacitor (SC) filters

• Data Converters
  – D/A converter architectures
  – A/D converter
    • Nyquist rate ADC- Flash, Pipeline ADCs,…
    • Oversampled converters
    • Self-calibration techniques

• Systems utilizing analog/digital interfaces
Data Converter Topics

- Basic operation of data converters
  - Uniform sampling and reconstruction
  - Uniform amplitude quantization
- Characterization and testing
- Common ADC/DAC architectures
- Selected topics in converter design
  - Practical implementations
  - Desensitization to analog circuit non-idealities
- Figures of merit and performance trends

Suggested Reference Texts


Data Converter Basics

- DSPs benefited from device scaling
- However, real world signals are still analog:
  - Continuous time
  - Continuous amplitude
- DSP can only process:
  - Discrete time
  - Discrete amplitude
  \[\text{Need for data conversion from analog to digital and digital to analog}\]

Converter Applications
A/D & D/A Conversion

Data Converters

- Stand alone data converters
  - Used in variety of systems
  - Example: Analog Devices AD9235 12bit/ 65Ms/s
    ADC- Applications:
      - Ultrasound equipment
      - IF sampling in wireless receivers
      - Various hand-held measurement equipment
      - Low cost digital oscilloscopes
Data Converters

• Embedded data converters
  – Cost, reliability, and performance → Integration of data conversion interfaces along with DSPs
  – Main issues
    • Feasibility of integrating sensitive analog functions in a technology optimized for digital performance
    • Down scaling of supply voltage
    • Interference & spurious signal pick-up from on-chip digital circuitry
    • Portable applications dictate low power consumption

Example: Typical Cell Phone

Contains in integrated form:
• 4 Rx filters
• 4 Tx filters
• 4 Rx ADCs
• 4 Tx DACs
• 3 Auxiliary ADCs
• 8 Auxiliary DACs

Total:
Filters → 8
ADCs → 7
DACs → 12

Dual Standard, I/Q
Audio, Tx/Rx power control, Battery charge control, display, ...
D/A Converter Transfer Characteristics

- For an ideal digital-to-analog converter accepting digital inputs \( b_1 - b_n \) and producing either an analog output voltage or current with:
  - uniform, binary digital encoding & a unipolar output ranging from 0 to \( V_{FS} \)

Nomenclature:

\[ N = \# \text{ of bits} \]
\[ V_{FS} = \text{full scale output} \]
\[ \Delta = \min \text{ step size} \rightarrow \text{LSB} \]
\[ \Delta = \frac{V_{FS}}{2^N} \]
\[ \text{or } N = \log_2 \frac{V_{FS}}{\Delta} \rightarrow \text{resolution} \]

\[ V_0 = V_{FS} \sum_{i=1}^{N} \frac{b_i}{2^i} = \Delta \sum_{i=1}^{N} b_i \times 2^{N-i} , \quad b_i = 0 \text{ or } 1 \]

---

D/A Converter

Example: D/A with 3-bit Resolution

Example: \( N = 3 \)

Assume \( V_{FS} = 0.8V \)

Input code is 101

\[ V_0 = \Delta \left( b_1 \times 2^2 + b_2 \times 2^1 + b_3 \times 2^0 \right) \]

Then: \( \Delta = \frac{V_{FS}}{2^3} = 0.1V \)

\[ \rightarrow V_0 = 0.1V \times (1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0) = \]

\[ \rightarrow V_0 = 0.5V \]

Note: MSB \( \rightarrow \frac{V_{FS}}{2} \) & LSB \( \rightarrow \frac{V_{FS}}{2^N} \)
### Ideal D/A Transfer Characteristic

- **Ideal DAC** introduces no error!
- **One-to-one mapping** from input to output

### A/D Converter Transfer Characteristic

- For an ideal analog-to-digital converter with uniform, binary digital encoding & a unipolar input range for 0 to $V_{FS}$
  - $m = \# \text{ of bits}$
  - $V_{FS} = \text{full scale output}$
  - $\Delta = \text{step size}$
  - $\Delta = \frac{V_{FS}}{2^m}$

**Note:**
- $D(b_1, b_2, b_3, ..., b_m) \rightarrow V_{FS} - \Delta \rightarrow V_{FS} \left(1 - \frac{b}{2^m}\right)$
**Ideal A/D Transfer Characteristic**

- Ideal ADC introduces error
  \[ \pm \frac{1}{2} \Delta \]
  \[ \Delta = \frac{V_{FS}}{2^m} \]
  \( m = \# \text{ of bits} \)

- This error is called "quantization error"

**Data Converter Performance Metrics**

- Data Converters are typically characterized by static, time-domain, & frequency domain performance metrics:
  - Static
    - Monotonicity
    - Offset
    - Gain error
    - Differential nonlinearity (DNL)
    - Integral nonlinearity (INL)
  - Dynamic
    - Delay, settling time
    - Aperture uncertainty
    - Distortion- harmonic content
    - Signal-to-noise ratio (SNR), Signal-to-(noise+distortion) ratio (SNDR)
    - Idle channel noise
    - Dynamic range & spurious-free dynamic range (SFDR)