ADC Converters
• Sampling (continued)
  – Clock boosters (continued)
  – Sampling switch charge injection & clock feedthrough
    • Complementary switch
    • Use of dummy device
    • Bottom-plate switching
  – Track & hold circuits
  – T/H circuit incorporating gain & offset cancellation
• Electro-Static Discharge (ESD) protection

Summary Last Lecture
• DAC Converters (continued)
  – DAC reconstruction filter
• ADC Converters
  – Sampling
    • Sampling network thermal noise
    • Acquisition bandwidth limitations
      – For example 1% accuracy $\Rightarrow T_s/2 > 5RC$
    • Sampling switch induced distortion
      – Sampling switch conductance dependence on input voltage
      – Complementary switch
      – Clock boosters
Boosted Clock Sampling
Complete Circuit

M7 & M13 for reliability

Remaining issues:
- $V_{GS}$ constant only for $V_{in} < V_{out}$
- Nonlinearity due to $V_{th}$ dependence of M11 on body-source voltage


Advanced Clock Boosting Technique

Advanced Clock Boosting Technique

• clk → low
  – Capacitors C1a & C1b → charged to VDD
  – MS → off
  – Hold mode

Advanced Clock Boosting Technique

• clk → high
  – Top plate of C1a & C1b connected to gate of sampling switch
  – Bottom plate of C1a connected to \( V_{IN} \)
  – Bottom plate of C1b connected to \( V_{OUT} \)
  – \( V_{GS} \) & \( V_{GD} \) of MS both @ VDD & ac signal on G of MS → average of \( V_{IN} \) & \( V_{OUT} \)
Advanced Clock Boosting Technique

- Gate tracks average of input and output, reduces effect of I·R drop at high frequencies
- Bulk also tracks signal ⇒ reduced body effect (technology used allows connecting bulk to S)
- Reported measured SFDR = 76.5dB at $f_s=200$MHz


Constant Conductance Switch

Constant Conductance Switch


M2 \rightarrow \text{Constant current} \\
\quad \rightarrow \text{constant } g_{ds}

M1 \rightarrow \text{replica of M2} \\
\quad & \text{same VGS} \\
\quad \text{as M2} \\
\quad \rightarrow \text{M1 also constant } g_{ds}

- Note: Authors report requirement of 280MHz GBW for the opamp for 12bit 50Ms/s ADC
- Also, opamp common-mode compliance for full input range
Switch Off-Mode Feedthrough Cancellation


Practical Sampling

- \( R_{SW} = f(V_i) \) \( \rightarrow \) distortion
- Switch charge injection & clock feedthrough
Sampling Switch Charge Injection & Clock Feedthrough
Switching from Track to Hold

- First assume \( V_i \) is a DC voltage
- When switch turns off \( \rightarrow \) offset voltage induced on \( C_s \)
- Why?

Sampling Switch Charge Injection

MOS xtor operating in triode region
Cross section view

- Channel \( \rightarrow \) distributed RC network formed between G,S, and D
- Channel to substrate junction capacitance \( \rightarrow \) distributed & voltage dependant
- Drain/Source junction capacitors to substrate \( \rightarrow \) voltage dependant
- Over-lap capacitance \( C_{ov} = L_s W x C_{ov} \) associated with G-S & G-D overlap
Switch Charge Injection
Slow Clock

- Slow clock $\rightarrow$ clock fall time $>>$ device speed
  $\rightarrow$ During the period ($t$ to $t_{off}$) current in channel discharges channel charge into low impedance signal source

- Only source of error $\rightarrow$ Clock feedthrough from $C_{ov}$ to $C_s$

Switch Clock Feedthrough
Slow Clock

$$\Delta V = -\frac{C_s}{C_s + C_i}(V_i + V_{th} - V_L)$$

$$V_s = V_G - \Delta V$$

$$V_i = V_{th} + \Delta V$$

$$V_o = V_i$$

where $\epsilon = -\frac{C_s}{C_i}$ : $V_s = -\frac{C_s}{C_i}(V_i - V_L)$
Switch Charge Injection & Clock Feedthrough
Slow Clock - Example

\[ C_{ox} = 0.1 \text{fF} / \mu \text{m} \quad C_{ox} = 9 \text{fF} / \mu \text{m}^2 \quad V_{th} = 0.4 \text{V} \quad V_i = 0 \]

\[ \epsilon = -C_{ox} = 10 \text{fF} / \mu \text{m} = -1\% \]

Allowing \( \epsilon = 1 / 2 \text{LSB} \rightarrow \text{ADC resolution} < 9 \text{bits} \)

\[ V_{toff} = \frac{C_{ox}}{C_g} (V_{ih} - V_i) = -0.4 \text{mV} \]

Switch Charge Injection & Clock Feedthrough
Fast Clock

- Sudden gate voltage drop \( \rightarrow \) no gate voltage to establish current in channel
- \( \rightarrow \) channel charge has no choice but to escape out towards S & D
Switch Charge Injection & Clock Feedthrough

Clock Fall-Time \(<<\) Device Speed:

\[ \Delta V = \frac{C_{so} (V_H - V_L)}{C_{so} + C_s} \cdot \frac{1}{2} \cdot \frac{Q_s}{C_s} \]

\[ V_e = V_{ih} - V_{ih} \]

\[ V_{o} = \frac{1}{2} WC_{s} L (V_{hi} - V_{so}) \]

where:

\[ \epsilon = \frac{1}{2} WC_{s} L (V_{hi} - V_{so}) \]

\[ V_{o} = \frac{1}{2} WC_{s} L (V_{hi} - V_{so}) \]

- For simplicity it is assumed channel charge divided equally between S & D
- Source of error \(\rightarrow\) channel charge transfer + clock feedthrough via \(C_{so}\) to \(C_s\)

Switch Charge Injection & Clock Feedthrough

Fast Clock - Example

\[ C_{so} = 0.1 fF / \mu \quad C_{si} = 9 fF / \mu^2 \quad V_{so} = 0.4V \quad V_{DD} = 1.8V \]

\[ V_{th} = 0 \]

\[ \epsilon = 1.6\% \rightarrow \sim 5 \text{ bits} \]

\[ V_{oi} = \frac{C_{so}}{C_s} (V_H - V_L) \cdot \frac{1}{2} WC_{s} L (V_{hi} - V_{so}) \]

\[ V_{oi} = -1.8mV - 14.6mV = -16.4mV \]
Switch Charge Injection & Clock Feedthrough
Slow Clock versus Fast Clock

Switch Charge Injection & Clock Feedthrough
Example-Summary

Error function of:
- Clock fall time
- Input voltage level
- Source impedance
- Sampling capacitance
- Switch size

Clock fall/rise should be controlled not be faster (sharper) than necessary
Switch Charge Injection Error Reduction

- How do we reduce the error?
  - Reduce switch size?

$$\Delta V_s = -\frac{I_{gs}}{2C_s} \downarrow$$

$$\tau = \frac{W}{2\mu C_s \frac{V_{gs} - V_{th}}{L}} \uparrow \quad \text{(note: } \frac{L}{2} = k\tau)$$

Consider the figure of merit (FOM):

$$FOM = \frac{\mu C_s \frac{W}{L}(V_{gs} - V_{th})}{\tau \times \Delta V_s \times C_s \times W C_s L (V_{th} - V_t - V_{th})}$$

$$\rightarrow FOM = \frac{\mu L}{E}$$

- Reducing switch size increases $\tau \rightarrow$ increased distortion not a viable solution
- Small $\tau$ and small $\Delta V$ use minimum channel length (mandated by technology)
- For a given technology $\tau \times \Delta V \approx$ constant

Sampling Switch Charge Injection & Clock Feedthrough Summary

- Extra charge injected onto sampling capacitor @ switch device turn-off
  - Channel charge injection
  - Clock feedthrough to $C_s$ via $C_{ov}$

- Issues:
  - DC offset
  - Input dependant error voltage $\rightarrow$ distortion

- Solutions:
  - Complementary switch?
  - Addition of dummy switches?
  - Bottom-plate sampling?
Switch Charge Injection
Complementary Switch

- In slow clock case if area of n & p devices widths are equal ($W_n=W_p$) effect of overlap capacitor for n & p devices to first order cancel (cancellation accuracy depends on matching of n & p width and $\Delta L$)
- Since in CMOS technologies $\mu_n \approx 2.5\mu_p$ choice of $W_n=W_p$ not optimal from linearity perspective ($W_p > W_n$ preferable)

Switch Charge Injection
Complementary Switch
Fast Clock

$\Delta V_o = \frac{1}{2} \left( \frac{Q_{b-n}}{C_i} - \frac{Q_{b-p}}{C_i} \right)$

$V_o = V_i (1 + \varepsilon) + V_{os}$

$\varepsilon = \frac{1}{2} \frac{W_n C_{ox} L_n + W_p C_{ox} L_p}{C_i}$

- In fast clock case
  - To 1st order, offset due to overlap caps cancelled for equal device width
  - Input voltage dependant error worse!
Switch Charge Injection
Dummy Switch

\[ Q_1 = \frac{1}{2} Q_{\text{clk}} + Q^{M_1}_{\text{in}} \]
\[ Q_2 = Q^{M_2}_{\text{in}} + 2Q^{M_2}_{\text{in}} \]

For \( W_{M_2} = \frac{1}{2} W_{M_1} \) \( \rightarrow \) \( Q_2 = -Q_1 \)

• Dummy switch same L as main switch but half W
• Main device clock goes low, dummy device gate goes high \( \rightarrow \) dummy switch acquires same amount of channel charge main switch needs to lose
• Effective only if exactly half of the charge transferred to M2 (depends on input/output node impedance) and requires good matching between clock fall/rise
Switch Charge Injection

Dummy Switch

- To guarantee half of charge goes to each side → create the same environment on both sides
  - Add capacitor equal to sampling capacitor to the other side of the switch
  - Add fixed resistor to emulate input resistance of following circuit
- Issues: Degrades sampling bandwidth

Dummy Switch Effectiveness Test

- Dummy switch → $W = 1/2W_{\text{main}}$
- As $V_{\text{in}}$ is increased $V_{c1} - V_{\text{in}}$ is decreased → channel charge decreased → less charge injection
- Note large $L_s$ → good device area matching

Switch Charge Injection

Differential Sampling

\[ V_{o+} = V_{o-} = V_{id} \]
\[ V_{ic} = \frac{V_{o+} + V_{o-}}{2} \]
\[ V_{ic} = V_{i+}(1 + \varepsilon_1) + V_{o+} \]
\[ V_{ic} = V_{i-}(1 + \varepsilon_2) + V_{o-} \]
\[ V_{id} = V_{o+} + V_{o-} \left( \varepsilon_1 + \varepsilon_2 \right) \left( \varepsilon_1 - \varepsilon_2 \right) \]

- To 1st order, offset terms cancel
- Note gain error \( \varepsilon \) still about the same
- Has the advantage of better immunity to noise coupling and cancellation of even order harmonics

Switch Charge Injection

Bottom Plate Sampling

- Switches M2 opened slightly earlier compared to M1
- Injected charge by the opening of M2 is constant & eliminated when used differentially
- Since \( C_s \) bottom plate open when M1 opened \( \rightarrow \) no charge injected on \( C_s \)
Flip-Around Track & Hold

- Concept based on bottom-plate sampling

Flip-Around T/H-Basic Operation

\[ Q_{\phi_1} = V_{IN} \times C \]

Note: Opamp has to be stable in unity-gain configuration
Flip-Around T/H-Basic Operation
\( \phi_2 \rightarrow \text{high} \)

\[ \text{Holding} \]

\[ \phi_1 \]

Flip-Around T/H - Timing

- S1 opens earlier than S1A
- No resistive path from C bottom plate to Gnd → charge can not change
  “Bottom Plate Sampling”
Charge Injection

- At the instant of transitioning from track to hold mode, some of the charge stored in sampling switch S1 is dumped onto C.

- With "Bottom Plate Sampling", only charge injection component due to opening of S1 and is to first-order independent of $v_{IN}$.
  - Only a dc offset is added. This dc offset can be removed with a differential architecture.

Flip-Around T/H

- Constant switch $V_{GS}$ to minimize distortion.

Note: Among all switches only S1A & S2A experience full input voltage swing.
Flip-Around T/H

- S1 is chosen to be an n-channel MOSFET
- Since it always switches the same voltage, its on-resistance, $R_{S1}$, is signal-independent (to first order)
- Choosing $R_{S1} \gg R_{S1A}$ minimizes the non-linear component of $R = R_{S1A} + R_{S1}$
  - $S1A$ is a wide (much lower resistance than S1) & constant $V_{GS}$ switch
  - In practice size of S1A is limited by the (nonlinear) S/D capacitance that also adds distortion
  - If S1A's resistance is negligible $\Rightarrow$ delay depends only on S1 resistance
  - S1 resistance is independent of $V_{IN} \Rightarrow$ error due to finite time-constant $\Rightarrow$ independent of $V_{IN}$

Differential Flip-Around T/H

Offset voltage associated with charge injection of S11 & S12 cancelled by differential nature of the circuit
During input sampling phase $\Rightarrow$ amp outputs shorted together

Differential Flip-Around T/H

- Gain = 1
- Feedback factor = 1

Issues: Input Common-Mode Range

- $\Delta V_{\text{in,cm}} = V_{\text{out,com}} - V_{\text{sig,com}}$
  - Amplifier needs to have large input common-mode compliance
Differential Flip-Around T/H
Choice of Sampling Switch Size

- THD simulated w/o sampling switch boosted clock → -45dB
- THD simulated with sampling switch boosted clock (see figure)

Ref: K. Vleugel et al, “A 2.5-V Sigma–Delta Modulator for Broadband Communications Applications”
IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 36, NO. 12, DECEMBER 2001, pp. 1887

Input Common-Mode Cancellation

- Shorting switches M4, M5 added

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-17, NO. 6, DECEMBER 1982 1008
**Input Common-Mode Cancellation**

- **Track mode (φ high)**
  - $V_{C1} = V_{I1}$, $V_{C2} = V_{I2}$
  - $V_{O1} = V_{O2} = 0$

- **Hold mode (φ low)**
  - $V_{O1} + V_{O2} = 0$
  - $V_{O1} - V_{O2} = -(V_{I1} - V_{I2})(C_1/(C_1 + C_3))$

→ Input common-mode level removed

**T/H + Charge Redistribution Amplifier**

- **Track mode**:
  - $(S1, S3 \rightarrow on \rightarrow S2 \rightarrow off)$
  - $V_{C1} = V_{os} - V_{IN}$, $V_{C2} = 0$
  - $V_{o} = V_{os}$
**T/H + Charge Redistribution Amplifier**

**Hold Mode**

\[ V_{C1} \rightarrow V_{OS} \]
\[ \Delta V_{C1} = V_{os} - (V_{os} - V_{IN}) = V_{IN} \]
\[ \Delta Q_1 = C_1 \Delta V_{C1} = C_1 V_{IN} \]
\[ \Delta Q_2 = C_2 \Delta V_{C2} = \Delta Q_1 \]
\[ \Delta V_{C2} = \left( \frac{C_1}{C_2} \right) V_{C1} = V_{C2} \]

\[ V_O = V_{C2} + V_{os} = \left( \frac{C_1}{C_2} \right) V_{IN} + V_{os} \]

Hold/amplify mode (S1, S3 \( \rightarrow \) off S2 \( \rightarrow \) on)

- Offset NOT cancelled, but not amplified
- Input-referred offset = \( \frac{C_2}{C_1} \times V_{OS} \), & \( C_2 < C_1 \)

---

**T/H & Input Difference Amplifier**

Sample mode (S1, S3 \( \rightarrow \) on S2 \( \rightarrow \) off)

\[ V_{C1} = V_{os} - V_{I1} \quad V_{C2} = 0 \]
\[ V_O = V_{os} \]
Input Difference Amplifier
Cont'd

Subtract/Amplify mode (S1, S3 off, S2 on)
During previous phase:
\[ V_{C1} = V_{os} - V_{I1} , V_{C2} = 0 \]
\[ V_o = V_{os} \]

\[ V_{C1} = V_{os} - V_{I2} \]
\[ \Delta V_{C1} = (V_{os} - V_{I2}) - (V_{os} - V_{I1}) = V_{I1} - V_{I2} \]
\[ \Delta V_{C2} = \left( \frac{C_2}{C_1} \right) \Delta V_{C1} = \left( \frac{C_2}{C_1} \right) (V_{I1} - V_{I2}) \]
\[ V_o = \left( \frac{C_1}{C_2} \right) (V_{I1} - V_{I2}) + V_{os} \]

→ Offset NOT cancelled, but not amplified
→ Input-referred offset = \( \frac{C_2}{C_1} \) \( V_{os} \) & \( C_2 < C_1 \)

T/H & Summing Amplifier
Sample mode (S1, S3, S5 on, S2, S4 off)

\[ V_{C1} = V_{os} - V_{I1}, \quad V_{C2} = V_{os} - V_{I3}, \quad V_{C3} = 0 \]

\[ V_o = V_{os} \]

Amplify mode (S1, S3, S5 off, S2, S4 on)

\[ V_{C1} = V_{os} - V_{I2} \Rightarrow \Delta V_{C1} = V_{I1} - V_{I2} \]
\[ V_{C2} = V_{os} - V_{I4} \Rightarrow \Delta V_{C2} = V_{I3} - V_{I4} \]
\[ \Delta Q_d = \Delta Q_1 + \Delta Q_2 = C_1 \Delta V_{C1} + C_2 \Delta V_{C2} \]
\[ \Delta V_{C2} = \frac{\Delta Q_2}{C_3} = \left( \frac{C_4}{C_1} \right) (V_{I1} - V_{I2}) + \left( \frac{C_5}{C_2} \right) (V_{I3} - V_{I4}) \]
\[ V_o = \frac{C_1}{C_3} (V_{I1} - V_{I2}) + \frac{C_2}{C_3} (V_{I3} - V_{I4}) + V_{os} \]
Differential T/H Combined with Gain Stage

Employs the previously discussed technique to eliminate the problem associated with high common-mode voltage excursion at the input of the opamp.

Differential T/H Combined with Gain Stage

- Gain = 4C/C = 4
- Input voltage common-mode level removed → opamp can have low CMRR
- Amplifier offset NOT removed


Differential T/H Including Offset Cancellation

- Operation during offset cancellation phase shown
- Auxiliary inputs added with A_{main}/A_{aux} = 10
- During offset cancellation phase:
  - Aux. amp configured in unity-gain mode: V_{out} = V_{out^{main}} → offset stored on C_{AZ} & canceled

Differential T/H Including Offset Cancellation
Operational Amplifier

- Operational amplifier →
  dual input folded-cascode opamp
- M3,4 auxiliary input, M1,2 main input
- To achieve 1/10 gain ratio
  \( W_{M3,4} = 1/10 \times W_{M1,2} \) &
  current sources are scaled by 1/10
- M5,6,7 → common-mode control
- Output stage → dual cascode → high DC gain

\[
V_{out} = g_{m1} r_o V_{in1} + g_{m2} r_o V_{in2}
\]


Differential T/H Including Offset Cancellation Phase

- During offset cancellation phase AZ and S1 closed → main amplifier offset amplified by \( g_{m1}/g_{m2} \) & stored on \( C_{AZ} \)
- Auxiliary amp chosen to have lower gain so that:
  - Aux. amp offset & charge injection associated with opening of switch AZ → reduced by \( A_{aux}/A_{main} = 1/10 \)
  - Low increase in power dissipation resulting from addition of aux. inputs
- Requires an extra auto-zero clock phase
ESD Protection

ADC Architectures

What is ESD?

• Electrostatic discharge
• Example: Charge built up on human body while walking on carpet...
• Charged objects near or touching IC pins can discharge through on-chip devices
• Without dedicated protection circuitry, ESD events could be destructive
Model and Protection Circuit

Figure 1. Human Body Model for ESD testing.

[http://www.idt.com/docs/AN_123.pdf]

Equivalent Circuit

- Nonlinear capacitance causes distortion
- Distortion increases with frequency
  - Today's converters: High frequency, low distortion!

ESD Circuit Distortion


\[ C(V_{in}) = 2...4pF \]
for \( V_{in} = 2...0V \)

---

**Analysis:**
- Volterra Series
- Or SPICE simulations

**Example:**

\[ R = 25\Omega \]
\[ C_j = 1pF \]
\[ C_L = 5pF \]
\[ V_{peak} = 0.5V \]
ESD Circuit Distortion

- Distortion from ESD circuits approaches state of-the-art ADC performance!
- If you are working on a new, record breaking ADC, better think about ESD now...
- Solutions still pre-mature
- Lots of company intellectual property! (IP)
ADC Architectures

- Slope Converters
- Successive approximation
- Flash
- Folding
- Time-interleaved / parallel converter
- Residue type ADCs
  - Two-step
  - Pipeline
  - Algorithmic
  - ...
- Oversampled ADCs

Single Slope ADC

- Low complexity
- Hard to generate precise ramp
- Better: Dual Slope, Multi-Slope
Dual Slope ADC

- Integrate $V_{in}$ for fixed time, de-integrate with $V_{ref}$ applied $\Rightarrow T_{De-Int} \sim V_{in}/V_{ref}$
- Insensitive to most linear error sources

Successive Approximation ADC

- Binary search over DAC output

DAC[Input] = ADC[Output]
Successive Approximation ADC

Example: 6-bit ADC & \( V_{IN} = \frac{5}{8} V_{REF} \)

- High accuracy achievable (16+ Bits)
- Moderate speed proportional to \( B \) (MHz range)