ADC Converters (continued)
- Successive approximation ADCs (continued)
- Flash ADC
- Flash ADC sources of error
  • Sparkle code
  • Meta-stability
- Comparator design

Summary of Last Lecture
ADC Converters
- Sampling (continued)
  • Track & hold circuits
  • T/H combined with summing/difference function
  • T/H circuit incorporating gain & offset cancellation
- Electro-Static Discharge (ESD) protection
- ADC architectures
  • Serial- slope type
  • Successive approximation
Successive Approximation ADC

Example: 6-bit ADC & $V_{IN} = 5/8V_{REF}$

- High accuracy achievable (16+ Bits)
- Require $N$ clock cycles for $N$-bit conversion (much faster than slope type)
- Moderate speed proportional to $B$ (MHz range)

Example: SAR ADC
Charge Redistribution Type

- T/H inherent in DAC
- Operation starts by connecting all top plate to gnd and all bottom plates to $V_{IN}$
- To test the MSB all top plate are opened bottom plate of $32C$ connected to $V_{REF}$ & rest of bottom plates connected to ground $\rightarrow$ input to comparator $= -V_{IN} + V_{REF}/2$
- Comparator is strobed to determine the polarity of input signal if - MSB=1 if + MSB=0
- The process continues until all bits are determined
Example: SAR ADC

Charge Redistribution Type

- To 1st order parasitic ($C_p$) insensitive since top plate driven from initial 0 to final 0 by the global negative feedback
- Linearity is a function of accuracy of C ratios
- Possible to add a C ratio calibration cycle (see ref.)


Flash ADC

- B-bit flash ADC:
  - DAC generates all possible $2^B - 1$ levels
  - $2^B - 1$ comparators compare $V_{IN}$ to DAC outputs
  - Comparator output:
    - If $V_{DAC} < V_{IN} \Rightarrow 0$
    - If $V_{DAC} > V_{IN} \Rightarrow 1$
  - Comparator outputs form thermometer code
  - Encoder converts thermometer to binary code
Flash ADC Converter

Example: 3-bit Conversion

<table>
<thead>
<tr>
<th>Encoder</th>
<th>B-bits</th>
</tr>
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<tbody>
<tr>
<td>1</td>
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Flash Converter

- Very fast: only 1 clock cycle per conversion
  - Half cycle \( V_{IN} \) and \( V_{DAC} \) comparison
  - Half cycle \( 2^B - 1 \) to B encoding

- High complexity: \( 2^B - 1 \) comparators

- Input capacitance of \( 2^B - 1 \) comparators connected to the input node:
  - High capacitance at input node
Flash Converter Sources of Error

- Comparator input:
  - Offset
  - Nonlinear input capacitance
  - Kickback noise (disturbs reference)
  - Signal dependent sampling time

- Comparator output:
  - Sparkle codes (… 11101000 …)
  - Metastability

---

Flash Converter Example: 8-bits ADC

- 8-bits → 255 comparators
- $V_{REF} = 1V \rightarrow 1LSB = 4mV$
- DNL < 1/2 LSB → Comparator input referred offset < 2mV
- $2mV = 6\sigma_{offset}$
  $\rightarrow \sigma_{offset} < 0.33mV$
Flash ADC Converter
Example: 8-bits ADC (continued)

\[ I \sigma_{\text{offset}} < 0.33 \text{mV} \]

• Let us assume in the technology used:
  – Offset-per-unit-sqrt(WxL)=\[ \frac{3 \text{[mV}\times\mu]}{\sqrt{W\times L}} = 0.33 \text{mV} \]
    \[ \rightarrow W \times L = 83 \mu^2 \]
  – Issues:
    • Si area quite large
    • Large input capacitance
    • Since depending on input voltage different number of comparator input
      transistors would be on/off- total input capacitance varies as input varies
    \[ \rightarrow \text{Nonlinear input capacitance could give rise to signal distortion particularly at} \]
    \[ \text{high frequencies} \]
  
  Ref: M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS

Trade-offs:

– Allowing larger DNL e.g. 1LSB instead of 0.5LSB:
  • Increases the maximum allowable input-referred offset voltage by a factor of 2
  • Decreases the required device WxL by a factor of 4
  • Reduces the input device area by a factor of 4
  • Reduces the input capacitance by a factor of 4!

– Reducing the ADC resolution by 1-bit
  • Increases the maximum allowable input-referred offset voltage by a factor of 2
  • Decreases the required device WxL by a factor of 4
  • Reduces the input device area by a factor of 4
  • Reduce the input capacitance by a factor of 4

– Add offset cancellation to the comparator and thus decrease the input device area-- could reduce the conversion rate
**Flash Converter**

Maximum Tolerable Comparator Offset versus ADC Resolution

Assumption:

\[ DNL = 0.5 \text{LSB} \]

Note:

Graph shows offset, note that depending on min acceptable yield, the derived offset numbers are associated with \(2\sigma\) to \(6\sigma\) offset voltage.

**Typical Flash Output Encoder**

- Thermometer code → 1-of-n decoding
- Final encoding → NOR ROM
- Ideally, for each code, only one ROM row is activated

Output \(0 0 1 1\)

\[ b_3 \ b_2 \ b_1 \ b_0 \]
Sparkle Codes

Correct Output: 0111

Problem: Two rows are on

Erroneous Output: 1111 → 1/2FS error!

Erroneous 0 (comparator offset?)

VDD

b3 b2 b1 b0

Sparkle Tolerant Encoder

Protects against a single sparkle.

Ref: C. Manglesdorf et al, "A 400-MHz Flash Converter with Error Correction," JSSC February 1990, pp. 997-1002
**Meta-Stability**

Different gates interpret metastable output \( X \) differently

Correct output: 0111

Erroneous output: 1111

Solutions:
- Extra latches following comparator (high power)
- Gray encoding


---

**Gray Encoding**

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<tr>
<th>Thermometer Code</th>
<th>Gray</th>
<th>Binary</th>
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<td>( T_7 )</td>
<td>( G_3 )</td>
<td>( B_3 )</td>
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<td>( T_6 )</td>
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<td>( T_4 )</td>
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\[ G_1 = T_1 \overline{T}_3 + T_5 \overline{T}_7 \]

\[ G_2 = T_2 \overline{T}_6 \]

\[ G_3 = T_4 \]

- Each \( T_i \) affects only one \( G_i \)
- Avoids disagreement of interpretation by multiple gates
- Protects also against sparkles
- Follow Gray encoder by (latch and) binary encoder
Voltage Comparators

![Comparator Diagram]

Play an important role in majority of ADCs
Function: Compare the instantaneous value of two analog signals & generate a digital output voltage based on the sign of the difference:

\[
\begin{align*}
\text{If } V_{i+} - V_{i-} &> 0 \Rightarrow V_{\text{out}} = \text{“1”} \\
\text{If } V_{i+} - V_{i-} &< 0 \Rightarrow V_{\text{out}} = \text{“0”}
\end{align*}
\]

Voltage Comparator Architectures

Comparator architectures
- High gain amplifier with differential analog input & single-ended large swing output
  - Output swing compatible with driving digital logic circuits
  - Open-loop amplification \(\Rightarrow\) no frequency compensation required
  - Precise gain not required
- Latched comparators; in response to a strobe, input stage disabled & digital output stored in a latch till next strobe
  - Two options for implementation:
    - Latch-only comparator
    - Low-gain amplifier + high-sensitivity latch
- Sample-data comparators
  - T/H input
  - Offset cancellation
Comparators w/ High-Gain Amplification

Amplify $V_{in}(\text{min})$ to $V_{DD}$
$V_{in}(\text{min})$ determined by ADC resolution

Example: 12-bit ADC with:
- $V_{FS} = 1.5V \rightarrow 1\text{LSB}=0.36mV$
- $V_{DD}=1.8V$

$\Rightarrow$ For 1.8V output & 0.5LSB precision:

$A_{\text{min}}^\text{Vin} = \frac{1.8V}{0.18mV} = 10,000$

Comparators
1-Single-Stage Amplification

$f_o = \text{unity-gain frequency, } f_o = -3dB \text{ frequency}$

$f_o = \frac{f_o}{A_v}$

Example: $f_o = 1GHz$ & $A_v = 10,000$

$f_o = \frac{1GHz}{10,000} = 100kHz$

$\tau_{\text{setting}} = \frac{1}{2\pi f_o} = 1.6\mu\text{sec}$

Allow a few $\tau$ for output to settle

$\frac{f_{\text{Max}}}{f_{\text{Clock}}} \rightarrow 5 \tau_{\text{setting}} = 126kHz$

Too slow!

$\Rightarrow$ Try cascade of lower gain stages to broadband response
Comparators
2- Cascade of Open Loop Amplifiers

The stages identical $\rightarrow$ small-signal model for the cascades:

One stage:

$|A_v(0)| = g_m R_L$

$\omega_c = -3\text{dB frequency} = \frac{1}{R_L C_T}$

$\omega_u = -\text{unity gain frequency} = G \cdot BW = \frac{g_m}{C_T}$

$\omega_d = \frac{\omega_a}{|A_v(0)|}$

Open Loop Cascade of Amplifiers

For an N-stage cascade:

$A_T(z) = |A_v(0)|^N = \left|\frac{A_v(0)}{1 + \frac{1}{C_T}}\right|^{1/N}$

Define $\omega_{oN} = -3$dB frequency of the N-stage cascade

Then

$|A_T\left(\omega_{oN}\right)| = \left|\frac{A_v(0)}{\sqrt{2}}\right|^N$

and

$\omega_{oN} = \omega_{o1} \frac{2^{N-1}}{2-1} = \frac{\omega_{o1}}{|A_v(0)|^{1/2}} \frac{2^{N-1}}{2-1}$

For a specified $|A_v(0)|$

$|A_v(0)| = \left|\frac{A_T(0)}{1^{1/N}}\right|^{1/N}$

$\Rightarrow \omega_{oN} = \frac{\omega_{o1}}{|A_v(0)|^{1/2}} \frac{2^{N-1}}{2-1}$

Thus,

$\frac{\omega_{oN}}{\omega_{o1}} = \left[\frac{\omega_{o1}}{|A_T(0)|^{1/2}} \frac{2^{N-1}}{2-1}\right] \left[\frac{\omega_{o1}}{|A_T(0)|^{1/2}} \frac{2^{N-1}}{2-1}\right]^{-1}$

$= \left|\frac{A_T(0)}{1^{1/N}}\right| \frac{2^{N-1}}{2-1}$
Open Loop Cascade of Amplifiers

For $|A_f(0)|=10,000$

| N  | $\omega_{on}/\omega_0$ | $|A_f(0)|$ |
|-----|------------------------|----------|
| 1   | 1                      | 10,000   |
| 2   | 64                     | 100      |
| 3   | 236                    | 21.5     |
| 4   | 435                    | 10       |
| 5   | 611                    | 6.3      |
| 10  | 1067                   | 2.5      |
| 20  | 1185                   | 1.6      |

Example:

$N=3, \quad f_o = 1 \text{GHz} \quad & \quad |A_f(0)|=10000$

$f_{o,N} = \frac{1 \text{GHz}}{(10,000)^{2/3}} \sqrt{2^{1/3} - 1} = 23.7 \text{MHz}$

$\tau_{setting} = \frac{1}{2\pi f_o} = 7 \text{nsec}$

Allow a few $\tau$ for output to settle

$f_{Clock} \rightarrow \frac{1}{5\tau_{setting}} = 29 \text{MHz}$

$f_{max}$ improved from 126kHz to 29MHz $\rightarrow x225$

---

Open Loop Cascade of Amplifiers

Offset Voltage

- From offset point of view high gain/stage is preferred

- Choice of # of stage $\rightarrow$ bandwidth vs offset tradeoff
Open Loop Cascade of Amplifiers
Step Response

- Assuming linear behavior

\[ v_{o1} = \frac{1}{C} \int_{0}^{t} g_m v_{in} \, dt = \frac{g_m}{C} v_{in} t \]

\[ v_{o2} = \frac{1}{C} \int_{0}^{t} g_m v_{o1} \, dt = \frac{g_m}{C} \left( \frac{1}{2} \right) \left( \frac{g_m}{C} \right) v_{in} t^2 \]

\[ v_{o3} = \frac{1}{C} \int_{0}^{t} g_m v_{o2} \, dt = \frac{g_m}{C} \left( \frac{1}{3} \right) \left( \frac{1}{2} \right) \left( \frac{g_m}{C} \right) v_{in} t^3 \]

---

N Stages

\[ v_{ON} = \left( \frac{g_m}{C} \right)^{N} \left( \frac{N!}{N!} \right) v_{in} \]

For the output to reach a specified \( v_{out} \) (i.e., \( v_{ON} = v_{out} \)) the delay is

\[ \tau_D = \left( \frac{C}{g_m} \right)^{1/N} \left( \frac{v_{out}}{v_{in}} \right)^{1/N} \]
Open Loop Cascade of Amplifiers

Delay/(C/gm)

- Minimum total delay broad function of N
- Relationship between # of stages that minimize delay ($N_{opt}$) and gain ($V_{out}/V_{in}$) approximately:

$$N_{opt} = \begin{cases} 1 + \log_2 A_T & \text{for } A < 1000 \\ 1.2 \ln A_T & \text{for } A \geq 1000 \end{cases}$$


Offset Cancellation

- In sampled-data cascade of amplifiers $V_{os}$ can be cancelled
  - Store on ac-coupling caps in series with amp stages
- Offset associated with a specific amp can be cancelled by storing it in series with either the input or the output of that stage
- Offset can be cancelled by adding a pair of auxiliary inputs to the amplifier and storing the offset on capacitors connected to the aux. inputs during offset cancellation phase

Offset Cancellation
Output Series Cancellation

- Amp modeled as ideal
  + $V_{os}$ (input referred)

- Store offset:
  - S1, S4 $\rightarrow$ open
  - S2, S3 $\rightarrow$ closed
    $\Rightarrow V_C = AV_{os}$


Offset Cancellation
Output Series Cancellation

Amplify:
- S1, S4 $\rightarrow$ closed
- S2, S3 $\rightarrow$ open
  $\Rightarrow V_C = AV_{os}$

Circuit requirements:
- Amp not saturate during offset storage
- High-impedance (C) load $\Rightarrow C_c$ not discharged
- $C_c >> C_L$ to avoid attenuation
- $C_c >> C_{switch}$ offset due to charge injection
Offset Cancellation
Cascaded Output Series Cancellation

1- $S_1$ open, $S_2, 3, 4, 5$ closed

$V_{C1} = A_1 x V_{os1}$
$V_{C2} = A_2 x V_{os2}$
$V_{C3} = A_3 x V_{os3}$
Offset Cancellation
Cascaded Output Series Cancellation

2- S3 \rightarrow \text{open}
- Feedthrough from S3 \rightarrow \text{offset on X}
- Switch offset, \( \varepsilon_2 \) induced on node X
- Since S4 remains closed, offset associated with \( \varepsilon_2 \) \rightarrow \text{stored on C2}

\[ V_x = \varepsilon_2 \]
\[ V_{C1} = A_1 \times V_{os1} - \varepsilon_2 \]
\[ V_{C2} = A_2 \times (V_{os2} + \varepsilon_2) \]

3- S4 \rightarrow \text{open}
- Feedthrough from S4 \rightarrow \text{offset on Y}
- Switch offset, \( \varepsilon_3 \) induces error on node Y
- Since S5 remains closed, offset associated with \( \varepsilon_3 \) \rightarrow \text{stored on C3}

\[ V_y = \varepsilon_3 \]
\[ V_{C2} = A_2 \times (V_{os2} + \varepsilon_2) - \varepsilon_3 \]
\[ V_{C3} = A_3 \times (V_{os3} + \varepsilon_3) \]
Offset Cancellation
Cascaded Output Series Cancellation

4. S2 $\rightarrow$ open, S1 $\rightarrow$ closed, S5 $\rightarrow$ open
   - S1 closed & S2 open $\rightarrow$ since input connected to low impedance source
     charge injection not of major concern
   - Switch offset, $\varepsilon_4$ introduced due to S5 opening

\[
V_X = A_1 (V_{in} + V_{os1}) - V_{c1}
= A_1 (V_{in} + V_{os1}) - (A_1 V_{os1} - \varepsilon_2)
= A_1 V_{in} + \varepsilon_2
\]

\[
V_Y = A_2 (V_X + V_{os2}) - V_{c2}
= A_2 (A_1 V_{in} + \varepsilon_2 + V_{os2}) - \left[A_2 (V_{os2} + \varepsilon_2) - \varepsilon_3\right]
= A_1 A_2 V_{in} + \varepsilon_3
\]

\[
V_{out} = A_3 (V_Y + V_{os3}) - V_{c3}
= A_3 (A_1 A_2 V_{in} + \varepsilon_3 + V_{os3}) - \left[A_3 (V_{os3} + \varepsilon_3) - \varepsilon_4\right]
= A_1 A_2 A_3 V_{in} + \varepsilon_4
\]
Offset Cancellation
Cascaded Output Series Cancellation

\[ V_{\text{out}} = A_1 \cdot A_2 \cdot A_3 \left( V_{\text{in}} + \frac{e_2}{A_1 \cdot A_2 \cdot A_3} \right) \]

Input-Refereed Offset = \( \frac{e_2}{A_1 \cdot A_2 \cdot A_3} \)

Example:
3-stage open-loop differential amplifier with offset cancellation + output amplifier (see ref.)

\[ A_{\text{Total(DC)}} = 2 \times 10^6 = 120\text{dB} \]
\[ \text{Input-referred offset} < 5\mu V \]


Offset Cancellation
Output Series Cancellation

• Advantages:
  – Complete cancellation
  – Closed-loop stability not required

• Disadvantages:
  – Gain per stage must be small
  – Offset storage C in the signal path- could slow down overall performance
**Offset Cancellation**

**Input Series Cancellation**


---

**Offset Cancellation**

**Input Series Cancellation**

Store offset

\[ S1 = 0 \text{ (off)} \]
\[ S2, S3 = 1 \text{ (conducting)} \]

\[ V_C = -A(V_C - V_{os}) \]

Note: Mandates closed-loop stability

Offset Cancellation
Input Series Cancellation

Amplify

\[
S2, S3 \rightarrow \text{open} \\
S1 \rightarrow \text{closed}
\]

\[
V_{out} = -A(V_{in} + V_C - V_{os}) = -A\left[ V_{in} + V_{os} \left( \frac{A}{A+1} - 1 \right) \right]
\]

\[
\therefore V_{out} = -A\left( V_{in} - \frac{V_{os}}{A+1} \right)
\]

and

Input-Referred Offset = \[ \frac{V_{os}}{A+1} \]

Offset Cancellation
Cascaded Input Series Cancellation

\[
V_{out} = A_1A_2 \left[ V_{in} - \frac{V_{os2}}{A_1(A_2+1)} \right] \frac{\varepsilon_2}{A_1}
\]

Input-Referred Offset = \[ \frac{V_{os2}}{A_1(A_2+1)} \frac{\varepsilon_2}{A_1} \]

\[ \varepsilon_2 \rightarrow \text{charge injection associated with} \]
\[ \text{opening of S4} \]
Offset Cancellation
Input Series Cancellation

• Advantages:
  – In applications such as C-array successive approximation ADCs can use C-array to store offset

• Disadvantages:
  – Cancellation not complete
  – Requires closed loop stability
  – Offset storage C in the signal path- could slow down overall performance

CMOS Comparators
Cascade of Gain Stages

Fully differential gain stages → 1st order cancellation of switch feedthrough offset

1-Output series offset cancellation

2- Input series offset cancellation
CMOS Comparators
Cascade of Gain Stages

3-Combined input & output series offset cancellation

Offset Cancellation

• Cancel offset by additional pair of inputs (Lecture 20 slide 16 & 17)
Latched Comparators

Compares two input voltages at time $t_x$ & generates a digital output:

- If $V_{i+} - V_{i-} > 0 \rightarrow V_{out} = \text{"1"}$
- If $V_{i+} - V_{i-} < 0 \rightarrow V_{out} = \text{"0"}$

CMOS Latched Comparators

Comparator amplification need not be linear
$\rightarrow$ can use a latch $\rightarrow$ regeneration

Latch $\rightarrow$ Amplification + positive feedback
CMOS Latched Comparators
Small Signal Model

Latch can be modeled as:

→ Single-pole amp + positive feedback

Small signal ac half circuit

CMOS Latched Comparator
Latch Delay

\[
g_a V = \frac{V}{R_i} + C \frac{dV}{dt}
\]

\[
\frac{g_a}{C} \left(1 - \frac{1}{g_m R_L} \right) V = \frac{dV}{dt}
\]

Integrating both sides:

\[
\frac{g_a}{C} \left(1 - \frac{1}{g_m R_L} \right) \int_{t_i}^{t_f} dt = \int_{V_i}^{V_f} \frac{1}{V} dV
\]

Latch Delay:

\[
t_h = t_f - t_i = C \left(1 - \frac{1}{g_m R_L} \right) \ln \left( \frac{V_f}{V_i} \right)
\]

For \(g_m R_L >> 1\)

\[
t_h = \frac{C}{g_m} \ln \left( \frac{V_f}{V_i} \right)
\]
CMOS Latched Comparators

\[ t_d \approx \frac{C}{g_m} \ln \left( \frac{V_2}{V_1} \right) \]

\[ \frac{V_2}{V_1} \rightarrow \text{Latch Gain} = A_L \]

\[ \rightarrow t_d \approx \frac{C}{g_m} \ln A_L \]

<table>
<thead>
<tr>
<th>( A_L )</th>
<th>( \frac{t_d}{C/g_m} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>2.3</td>
</tr>
<tr>
<td>100</td>
<td>4.6</td>
</tr>
<tr>
<td>1000</td>
<td>6.9</td>
</tr>
<tr>
<td>10K</td>
<td>9.2</td>
</tr>
</tbody>
</table>

Compared to a 3-stage open-loop cascade of amps for equal overall gain of 1000

\( \rightarrow \) Latch faster by about x3

Latch-Only Comparator

- Main problem associated with latch-only comparator topology:
  - High input-referred offset voltage (as high as 100mV!)
- Solution:
  - Use preamplifier to amplify the signal and reduce overall input-referred offset
Latch offset attenuated by preamp gain when referred to preamp input.

Assuming the two offset sources are uncorrelated:

\[ \sigma_{\text{Input-Ref. Offset}} = \sqrt{\sigma_{\text{Vos Preamp}}^2 + \frac{1}{A_{\text{Preamp}}} \sigma_{\text{Vos Latch}}^2} \]

**Example:**
- \( \sigma_{\text{Vos Preamp}} = 4\text{mV} \)
- \( \sigma_{\text{Vos Latch}} = 50\text{mV} \)
- \( A_{\text{Preamp}} = 10 \)

\[ \sigma_{\text{Input-Ref. Offset}} = \sqrt{4^2 + \frac{1}{10^2} 50^2} = 6.4\text{mV} \]

---

**Pre-Amplifier Tradeoffs**

- Example:
  - Latch offset: 50 to 100mV
  - Preamp DC gain: 10X
  - Preamp input-referred latch offset: 5 to 10mV
  - Input-referred preamplifier offset: 2 to 10mV
  - Overall input-referred offset: 5.5 to 14mV

\[ \Rightarrow \text{Addition of preamp reduces the latch input-referred offset reduced by } \sim 7 \text{ to } 9X \Rightarrow \sim \text{extra 3-bit resolution!} \]
Comparator Preamplifier Gain-Speed Tradeoffs

- Amplifier maximum Gain-Bandwidth product \((f_u)\) for a given technology, typically a function of maximum device \(f_t\)

\[
f_u = f_0 = \frac{f_s}{A_{\text{preamp}}} = 3dB \text{ frequency } \quad \tau_0 = \text{settling time}
\]

For example assuming preamp has a gain of 10:

\[
f_0 = \frac{f_s}{10} = \frac{1GHz}{10} = 100MHz
\]

\[
\tau_0 = \frac{1}{2\pi f_0} = 1.6\text{ sec}
\]

→ Tradeoff:
- To reduce the effect of latch offset → high preamp gain desirable
- Fast comparator → low preamp gain

Latched Comparator

Important features:
- Maximum clock rate \(f_s\) → settling time, slew rate, small signal bandwidth
- Resolution → gain, offset
- Overdrive recovery
- Input capacitance (and linearity of input capacitance!)
- Power dissipation
- Input common-mode range and CMR
- Kickback noise
- ...
Comparators Overdrive Recovery

Linear model for a single-pole amplifier:

$U \rightarrow$ amplification after time $t_a$

During reset amplifier settles exponentially to its zero input condition with $t_0 = RC$

Assume $V_m \rightarrow$ maximum input normalized to $1/2\text{lsb} (=1)$

Example: Worst case input/output waveforms

Previous input $\rightarrow$ max. possible e.g. VFS

Current input $\rightarrow$ min. input-referred signal $(0.5\text{LSB})$

If recovery is not high enough to allow output to discharge (recover) from previous state- then it may not be able to resolve the current input $\rightarrow$ error

To minimize this effect:
1. Passive clamp
2. Active restore
3. Low gain/stage
Comparators Overdrive Recovery
Limiting Output

Clamp
Adds parasitic capacitance

Active Restore
After outputs are latched → Activate $\phi_R$ & equalize output nodes

CMOS Latched Comparator Delay
Including Preamplifier

Latch delay found previously:

$$\tau_D = \frac{C}{g_m} \ln \left( \frac{V_2}{V_1} \right)$$

Assuming gain of $A_c$ for the preamplifier:

$$\tau_D = \frac{C}{g_m} \ln \left( A_c \frac{V_0}{V_m} \right)$$
Latched Comparator Including Preamplifier Example

Preamplifier gain:
\[ A_c = \frac{g_{m3}^{M3}}{g_{m3}^{M7}} \left( \frac{V_{GS}^{M3} - V_{th}^{M1}}{V_{GS}^{M1} - V_{th}^{M1}} \right) \]

Comparator delay:
\[ \tau_d = C \ln \left( A \frac{V_o}{V_{in}} \right) \]

Comparator Dynamic Behavior

 Comparator Reset Comparator Decision

\( V_{\text{OUT}} \)

\( \tau_{\text{delay}} \)

\( T_{\text{CLK}} \)
Comparator Resolution

\[ \Delta t = \left( \frac{g_m}{C} \right) \ln\left( \frac{V_{in1}}{V_{in2}} \right) \]

Comparator Voltage Transfer Function

Non-Idealities

- Comparator offset voltage
- Meta-Stable region (output ambiguous)
CMOS Comparator Example

- Flash ADC: 8 bits, ±1/2LSB INL @ fs=15MHz (Vref=3.8V, LSB~15mV)
- No offset cancellation


Comparator with Auto-Zero

Flash ADC Comparator with Auto-Zero

\[ V_{C+} - V_{C-} = (V_{Ref+} - V_{Ref-}) - V_{offset} \]


\[ V_i = A_{i1} \cdot A_{i2} \cdot [V_{in+} - V_{in-}] - (V_{C+} - V_{C-}) - V_{offset} \]

Substituting for \((V_{C+} - V_{C-})\) from previous cycle:

\[ V_i = A_{i1} \cdot A_{i2} \cdot [V_{in+} - V_{in-}] - (V_{Ref+} - V_{Ref-}) \]

Note: Offset is cancelled & difference between input & reference established