EE247
Lecture 25

Pipelined ADCs (continued)
- How many bits per stage?

– Algorithmic ADCs utilizing pipeline structure
– Advanced background calibration techniques

Oversampled ADCs
– Why oversampling?
– Pulse-count modulation
– Sigma-delta modulation
- 1-Bit quantization
- Quantization error (noise) spectrum
- SQNR analysis
- Limit cycle oscillations

Summary Last Lecture

Pipelined ADCs (continued)
– Effect gain stage, sub-DAC non-idealities on overall ADC performance
- Digital calibration (continued)
- Correction for inter-stage gain nonlinearity

– Implementation
- Practical circuits
- Combining the digital bits
- Stage implementation
  – Circuits
  – Noise budgeting

How Many Bits Per Stage?

- Many possible architectures
  - E.g. B_{1eff}=3, B_{2eff}=1, ...
    vs. B_{1eff}=1, B_{2eff}=1, B_{3eff}=1, ...
- Complex optimization problem, fortunately optimum tends to be shallow...
- Qualitative answer:
  - Maximum speed for given technology
    - Use small resolution-per-stage (large feedback factor)
  - Maximum power efficiency for fixed, "low" speed
    - Try higher resolution stages
    - Can help alleviate matching & noise requirements in stages following the 1st stage
      Ref: Singer VLSI 96, Yang, JSSC 12/01

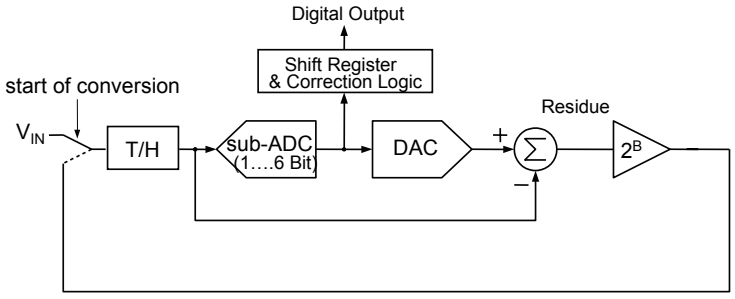
14 & 12-Bit State-of-the-Art Implementations

Reference	Yang (JSSC 12/2001) 0.35µ/3V	Loloee (ESSIRC 2002) 0.18µ/3V
Bits	14	12
Architecture	3-1-1-1-1-1-1-1-1-3	1-1-1-1-1-1-1-1-1-1-2
SNR/SFDR	~73dB/88dB	~66dB/75dB
Speed	75MS/s	80MS/s
Power	340mW	260mW

10 & 8-Bit State-of-the-Art Implementations

Reference	Yoshioko et al (ISSCC 2005) 0.18μ/1.8V	Kim et al (ISSCC 2005) 0.18μ/1.8V
Bits	10	8
Architecture	1.5bit/stage	2.8 -2.8 - 4
SNR/SFDR	~55dB/66dB	~48dB/56dB
Speed	125MS/s	200MS/s
Power	40mW	30mW

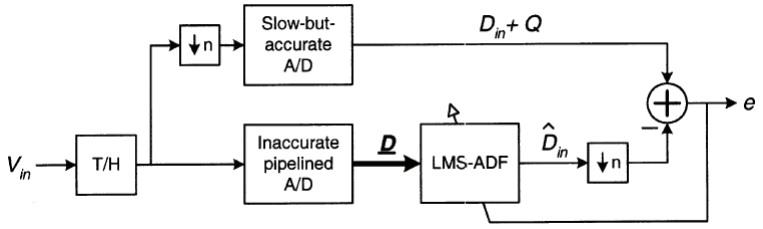
Algorithmic ADC



- Essentially same as pipeline, but a single stage is reused for all partial conversions
- For overall $B_{overall}$ bits → need $B_{overall}/B_{stage}$ clock cycles per conversion

  → Small area, slow

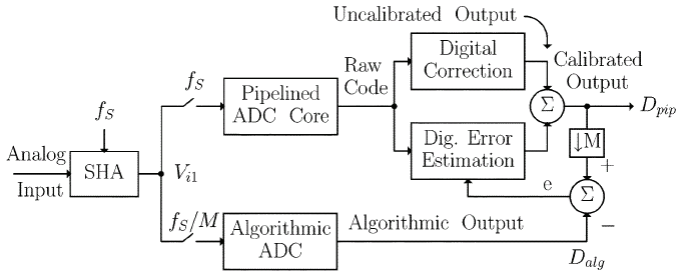
Least Mean Square Adaptive Digital Background Calibration of Pipelined Analog-to-Digital Converters



- Slow, but accurate ADC operates in parallel with pipelined (main) ADC
- Slow ADC samples input signal at a lower sampling rate (f_s/n)
- Difference between corresponding samples for two ADCs (e) used to correct fast ADC digital output via an adaptive digital filter (ADF) based on minimizing the Least-Mean-Squared error

Ref: Y. Chiu, *et al,* "Least Mean Square Adaptive Digital Background Calibration of Pipelined Analog-to-Digital Converters," IEEE TRANS. CAS, VOL. 51, NO. 1, JANUARY 2004

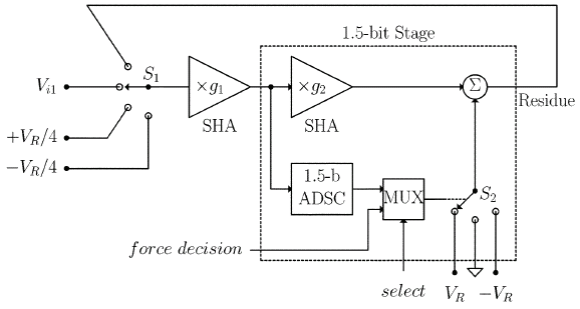
Example: "A 12-bit 20-MS/s pipelined analog-to-digital converter with nested digital background calibration"



- Pipelined ADC operates at 20Ms/s @ has 1.5bit/stage
- Slow ADC → Algorithmic type operating at 20Ms/32=625ks/s
- Digital correction accounts for bit redundancy
- Digital error estimator → minimizes the mean-squared-error

Ref: X. Wang, P. J. Hurst, S. H. Lewis, " A 12-bit 20-Msample/s pipelined analog-to-digital converter with nested digital background calibration", IEEE JSSC, vol. 39, pp. 1799 - 1808, Nov. 2004

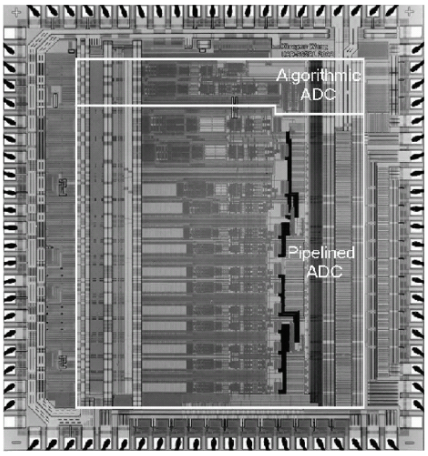
Algorithmic ADC Used for Calibration of Pipelined ADC (continued from previous page)



- Uses replica of pipelined ADC stage
- Requires extra SHA in front to hold residue
- Undergoes a calibration cycle periodically prior to being used to calibrate pipelined ADC

Ref: X. Wang, P. J. Hurst, S. H. Lewis, " A 12-bit 20-MS/s pipelined analog-to-digital converter with nested digital background calibration", IEEE JSSC, vol. 39, pp. 1799 - 1808, Nov. 2004

12-bit 20-MS/s Pipelined ADC with Digital Background Calibration

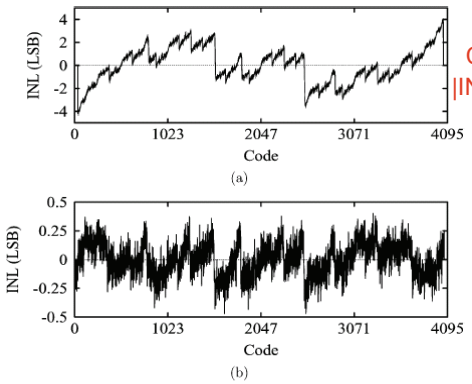


Sampling capacitors scaled:
- Input SHA: 6pF
- Pipelined ADC: 2pF,0.9,0.4,0.2, 0.1,0.1…
- Algorithmic ADC: 0.2pF

Chip area: 13.2mm^2
- Area of Algorithmic ADC <20%
- Does not include digital calibration circuitry estimated ~1.7mm^2

Ref: X. Wang, P. J. Hurst, S. H. Lewis, " A 12-bit 20-MS/s pipelined analog-to-digital converter with nested digital background calibration", IEEE JSSC, vol. 39, pp. 1799 - 1808, Nov. 2004

Measurement Results
12-bit 20-MS/s Pipelined ADC with Digital Background Calibration

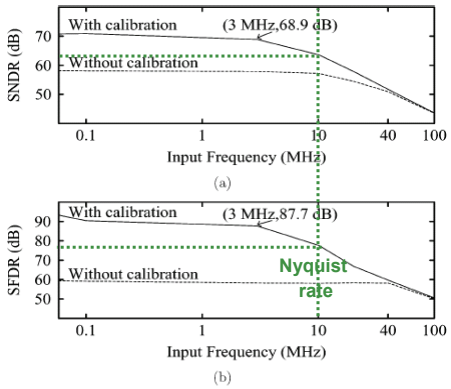


Without Calibration |INL|<4.2LSB

With Calibration |INL|<0.5LSB

Ref: X. Wang, P. J. Hurst, S. H. Lewis, " A 12-bit 20-MS/s pipelined analog-to-digital converter with nested digital background calibration", IEEE JSSC, vol. 39, pp. 1799 - 1808, Nov. 2004

Measurement Results
12-bit 20-MS/s Pipelined ADC with Digital Background Calibration



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Measurement Results

12-bit 20-MS/s Pipelined ADC with Digital Background Calibration

PERFORMANCE SUMMARY (3.3 V, 25 °C)

Process	0.35μm 2P4M CMOS	
Sampling rate	20 Msample/s	
Active area	7.5 mm^2	
Full-Scale Input	1.6 Vp-p	
	Without Cal.	With Cal.
Analog Power Diss.	190 mW	226 mW
Total Power Diss.	217 mW	254 mW
Max. |INL| (Pip. ADC)*	4.21 LSB	0.47 LSB
Max. |DNL| (Pip. ADC)*	0.60 LSB	0.41 LSB
SNDR (Alg. ADC)*	49.6 dB	59.6 dB
SNDR (Pip. ADC)*	58.2 dB	70.8 dB
SFDR (Pip. ADC)*	59.4 dB	93.3 dB
THD (Pip. ADC) *	–59.4 dB	–92.9 dB
PSRR*	65.0 dB	64.8 dB
CMRR*	73.6 dB	73.4 dB

*f_{in}=58 kHz

Does not include digital calibration circuitry estimated ~1.7mm²

Alg. ADC SNDR dominated by noise

Ref: X. Wang, P. J. Hurst, *S.* H. Lewis, " A 12-bit 20-MS/s pipelined analog-to-digital converter with nested digital background calibration", IEEE JSSC, vol. 39, pp. 1799 - 1808, Nov. 2004

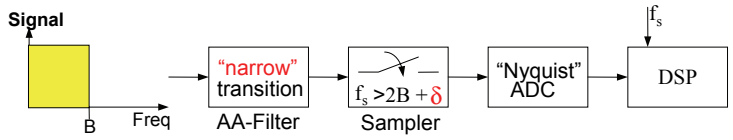
Oversampled ADCs

Analog-to-Digital Converters

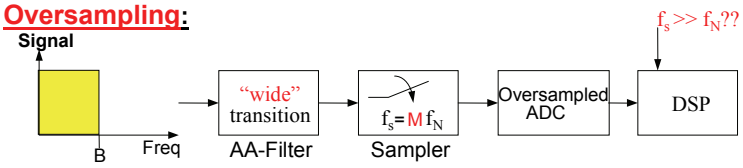
- Two categories:
  - Nyquist rate ADCs → $f_{sig}^{max} \sim 0.5 x f_{sampling}$
    - Maximum achievable signal bandwidth higher compared to oversampled type
    - Resolution limited to max. 12-14bits
  - Oversampled ADCs → $f_{sig}^{max} << 0.5 x f_{sampling}$
    - Maximum possible signal bandwidth lower compared to nyquist
    - Maximum achievable resolution high (18 to 20bits!)

The Case for Oversampling

Nyquist sampling:

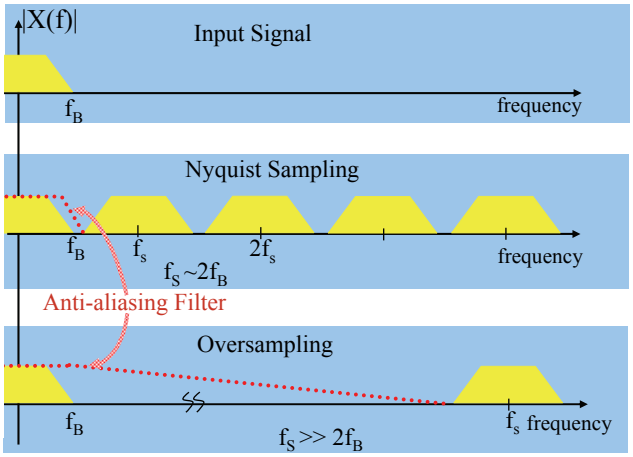


Oversampling:



- Nyquist rate $f_N = 2B$
- Oversampling rate $M = f_s/f_N >> 1$

Nyquist v.s. Oversampled Converters Antialiasing

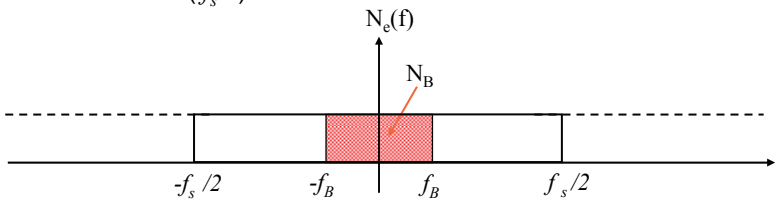


Oversampling Benefits

- No stringent requirements imposed on analog building blocks
- Takes advantage of the availability of low cost, low power digital filtering
- Relaxed transition band requirements for analog anti-aliasing filters
- Reduced baseband quantization noise power
- Allows trading speed for resolution

ADC Converters
Baseband Noise

- For a quantizer with step size Δ and sampling rate f_s:
  - Quantization noise power distributed uniformly across Nyquist bandwidth ($f_s/2$)



  - Power spectral density:

$$N_e(f) = \frac{\overline{e^2}}{f_s} = \left(\frac{\Delta^2}{12}\right)\frac{1}{f_s}$$

  - Noise is distributed over the Nyquist band $-f_s/2$ *to* $f_s/2$

Oversampled Converters
Baseband Noise

$$S_B = \int_{-f_B}^{f_B} N_e(f)\,df = \int_{-f_B}^{f_B} \left(\frac{\Delta^2}{12}\right)\frac{1}{f_s}\,df$$

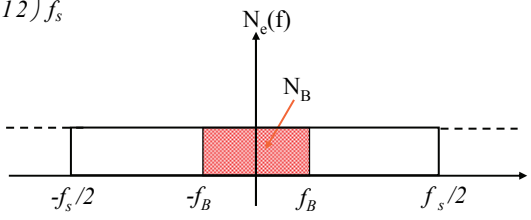
$$= \frac{\Delta^2}{12}\left(\frac{2f_B}{f_s}\right)$$

where for $f_B = f_s/2$

$$S_{B0} = \frac{\Delta^2}{12}$$

$$S_B = S_{B0}\left(\frac{2f_B}{f_s}\right) = \frac{S_{B0}}{M}$$

$$\text{where } M = \frac{f_s}{2f_B} = \textit{oversampling ratio}$$



Oversampled Converters
Baseband Noise

$$S_B = S_{B0}\left(\frac{2f_B}{f_s}\right) = \frac{S_{B0}}{M}$$

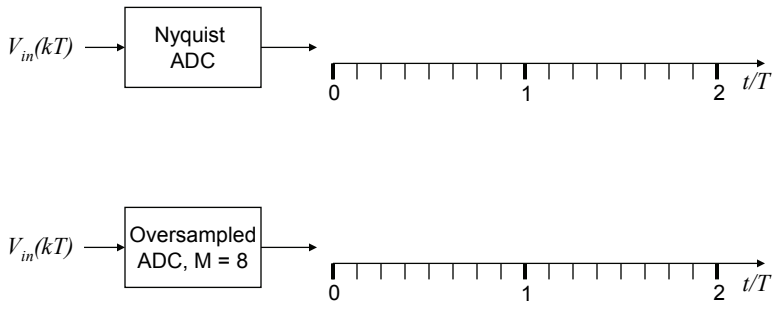
$$where\ M = \frac{f_s}{2f_B} = oversampling\ ratio$$

2X increase in M
→ 3dB reduction in S_B
→ ½ bit increase in resolution/octave oversampling

To increase the improvement in resolution:

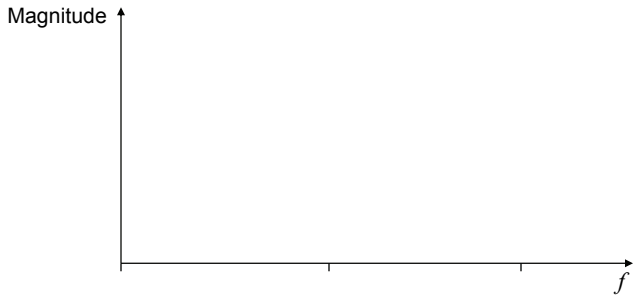
- Embed quantizer in a feedback loop
  →Noise shaping (sigma delta modulation)

Pulse-Count Modulation



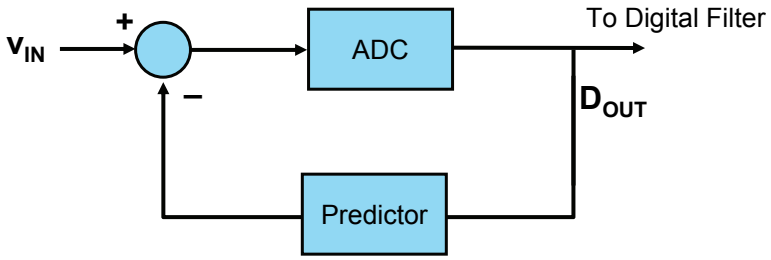
Mean of pulse-count signal approximates analog input!

Pulse-Count Spectrum



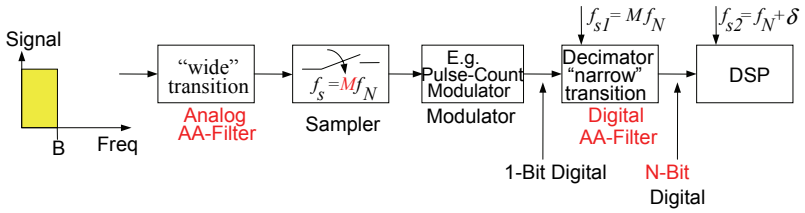
- Signal: low frequencies, $f < B << f_s$
- Quantization error: high frequency, $B \ldots f_s / 2$
- Separate with low-pass filter!

Oversampled ADC Predictive Coding



- Quantize the difference signal rather than the signal itself
- Smaller input to ADC → Buy dynamic range
- Only works if combined with oversampling
- 1-Bit digital output
- Digital filter computes "average" →N-Bit output

Oversampled ADC



Decimator:

- Digital (low-pass) filter
- Removes quantization error for f > B
- Provides anti-alias filtering for DSP
- Narrow transition band, high-order
- 1-Bit input, N-Bit output (essentially computes "average")

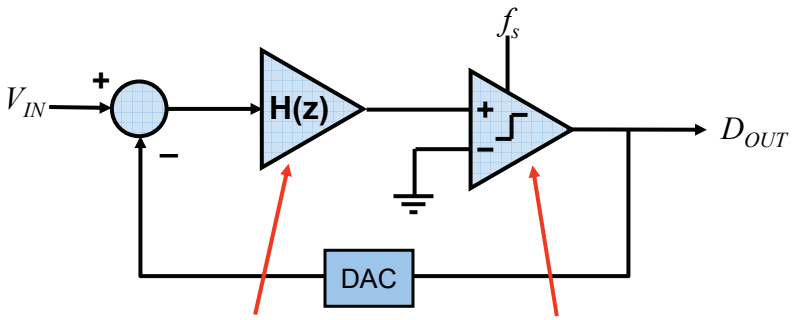
Modulator (AFE)

- Objectives:
  - Convert analog input to 1-Bit pulse density stream
  - Move quantization error to high frequencies f >>B
  - Operates at high frequency $f_s >> f_N$
    - M = 8 … 256 (typical)….1024
    - Since modulator operated at high frequencies → need to keep circuitry "simple"

→ ΣΔ = ΔΣ Modulator

Sigma- Delta Modulators

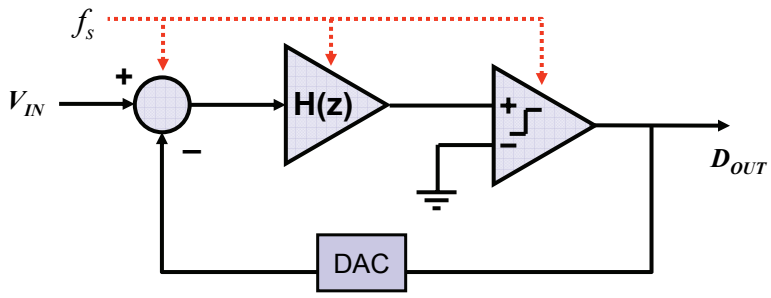
Analog 1-Bit ΣΔ modulators convert a continuous time analog input v_{IN} into a 1-Bit sequence D_{OUT}



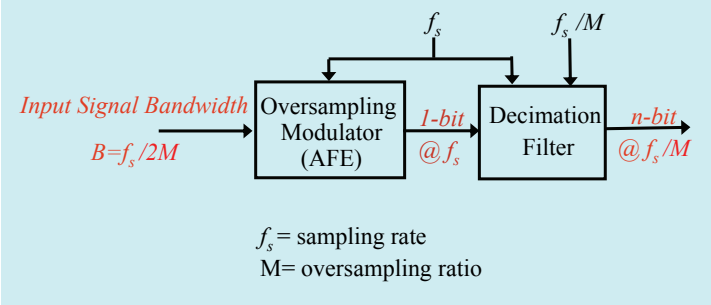
Loop filter **1b Quantizer (comparator)**

Sigma-Delta Modulators

- The loop filter H can be either switched-capacitor or continuous time
- Switched-capacitor filters are "easier" to implement + frequency characteristics scale with clock rate
- Continuous time filters provide anti-aliasing protection
- Loop filter can also be realized with passive LC's at very high frequencies



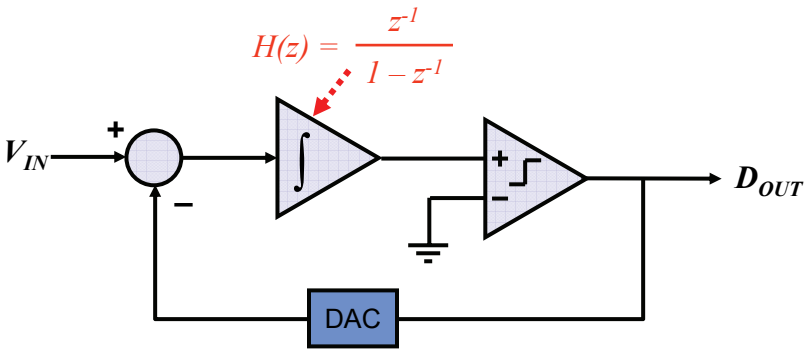
Oversampling A/D Conversion



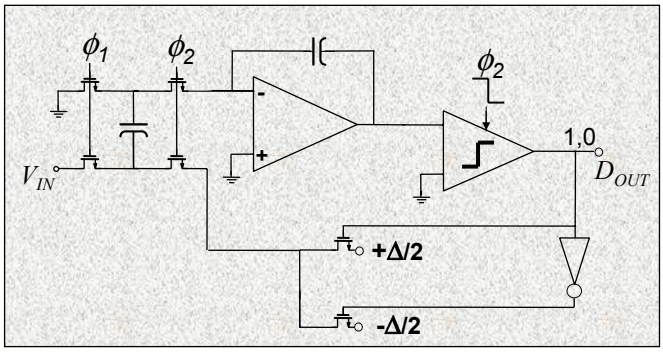
- Analog front-end → oversampled noise-shaping modulator
  - Converts original signal to a 1-bit digital output at the high rate of (*2MXB*)
- Digital back-end → digital filter (decimation)
  - Removes out-of-band quantization noise
  - Provides anti-aliasing to allow re-sampling @ lower sampling rate

1st Order ΣΔ Modulator

In a 1st order modulator, simplest loop filter → an integrator

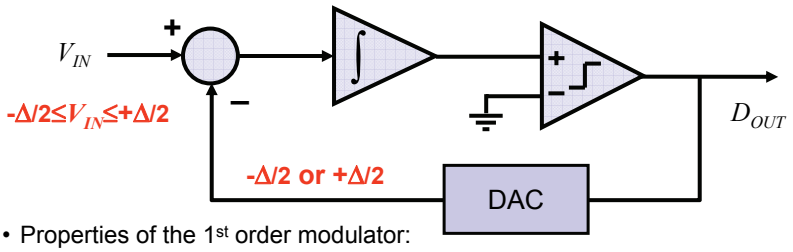


1st Order ΣΔ Modulator
Switched-capacitor implementation



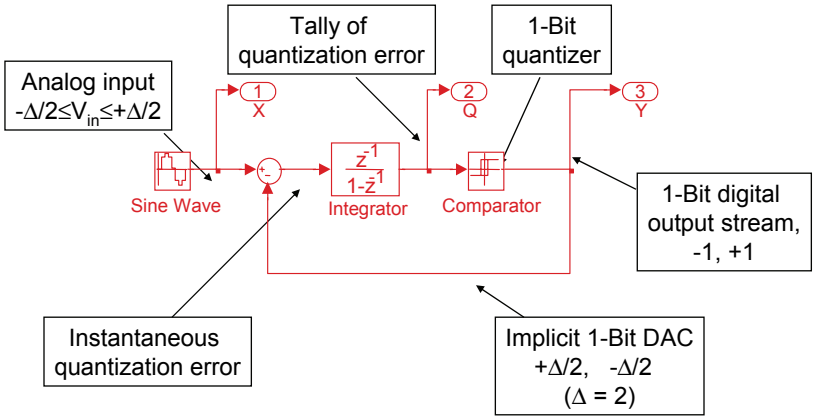
– Full-scale input range → Δ
– Note that Δ here is different from Nyquist rate ADC Δ (1LSB)

1st Order ΔΣ Modulator



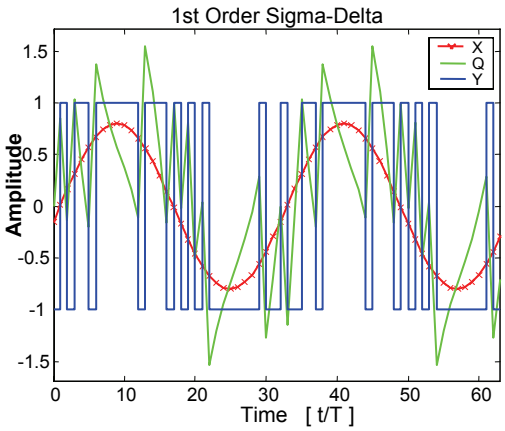
- Properties of the 1st order modulator:
  – Maximum analog input range is equal to the DAC reference
  – The average value of D_{OUT} must equal the average value of V_{IN}
  – +1's (or –1's) density in D_{OUT} is an inherently monotonic function of V_{IN}
    → To 1st order, linearity is not dependent on component matching
  – Alternative multi-bit DAC (and ADCs) solutions reduce the quantization error but loose this inherent monotonicity & relaxed matching requirements

1st Order ΣΔ Modulator



- M chosen to be 8 (low) to ease observability

1st Order Modulator Signals



X analog input
Q tally of q-error
Y digital/DAC output

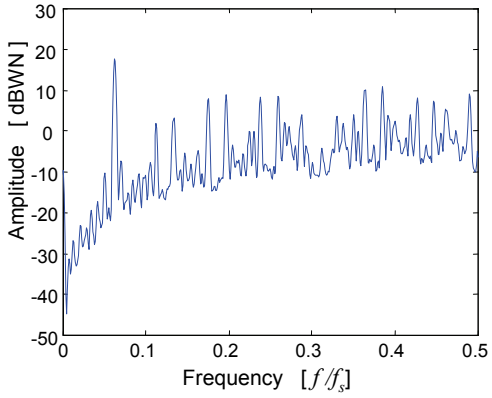
Mean of Y approximates X
That is exactly what the digital filter does

$T = 1/f_s = 1/ (M f_N)$

ΣΔ Modulator Characteristics

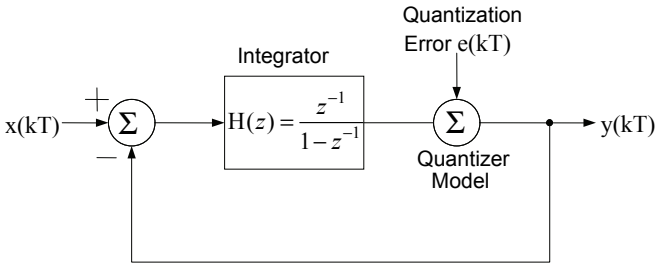
- Inherently linear for 1-Bit DAC
- Quantization noise and thermal noise (KT/C) distributed over $-f_s/2$ *to* $+f_s/2$
  - →Total noise within signal bandwidth reduced by 1/M
  - → Required capacitor sizes $x1/M$ compared to nyquist rate ADCs
- Very high SQNR achievable (> 20 Bits!)
- To first order, quantization error independent of component matching
- Limited to moderate & low speed

Output Spectrum



- Definitely not white!
- Skewed towards higher frequencies
- Notice the distinct tones
- dBWN (dB White Noise) scale sets the 0dB line at the noise per bin of a random -1, +1 sequence

Quantization Noise Analysis

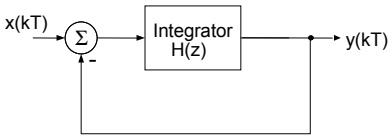


- Sigma-Delta modulators are nonlinear systems with memory → difficult to analyze directly
- Representing the quantizer as an additive noise source linearizes the system

Signal Transfer Function

$$H(z)=\frac{z^{-1}}{1-z^{-1}}$$

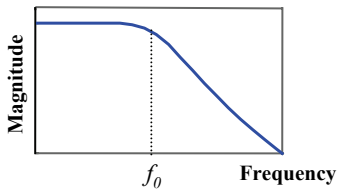
$$H(j\omega)=\frac{\omega_0}{j\omega}$$



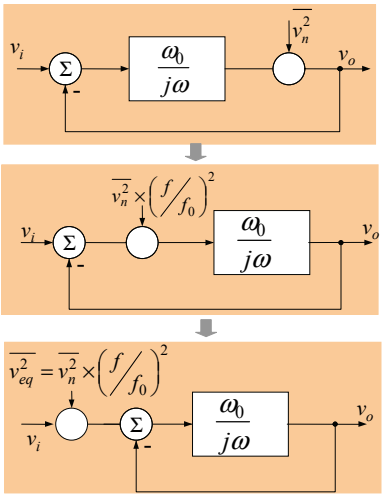
Signal transfer function
→ low pass function:

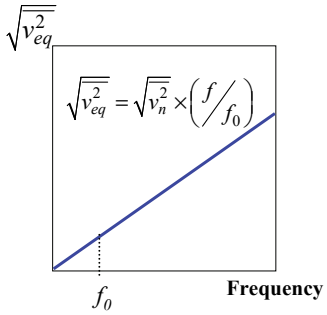
$$H_{Sig}(j\omega)=\frac{1}{1+\frac{s}{\omega_0}}$$

$$H_{Sig}(z)=\frac{Y(z)}{X(z)}=\frac{H(z)}{1+H(z)}=z^{-1} \quad \Rightarrow \quad \text{Delay}$$



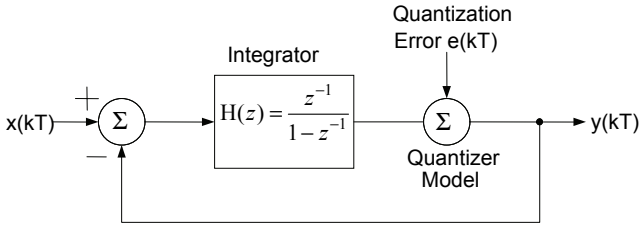
Noise Transfer Function
Qualitative Analysis





- Input referred-noise→ zero @ DC (s-plane)

STF and NTF



Signal transfer function:

$$\text{STF}=\frac{Y(z)}{X(z)}=\frac{H(z)}{1+H(z)}=z^{-1} \quad \Rightarrow \quad \text{Delay}$$

Noise transfer function:

$$\text{NTF}=\frac{Y(z)}{E(z)}=\frac{1}{1+H(z)}=1-z^{-1} \quad \Rightarrow \quad \text{Differentiator}$$

Noise Transfer Function

$$NTF = \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)} = 1 - z^{-1} \qquad \text{set} \quad z = e^{j\omega T}$$

$$NTF(j\omega) = (1 - e^{-j\omega T}) = 2e^{-j\omega T/2}\left(\frac{e^{j\omega T/2} - e^{-j\omega T/2}}{2}\right)$$

$$= 2e^{-j\omega T/2} j \sin(\omega T/2)$$

$$= 2e^{-j\omega T/2} \times e^{-j\pi/2}\left[\sin(\omega T/2)\right]$$

$$= \left[2\sin(\omega T/2)\right] e^{-j(\omega T - \pi)/2}$$

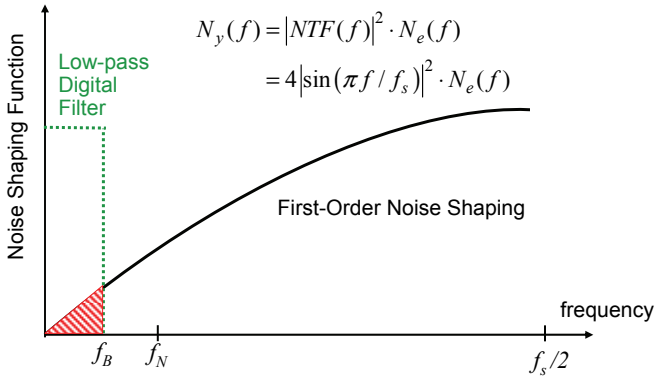
where $T = 1/f_s$

Thus:

$$|NTF(f)| = 2\left|\sin(\omega T/2)\right| = 2\left|\sin(\pi f/f_s)\right|$$

$$N_y(f) = |NTF(f)|^2 N_e(f)$$

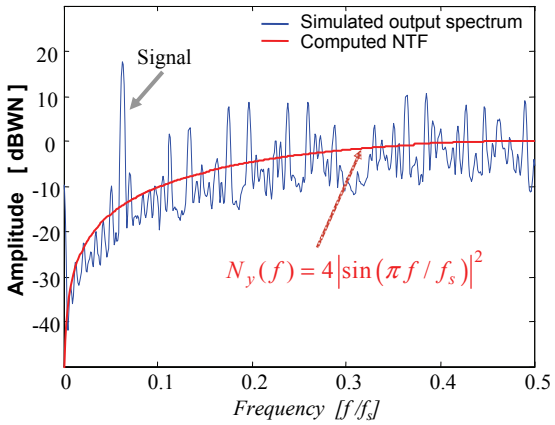
First Order ΣΔ Modulator Noise Transfer Characteristics



Key Point:

Most of quantization noise pushed out of frequency band of interest

First Order ΣΔ Modulator
Simulated Noise Transfer Characteristic



- Confirms assumption of quantization noise being white at insertion point

Quantizer Error

- For quantizers with many bits

$$\overline{e^2(kT)} = \frac{\Delta^2}{12}$$

- Let's use the same expression for the 1-Bit case
- **Use simulation to verify validity**
- Experience: Often sufficiently accurate to be useful, with enough exceptions to be very careful

First Order ΣΔ Modulator
In-Band Quantization Noise

$$NTF(z) = 1 - z^{-1}$$

$$\left|NTF(f)\right|^2 = 4\left|\sin(\pi f / f_s)\right|^2 \quad for \quad M >> 1$$

$$\overline{S_Y} = \int_{-B}^{B} S_Q(f)\left|NTF(z)\right|^2_{z=e^{2\pi jfT}}\, df$$

$$\cong \int_{-f_s/2M}^{f_s/2M} \frac{1}{f_s}\frac{\Delta^2}{12}(2\sin\pi fT)^2\, df$$

$$\rightarrow \overline{S_Y} \approx \frac{\pi^2}{3}\frac{1}{M^3}\frac{\Delta^2}{12}$$

Dynamic Range

$$DR = 10\log\left[\frac{\text{full-scale signal power}}{\text{inband noise power}}\right] = 10\log\left[\frac{\overline{S_X}}{\overline{S_Y}}\right]$$

$$\overline{S_X} = \frac{1}{2}\left(\frac{\Delta}{2}\right)^2 \qquad \text{sinusoidal input,} \quad STF = 1$$

$$\overline{S_Y} = \frac{\pi^2}{3}\frac{1}{M^3}\frac{\Delta^2}{12}$$

$$\frac{\overline{S_X}}{\overline{S_Y}} = \frac{9}{2\pi^2}M^3$$

$$DR = 10\log\left[\frac{9}{2\pi^2}M^3\right] = 10\log\left[\frac{9}{2\pi^2}\right] + 30\log M$$

$$DR = -3.4dB + +30\log M$$

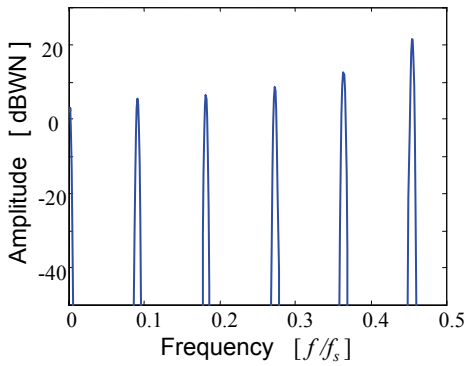
M	DR
16	33 dB
32	42 dB
1024	87 dB

2X increase in M➔9dB (1.5-Bit) increase in dynamic range

Oversampling and Noise Shaping

- ΣΔ modulators have interesting characteristics
  - Unity gain for input signal V_{IN}
  - Large in-band attenuation of quantization noise injected at quantizer input
  - Performance significantly better than 1-Bit noise performance possible for frequencies << f_s
- Increase in oversampling ($M = f_s/f_N >> 1$) improves SQNR considerably
  - 1st order ΣΔ: DR increases 9dB for each doubling of M
  - To first order, SQNR independent of circuit complexity and accuracy
- Analysis assumes that the quantizer noise is "white"
  - Not true in practice, especially for low-order modulators
  - Practical modulators suffer from other noise sources also (e.g. thermal noise)

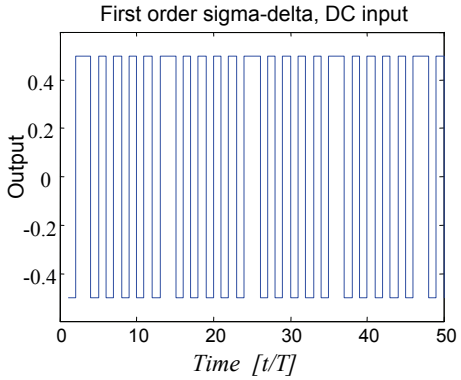
DC Input



- DC input A = 1/11
- Doesn't look like spectrum of DC at all
- Tones frequency shaped the same as quantization noise
  → More prominent at higher frequencies

  → Seems like periodic quantization "noise"

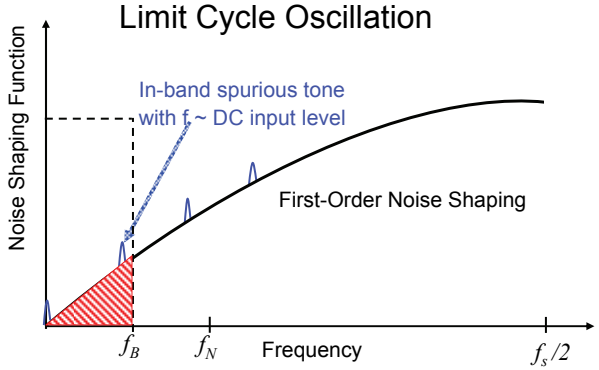
Limit Cycle Oscillation



DC input 1/11 →
Periodic sequence:

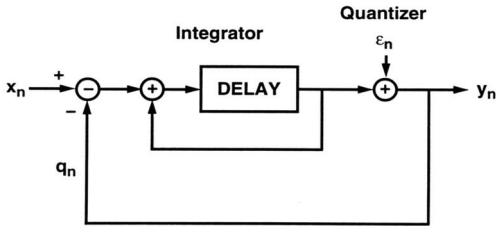
1	+1
2	+1
3	-1
4	+1
5	-1
6	+1
7	-1
8	+1
9	-1
10	+1
11	-1

1st Order ΣΔ Limit Cycle Oscillation



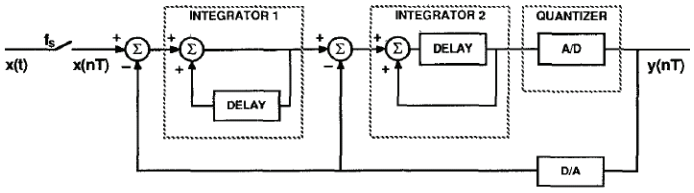
- Problem: quantization noise becomes periodic in response to low level DC inputs & could fall within passband of interest!
- Solution:
  - Use dithering (inject noise-like signal at the input): randomizes quantization noise
    - If circuit thermal noise if large enough→ acts as dither
  - Second order loop

1st Order ΣΔ Modulator Linearized Model Analysis



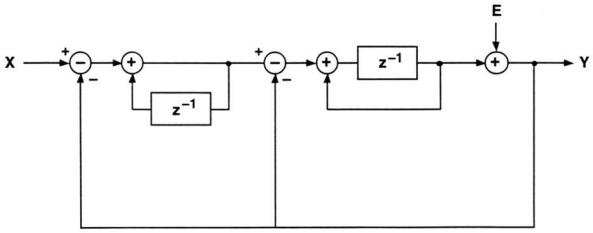
$$Y(z) = \underbrace{z^{-1}}_{\text{LPF}} X(z) + \underbrace{\left(1 - z^{-1}\right)}_{\text{HPF}} E(z)$$

2nd Order ΣΔ Modulator



- Two integrators in series
- Single quantizer (typically 1-bit)
- Feedback from output to both integrators
- Tones less prominent compared to 1st order

2nd Order ΣΔ Modulator
Linearized Model Analysis



Recursive drivation: $Y_n = X_{n-1} + (E_n - 2E_{n-1} + E_{n-2})$

Using the delay operator z^{-1} : $Y(z) = \underbrace{z^{-1}}_{\text{LPF}} X(z) + \underbrace{(1-z^{-1})^2}_{\text{HPF}} E(z)$

2nd Order ΣΔ Modulator
In-Band Quantization Noise

$$NTF(z) = (1-z^{-1})^2$$

$$|NTF(f)|^2 =$$

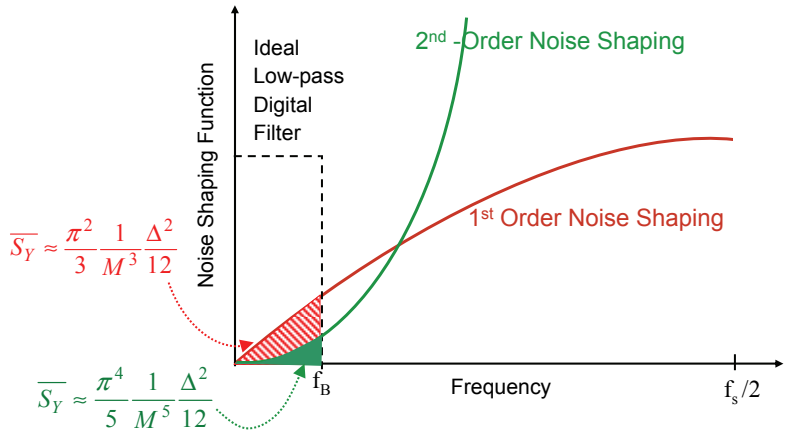
$$= 2^4 |\sin(\pi f / f_s)|^4 \quad \text{for} \quad M >> 1$$

$$\overline{S_Y} = \int_{-B}^{B} S_Q(f) |NTF(z)|^2_{z=e^{2\pi jfT}} \, df$$

$$\cong \int_{-f_s/2M}^{f_s/2M} \frac{1}{f_s} \frac{\Delta^2}{12} (2\sin \pi fT)^4 \, df$$

$$\approx \frac{\pi^4}{5} \frac{1}{M^5} \frac{\Delta^2}{12}$$

Quantization Noise
2nd Order ΣΔ Modulator vs 1st Order Modulator



2nd Order ΣΔ Modulator
Dynamic Range

$$DR = 10\log\left[\frac{\text{full-scale signal power}}{\text{inband noise power}}\right] = 10\log\left[\frac{\overline{S_X}}{\overline{S_Y}}\right]$$

$$\overline{S_X} = \frac{1}{2}\left(\frac{\Delta}{2}\right)^2 \qquad \text{sinusoidal input,} \quad STF = 1$$

$$\overline{S_Y} = \frac{\pi^4}{5}\frac{1}{M^5}\frac{\Delta^2}{12}$$

$$\frac{\overline{S_X}}{\overline{S_Y}} = \frac{15}{2\pi^4}M^5$$

$$DR = 10\log\left[\frac{15}{2\pi^4}M^5\right] = 10\log\left[\frac{15}{2\pi^4}\right] + 50\log M$$

$$DR = -11.1dB + 50\log M$$

M	DR (2nd)	DR (1st)
16	49 dB	33dB
32	64 dB	42dB
1024	139 dB	87dB

2X increase in M➔15dB (2.5-bit) increase in DR

2nd Order vs 1st Order ΣΔ Modulator Dynamic Range

M	2nd Order DR	1st Order DR	Resolution Difference
16	49 dB (7.8bit)	33dB (5.2bit)	2.6 bit
32	64 dB (10.3bit)	42dB (6.7bit)	3.6 bit
256	109 dB (17.9bit)	68.8dB (11.1bit)	6.8 bit
1024	139 dB (22.8bit)	87dB (14.2bit)	8.6 bit

– Note: For higher oversampling ratios resolution of 2nd order modulator significantly higher compared to 1st order

2nd Order ΣΔ Modulator Example

- Digital audio application
  - ✓ Signal bandwidth *20kHz*
  - ✓ Desired resolution *16-bit*

$16-bit \rightarrow 98dB$ Dynamic Range

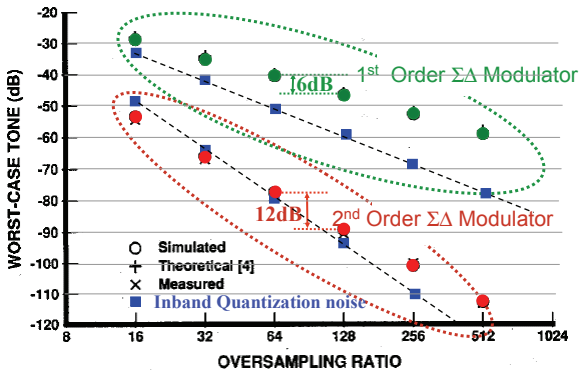
$$DR = -11.1dB + 50\log M$$
$$M_{\min} = 153$$

M → 256=2^8 to allow some margin so that thermal noise dominants & provides dithering & also choice of M power of 2 → ease of digital filter implementation

→ Sampling rate *(2x20kHz + 5kHz)M = 12MHz* (quite reasonable!)

Limit Cycle Tones in 1st Order & 2nd Order ΣΔ Modulator

- Higher oversampling ratio → lower tones
- 2nd order much lower tones compared to 1st
- 2X increase in M decreases the tones by 6dB for 1st order loop and 12dB for 2nd order loop



Ref: B. P. Brandt, et al., "Second-order sigma-delta modulation for digital-audio signal acquisition," IEEE Journal of Solid-State Circuits, vol. 26, pp. 618 - 627, April 1991.

R. Gray, "Spectral analysis of quantization noise in a single-loop sigma–delta modulator with dc input," *IEEE Trans. Commun.*, vol. 37, pp. 588–599, June 1989.