Notes on the Class Project

- ENOB=6bit for the case:
  - Input test signal a 10MHz full-scale sinusoidal signal
  - No non-idealities such as comparator offset added
  - Note that:
    - Transient analysis in Spectre or HSpice does not include device noise
    - Device models do not address charge injection for switches
  → Results obtained from transient analysis + FFT will indicate performance better than measured data from actual silicon

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EE247
Lecture 24
Oversampled ADCs (continued)

– 2nd order ΣΔ modulator
  - Practical implementation
    - Effect of various building block nonidealities on the ΣΔ performance
      - Integrator maximum signal handling capability
      - Integrator finite DC gain
      - Comparator hysteresis (minimum signal handling capability)
      - Integrator non-linearity
      - Effect of KT/C noise
      - Finite opamp bandwidth
      - Opamp slew limited settling
    - Implementation example
– Higher order ΣΔ modulators
  - Cascaded modulators (multi-stage)
  - Single-loop single-quantizer modulators with multi-order filtering in the forward path
**ΣΔ Implementation**  
**Practical Design Considerations**

- Internal node scaling & clipping
- Effect of finite opamp gain & linearity
- KT/C noise
- Opamp noise
- Finite opamp bandwidth
- Opamp slew limited settling
- Effect of comparator nonidealities
- Power dissipation considerations

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**Switched-Capacitor Implementation 2nd Order ΣΔ**  
**Nodes Scaled for Maximum Dynamic Range**

- Modification (gain of ½ in front of integrators) reduce & optimize required signal range at the integrator outputs ~ 1.7x input full-scale (Δ)
- Note: Non-idealities associated with 2nd integrator and quantizer when referred to the ΣΔ input is attenuated by 1st integrator high gain
  - The only building block requiring low-noise and high accuracy is the 1st integrator

2nd Order $\Sigma\Delta$ Modulator
Example: Switched-Capacitor Implementation

- Fully differential front-end
- Two bottom-plate integrators
- 1-bit DAC is made of switches and Vrefs

$C_2 = 2C_1 \Rightarrow f_{0,\text{intg}} = f_s / (4\pi)$
Design Phase Simulations

- Design of oversampled ADCs requires simulation of extremely long data traces due to the oversampled nature of the system
- SPICE type simulators:
  - Normally used to test for gross circuit errors only
  - Too slow for detailed performance verification
- Typically, behavioral modeling is used in MATLAB-like environments
- Circuit non-idealities either computed or found by using SPICE at subcircuit level
- Non-idealities introduced in the behavioral model one-by-one first to fully understand the effect of each individually
- Next step is to add as many of the non-idealities simultaneously as possible to verify whether there are interaction among non-idealities

Testing of AFE

- Typically in the design phase, provisions are made to test the AFE separate from Decimator
- Output of the AFE (0,1) is acquired by a data acquisition board or logic analyzer
- Matlab-like program is used to analyze data e.g. perform filtering & measure SNR, SNDR.....
- During pre-silicon design phase, output of AFE is filtered in software & Matlab used to measure SNR, SNDR
Example: Testing $\Sigma\Delta$ ADC

Note:
The Nyquist ADC tests such as INL and DNL test do not apply to $\Sigma\Delta$ modulator type ADCs

$\Sigma\Delta$ testing is performed via SNDR as a function of input signal level

$2^{nd}$ Order $\Sigma\Delta$

Effect of 1st Integrator Maximum Signal Handling Capability on SNR

- Behavioral model
- Non-idealities tested one by one

2nd Order $\Sigma\Delta$

Effect of 2nd Integrator Maximum Signal Handling Capability on SNR

- Effect of 2nd Integrator maximum signal handling capability on SNR
  $\Rightarrow$ No SNR loss for max. sig. handling $>1.7 \Delta$


Effect of Integrator Finite DC Gain

$\phi_1$, $\phi_2$, $a$, $Vo$, $Cs$, $CI$

$H(z)_{ideal} = \frac{Cs}{Cl} \times \frac{z^{-1}}{1 - z^{-1}}$

$H(z)_{Fint \ DC \ Gain} = \frac{Cs}{Cl} \times \frac{\left(\frac{a}{1 + a + \frac{Cs}{Cl}}\right)z^{-1}}{1 - \left(\frac{1 + a + \frac{Cs}{Cl}}{1 + a + \frac{Cs}{Cl}}\right)z^{-1}}$

$\Rightarrow H(DC) = a$
1\textsuperscript{st} & 2\textsuperscript{nd} Order \(\Sigma\Delta\) 
Effect of Integrator Finite DC Gain Analysis

- Low integrator DC gain \( \Rightarrow \) Increase in total in-band quantization noise
- Can be shown: If \( a > M \) (oversampling ratio) \( \Rightarrow \) Insignificant degradation in SNR
- Normally DC gain designed to be \( > > M \) in order to suppress nonlineairties
2nd Order ΣΔ
Effect of Integrator Finite DC Gain

- Example: \( a = 2M \) → 0.4dB degradation in SNR
- \( a = M \) → 1.4dB degradation in SNR


1-bit A/D → Single comparator
- Speed must be adequate for the operating sampling rate
- Input referred offset- feedback loop & high DC intg. gain suppresses the effect
  → ΣΔ performance quite insensitive to comparator offset
- Input referred comparator noise- same as offset
- Hysteresis= Minimum overdrive required to change the output
Comparator Hysteresis

Hysteresis = Minimum overdrive required to change the output

Comparator hysteresis < $\Delta/25$ does not affect SNR

E.g. $\Delta=1V$, comparator hysteresis up to 40mV tolerable

Key Point: One of the main advantages of $\Sigma\Delta$ ADCs → Highly tolerant of comparator and in general building-block non-idealities
2nd Order ΣΔ
Effect of Integrator Nonlinearities

With non-linearity added:

\[ v(kT + T) = u(kT) + \alpha_1 u(kT)^2 + \alpha_2 [u(kT)]^3 + \ldots \]
\[ + v(kT) + \beta_1 [v(kT)]^3 + \beta_2 [v(kT)]^5 + \ldots \]


---

2nd Order ΣΔ
Effect of Integrator Nonlinearities (Single-Ended)

- Simulation for single-ended topology
- Effect of even order nonlinearities can be significantly suppressed by using differential circuit topologies

2nd Order ΣΔ
Effect of Integrator Nonlinearities

- Simulation for single-ended topology
- Odd order nonlinearities (3rd in this case)
- Odd order nonlinearities (usually 3rd) could cause significant loss of SNDR for high resolution oversampled ADCs
- Two significant source of non-linearities:
  - Non-linearities associated with opamp used to build integrators
    - Opamp open-loop non-linearities are suppressed by the loopgain since there is feedback around the opamp
    - Class A opamps tend to have lower open-loop gain but more linear output versus input transfer characteristic
    - Class A/B opamps typically have higher open-loop gain but non-linear transfer function. At times this type is preferred for ΣΔ AFE due to its superior slew rate compared to class A type
  - Integrator capacitor non-linearities
    - Poly-Sio2-Poly capacitors → C non-linearity in the order of 10ppm/V
    - Metal-Sio2-Metal capacitors ~ 1ppm/V

2nd Order $\Sigma \Delta$

Effect of Integrator $KT/C$ noise

For the example of digital audio with 16-bit (96dB) & $M=256$ (110dB SQNR)

→ $C_s=1pF$ → 7$\mu$Vrms noise

→ If $V_{fs}=2V_{p-p}$ then thermal noise @ -101dB → degrades overall SNR by ~10dB

→ $C_s=1pF, C_l=2pF$ → much smaller capacitor area (~1/M) compared to Nyquist ADC

→ Since thermal noise provides some level of dithering → better not choose much larger capacitors!

---

2nd Order $\Sigma \Delta$

Effect of Finite Opamp Bandwidth

Assumptions:

Opamp → does not slew
Opamp has only one pole → exponential settling
2nd Order $\Sigma\Delta$

Effect of Finite Opamp Bandwidth

$\rightarrow \Sigma\Delta$ does not require high opamp bandwidth $\tau / \tau > 2$ or $f_u > 2f_s$ adequate

Note: Bandwidth requirements significantly more relaxed compared to Nyquist rate ADCs


2nd Order $\Sigma\Delta$

Effect of Slew Limited Settling
2nd Order $\Sigma\Delta$

Effect of Slew Limited Settling

Assumption:
- Opamp settling includes a single-pole setting of $\tau = \frac{1}{2f_s}$ + slewing
- Low slew rate degrades SNR rapidly, increases quantization noise and also causes signal distortion
- Minimum slew rate of $S_{\text{min}} \approx 1.2 (\Delta \times f_s)$ required


2nd Order $\Sigma\Delta$

Implementation Example: Digital Audio Application

- In Ref.: 5V supply, $\Delta = 4V_{\text{p-p}}$, $f_s = 12.8\text{MHz} \Rightarrow M = 256 \Rightarrow$ theoretical quantization noise @-110dB
- Minimum capacitor values computed based on -104dB noise wrt maximum signal
  - Max. inband KT/C noise = $7\mu V_{\text{rms}}$ (thermal noise dominates $\Rightarrow$ provide dithering & reduce limit cycle oscillations)
  - $C_1 = \frac{2kT}{M v_n^2} = 1pF$ $C_2 = 2C_1$

2nd Order $\Sigma\Delta$
Implementation Example: Integrator Opamp

- Class A/B type opamp $\rightarrow$ High slew-rate
- S.C. common-mode feedback
- Input referred noise (both thermal and 1/f) important for high resolution performance
- Minimum required DC gain $> M=256$, usually DC gain designed to be much higher to suppress nonlinearities (particularly, for class A/B amps)
- Minimum required slew rate of $1.2(\Delta f) \rightarrow 65\text{V}/\text{usec}$
- Minimum opamp settling time constant $\rightarrow 1/2fs \sim 30\text{ns}$


---

2nd Order $\Sigma\Delta$
Implementation Example: Comparator

- Comparator $\rightarrow$ simple design
- Maximum acceptable hysteresis or offset (based on analysis) $\rightarrow \Delta/25 \sim 160\text{mV}$
- Have to make sure adequate speed for the chosen sampling freq.
  $\rightarrow$ Since offset requirement not stringent $\rightarrow$ No preamp needed, basically a latch with reset

2nd Order $\Sigma\Delta$
Implementation Example: Subcircuit Performance

<table>
<thead>
<tr>
<th>Subcircuit Performance</th>
<th>Our computed minimum required</th>
<th>Over-Design Factor</th>
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</thead>
<tbody>
<tr>
<td>Operational Amplifier</td>
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<tr>
<td>DC gain</td>
<td>67 dB</td>
<td>x8</td>
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<td>Unity-gain frequency</td>
<td>50 MHz</td>
<td></td>
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<tr>
<td>Slew rate</td>
<td>350 V/μsec</td>
<td>x2</td>
</tr>
<tr>
<td>Linear output range</td>
<td>6 V</td>
<td>x5</td>
</tr>
<tr>
<td>Sampling rate</td>
<td>12.8 MHz</td>
<td></td>
</tr>
<tr>
<td>Integrator</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Settling time constant</td>
<td>7.25 nsec</td>
<td>x4</td>
</tr>
<tr>
<td>Comparator</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Offset</td>
<td>13 mV</td>
<td>x12</td>
</tr>
<tr>
<td></td>
<td>Output range 1.7Δ=6.8V1</td>
<td>X0.9</td>
</tr>
<tr>
<td></td>
<td>Settling time constant≈30nsec</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Comparator offset 160mV</td>
<td></td>
</tr>
</tbody>
</table>


Measured SNDR
M=256, 0dB=4V_{p-p}d
$f_{\text{sampling}}$: 12.8MHz
Test signal frequency: 2.8kHz

2nd Order $\Sigma\Delta$

Implementation Example: Digital Audio Applications

Measured Performance Summary
(Does Not Include Decimator)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dynamic Range</td>
<td>98 dB (16 b)</td>
</tr>
<tr>
<td>Peak SNDR</td>
<td>94 dB</td>
</tr>
<tr>
<td>Sampling Rate</td>
<td>12.8 MHz</td>
</tr>
<tr>
<td>Oversampling Ratio</td>
<td>256</td>
</tr>
<tr>
<td>Output Rate</td>
<td>50 kHz</td>
</tr>
<tr>
<td>Signal Band</td>
<td>23 kHz</td>
</tr>
<tr>
<td>Differential Input Range</td>
<td>4 V</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>5 V</td>
</tr>
<tr>
<td>Power Supply Rejection</td>
<td>60 dB</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>13.8 mW</td>
</tr>
<tr>
<td>Area</td>
<td>0.39 mm$^2$</td>
</tr>
<tr>
<td>Technology</td>
<td>1-\mu m CMOS</td>
</tr>
</tbody>
</table>

2nd Order $\Sigma\Delta$ Implementation Example: Digital Audio Applications

- Measured & simulated in-band spurious tones as a function of DC input signal
- Sampling rate=12.8MHz, $M=256$


---

2nd Order $\Sigma\Delta$ Implementation Example: Digital Audio Applications

- Measured & simulated noise tone performance for near zero DC worst case input $\rightarrow 0.00088 \Delta$

2nd Order $\Sigma \Delta$
Implementation Example: Digital Audio Applications

- Measured & simulated worst-case noise tone @ DC input of 0.00088Δ
- Both indicate maximum tone @ 22.5kHz around -100dB level


Higher Order $\Sigma \Delta$ Modulator Dynamic Range

$Y(z) = z^{-1}X(z) + \left(1 - z^{-1}\right)^L E(z)$, $L \rightarrow \Sigma \Delta$ order

$\overline{S_X} = \left(\frac{\Delta}{\Delta_2}\right)^2$ sinusoidal input, $STF = 1$

$\frac{S_Q}{S_Q} = \frac{\pi^{2L}}{2L+1} \frac{1}{M^{2L+1} 12}$

$\frac{S_X}{S_Q} = \frac{3(2L+1)}{2\pi^{2L}} M^{2L+1}$

$DR = 10 \log \left[ \frac{3(2L+1)}{2\pi^{2L}} M^{2L+1} \right]$ 

$DR = 10 \log \left[ \frac{3(2L+1)}{2\pi^{2L}} \right] + (2L+1) \times 10 \times \log M$

$2X$ increase in $M \rightarrow (6L+3)\text{dB}$ or $(L+0.5)$-bit increase in DR
Higher Order $\Sigma \Delta$ Modulators

- Extending $\Sigma \Delta$ Modulators to higher orders by adding integrators in the forward path (similar to 2nd order)
  - Issues with stability

- Two different architectural approaches used to implement $\Sigma \Delta$ modulators with order >2
  1. Cascade of lower order modulators (multi-stage)
  2. Single-loop single-quantizer modulators with multi-order filtering in the forward path
Higher Order $\Sigma\Delta$ Modulators

(1) Cascade of 2-Stages $\Sigma\Delta$ Modulators

- Main $\Sigma\Delta$ quantizes the signal
- The 1st stage quantization error is then quantized by the 2nd quantizer
- The quantized error is then subtracted from the results in the digital domain

2nd Order (1-1) Cascaded $\Sigma\Delta$ Modulators

$Y_1(z) = z^{-2}x(z) + (1 - z^{-1})E_1(z)$

$Y_2(z) = z^{-2}E_1(z) + (1 - z^{-1})E_2(z)$

$Y(z) = z^{-2}Y_1(z) - (1 - z^{-1})Y_2(z)$

$= z^{-2}x(z) + z^{-2}(1 - z^{-1})E_1(z) - z^{-2}(1 - z^{-1})E_1(z)$

$= z^{-2}x(z) - (1 - z^{-1})^2E_2(z)$

$Y(z) = z^{-2}x(z) - (1 - z^{-1})^2E_2(z)$

2nd order noise shaping
3rd Order Cascaded \(\Sigma\Delta\) Modulators

(a) Cascade of 1-1-1 \(\Sigma\Delta\)s

- Can implement 3rd order noise shaping with 1-1-1
- This is also called MASH (multi-stage noise shaping)

(b) Cascade of 2-1 \(\Sigma\Delta\)s

Advantages of 2-1 cascade compared to 1-1-1:

- Low sensitivity to matching precision of analog/digital paths
- Low spurious limit cycle tone levels
- No potential instability

3rd order noise shaping
Sensitivity of Cascade of $\Sigma\Delta$ Modulators to Matching of Analog & Digital Paths

Matching of $\sim 1\%$ → 28dB loss in DR

Matching of $\sim 0.1\%$ → 2dB loss in DR

Main advantage of 2-1 cascade compared to 1-1-1 topology:
- Low sensitivity to matching of analog/digital paths (in excess of one order of magnitude less sensitive compared to (1-1-1)!)

Sensitivity of Cascade of (2-1) $\Sigma\Delta$ Modulators to Matching Error

Matching of $< \sim 3\%$ → 2dB loss in DR
2-1 Cascaded $\Sigma\Delta$ Modulators


Effect of gain parameters on signal-to-noise ratio
### Comparison of 2\textsuperscript{nd} order & Cascaded (2-1) ΣΔ Modulator

**Digital Audio Application, \( f_N = 50kHz \)**

*(Does not include Decimator)*

<table>
<thead>
<tr>
<th>Reference</th>
<th>Brandt, JSSC 4/91</th>
<th>Williams, JSSC 3/94</th>
</tr>
</thead>
<tbody>
<tr>
<td>Architecture</td>
<td>2\textsuperscript{nd} order</td>
<td>(2+1) Order</td>
</tr>
<tr>
<td>Dynamic Range</td>
<td>98dB (16-bits)</td>
<td>104dB (17-bits)</td>
</tr>
<tr>
<td>Peak SNDR</td>
<td>94dB</td>
<td>98dB</td>
</tr>
<tr>
<td>Oversampling rate</td>
<td>256 (theoretical → SNR=109dB)</td>
<td>128 (theoretical → SNR=128dB)</td>
</tr>
<tr>
<td>Differential input range</td>
<td>4Vppd 5V supply</td>
<td>8Vppd 5V supply</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>13.8mW</td>
<td>47.2mW</td>
</tr>
<tr>
<td>Active Area</td>
<td>0.39mm(^2)/1(\mu) tech.</td>
<td>5.2mm(^2)/1(\mu) tech.</td>
</tr>
</tbody>
</table>

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### 2-1 Cascaded ΣΔ Modulators

**Measured Dynamic Range Versus Oversampling Ratio**

Higher Order $\Sigma\Delta$ Modulators

(1) Cascaded Modulators Summary

- Cascade two or more stable $\Sigma\Delta$ stages
- Quantization error of each stage is quantized by the succeeding stage/s and subtracted digitally
- Order of noise shaping equals sum of the orders of the stages
- Quantization noise cancellation depends on the precision of analog/digital signal paths
- Quantization noise further randomized $\Rightarrow$ less limit cycle oscillation problems
- Typically, no potential instability

(2) Multi-Order Filter

- Zeros of NTF (poles of $H(z)$) can be strategically positioned to suppress in-band noise spectrum
- Approach: Design NTF first and solve for $H(z)$

\[ Y(z) = \frac{H(z)}{1 + H(z)} X(z) + \frac{1}{1 + H(z)} E(z) \]

\[ NTF = \frac{Y(z)}{E(z)} \frac{1}{1 + H(z)} \]
Example: Modulator Specification

- **Example: Audio ADC**
  - Dynamic range (DR) 18 Bits
  - Signal bandwidth (B) 20 kHz
  - Nyquist frequency (f_N) 44.1 kHz
  - Modulator order (L) 5
  - Oversampling ratio (M = f_s/f_N) 64
  - Sampling frequency (f_s) 2.822 MHz

- The order L and oversampling ratio M are chosen based on
  - SQNR > 120dB

---

Noise Transfer Function, NTF(z)

```matlab
% stop-band attenuation Rstop=80dB, L=5 ...
L=5;
Rstop = 80;
B=20000;
[b,a] = cheby2(L, Rstop, B, 'high');

% normalize
b = b/b(1);
NTF = filt(b, a, ...);
```

Chebychev II filter chosen → zeros in stop-band
Loop-Filter Characteristics

\[ H(z) \]

\[ NTF = \frac{Y(z)}{E(z)} = \frac{1}{1 + H(z)} \]

\[ \Rightarrow H(z) = \frac{1}{NTF} - 1 \]

Note: For 1st order \( \Sigma\Delta \) an integrator is used instead of the high order filter shown.
Filter Coefficients

\[ a_1 = 1; \quad k_1 = 1; \quad b_1 = 1/1024; \]
\[ a_2 = 1/2; \quad k_2 = 1; \quad b_2 = 1/16-1/64; \]
\[ a_3 = 1/4; \quad k_3 = 1/2; \]
\[ a_4 = 1/8; \quad k_4 = 1/4; \]
\[ a_5 = 1/8; \quad k_5 = 1/8; \quad g = 1; \]

Ref: Nav Sooch, Don Kerth, Eric Swanson, and Tetsuro Sugimoto, “Phase Equalization System for a Digital-to-Analog Converter Using Separate Digital and Analog Sections”, U.S. Patent 5061925, 1990, figure 3 and table 1

5th Order Noise Shaping Simulation Results

- Mostly quantization noise, except at low frequencies
- Let’s zoom into the baseband portion…
### 5th Order Noise Shaping

- SQNR > 120dB
- Sigma-delta modulators are usually designed for negligible quantization noise
- Other error sources dominate, e.g. thermal noise are allowed to dominate & thus provide dithering to eliminate limit cycle oscillations

### In-Band Noise Shaping

- Lot’s of gain in the loop filter pass-band
- Forward path filter not necessarily stable!
- Remember that:
  - $\text{NTF} \sim 1/H \Rightarrow$ small within passband since $H$ is large
  - $\text{STF} = H/(1+H) \Rightarrow -1$ within passband

<table>
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<th>Frequency $[f/f_N]$</th>
<th>Magnitude [dB]</th>
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<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0.2</td>
<td>40</td>
</tr>
<tr>
<td>0.4</td>
<td>120</td>
</tr>
<tr>
<td>0.6</td>
<td>140</td>
</tr>
<tr>
<td>0.8</td>
<td>100</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
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<table>
<thead>
<tr>
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<th>Output Spectrum</th>
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<tbody>
<tr>
<td>0</td>
<td>-160</td>
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<td>0.2</td>
<td>-140</td>
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<td>0.4</td>
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<td>0.6</td>
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<td>0.8</td>
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</table>

<table>
<thead>
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<th>Loop Filter</th>
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