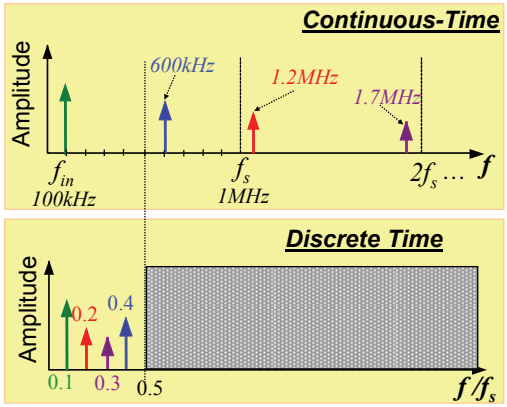
EE247
Lecture 9

- Switched-capacitor filters (continued)
  - Example of anti-aliasing prefilter for S.C. filters
  - Switched-capacitor network electronic noise
  - Switched-capacitor integrators
    - DDI integrators
    - LDI integrators
      - Effect of parasitic capacitance
      - Bottom-plate integrator topology
  - Switched-capacitor resonators
  - Bandpass filters
  - Lowpass filters
  - Switched-capacitor filter design considerations
    - Termination implementation
    - Transmission zero implementation
    - Effect of non-idealities

Sampling Sine Waves Frequency Spectrum

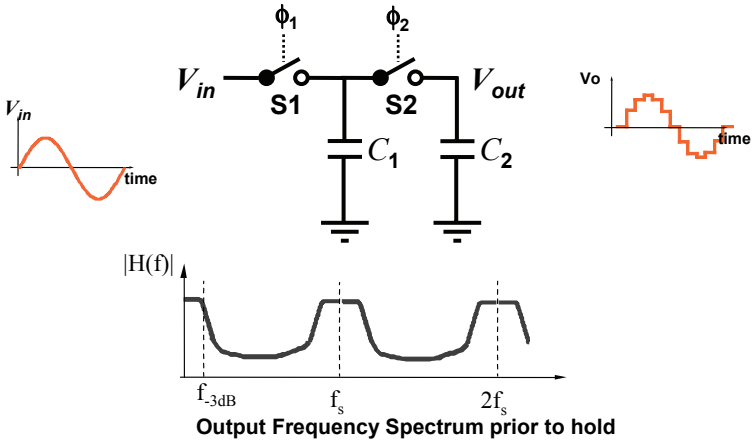
Signal scenario before sampling

Signal scenario after sampling



Key point: Signals @ $nf_S \pm f_{max\_signal}$ fold back into band of interest→Aliasing

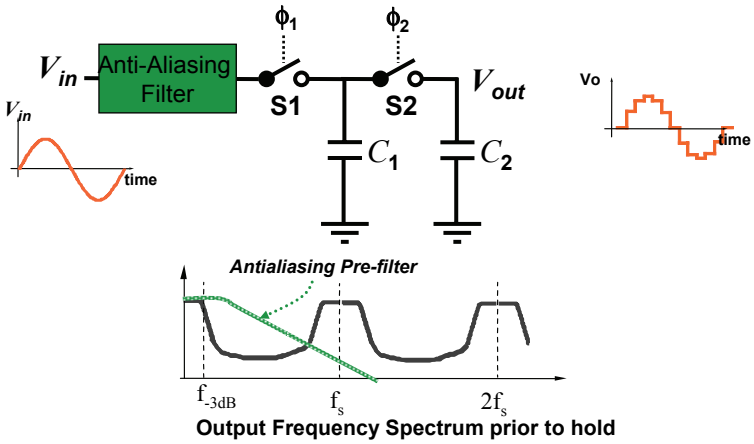
First Order S.C. Filter



Output Frequency Spectrum prior to hold

Switched-Capacitor Filters → problem with aliasing

First Order S.C. Filter



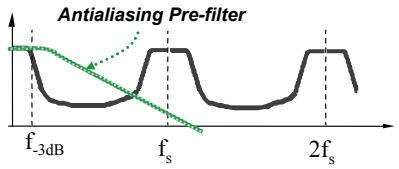
Output Frequency Spectrum prior to hold

Switched-Capacitor Filters → problem with aliasing

Sampled-Data Systems (Filters)
Anti-aliasing Requirements

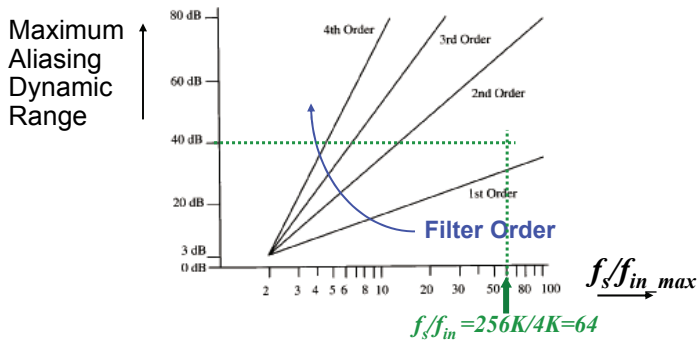
- Frequency response repeats at f_s, $2f_s$, $3f_s$.....
- High frequency signals close to f_s, $2f_s$,….folds back into passband (aliasing)
- Most cases must pre-filter input to sampled-data systems (filter) to attenuate signal at:
  $f > f_s/2$ (nyquist $\rightarrow f_{max} < f_s/2$)
- Usually, anti-aliasing filter → included on-chip as continuous-time filter with relaxed specs. (no tuning)

Example : Anti-Aliasing Filter Requirements



- Voice-band CODEC S.C. filter high order low-pass with $f_{-3dB} = 4kHz$ & $f_s = 256kHz$
- Anti-aliasing continuous-time pre-filter requirements:
  - Need at least 40dB attenuation of all out-of-band signals which can alias inband
  - Incur no phase-error from 0 to 4kHz
  - Gain error due to anti-aliasing filter → 0 to 4kHz < 0.05dB
  - Allow +-30% variation for anti-aliasing filter corner frequency (no tuning) **Need to find minimum required filter order**

Oversampling Ratio versus Anti-Aliasing Filter Order



* *Assumption → anti-aliasing filter is Butterworth type*

→2nd order Butterworth

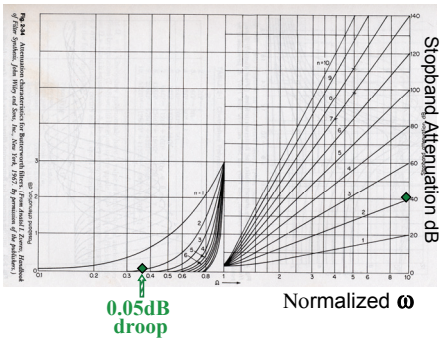
→Need to find minimum corner frequency for mag. droop < 0.05dB

Example : Anti-Aliasing Filter Specifications

- Normalized frequency for 0.05dB droop: need perform passband simulation→ normalized ω=0.34→ 4kHz/0.34=12kHz
- Set anti-aliasing filter corner frequency for minimum corner frequency 12kHz → Find nominal corner frequency: 12kHz/0.7=17.1kHz
- Check if attenuation requirement is satisfied for widest filter bandwidth → 17.1x1.3=22.28kHz
- Find $(f_s-f_{sig})/f_{-3dB}^{max}$

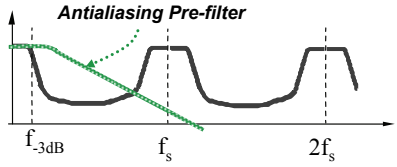
→252/22.2=11.35→ make sure enough attenuation

- Check phase-error within 4kHz signal band for min. filter bandwidth via simulation



From: Williams and Taylor, p. 2-37

Example : Anti-Aliasing Filter



- Voice-band S.C. filter $f_{-3dB}=4kHz$ & $f_s=256kHz$
- Anti-aliasing filter requirements:
  - Need 40dB attenuation at clock freq.
  - Incur no phase-error from 0 to 4kHz
  - Gain error 0 to 4kHz < 0.05dB
  - Allow +-30% variation for anti-aliasing corner frequency (no tuning)

→2-pole Butterworth LPF with nominal corner freq. of 17kHz & no tuning (min.=12kHz & max.=22kHz corner frequency)

Summary

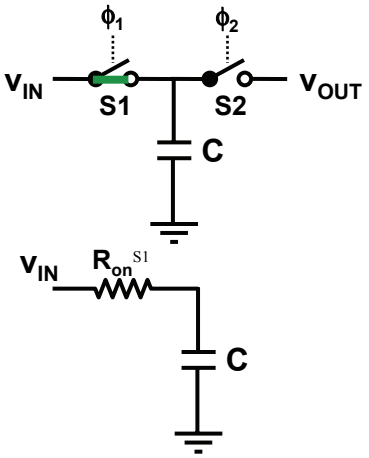
- Sampling theorem → $f_s > 2f_{max\_Signal}$
- Signals at frequencies $nf_S \pm f_{sig}$ fold back down to desired signal band, f_{sig}
  - → This is called <u>aliasing</u> & usually mandates use of anti-aliasing pre-filters combined with oversampling
- Oversampling helps reduce required order for anti-aliasing filter
- S/H function shapes the frequency response with <u>*sinx/x*</u> shape
  - → Need to pay attention to droop in passband due to <u>*sinx/x*</u>
- If the above requirements are not met, CT signals can NOT be recovered from sampled-data networks without loss of information

Switched-Capacitor Network Noise

- During ϕ_1 high: Resistance of switch S1 (R_{on}^{S1}) produces a noise voltage on C with variance kT/C (lecture 1- first order filter noise)
- The corresponding noise charge is:

$$Q^2 = C^2V^2 = C^2.\ kT/C = kTC$$

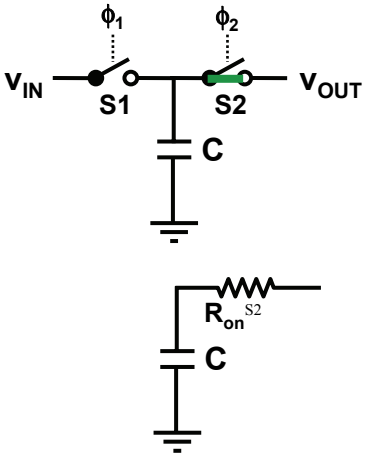
- ϕ_1 low: S1 open →This charge is sampled



Switched-Capacitor Noise

- During ϕ_2 high: Resistance of switch S2 contributes to an uncorrelated noise charge on C at the end of ϕ_2 : with variance kT/C
- Mean-squared noise charge transferred from v_{IN} to v_{OUT} per sample period is:

$$Q^2=2kTC$$



Switched-Capacitor Noise

- The mean-squared noise current due to S1 and S2's kT/C noise is :

$$Since\ \ i = Q/t \quad then \rightarrow \overline{i^2} = \left(Qf_s\right)^2 = 2k_BTCf_s^2$$

- This noise is approximately white and distributed between 0 and $f_s/2$ (noise spectra → single sided by convention)
  The spectral density of the noise is found:

$$\frac{\overline{i^2}}{\Delta f} = \frac{2k_BTCf_s^2}{f_s/2} = 4k_BTCf_s$$

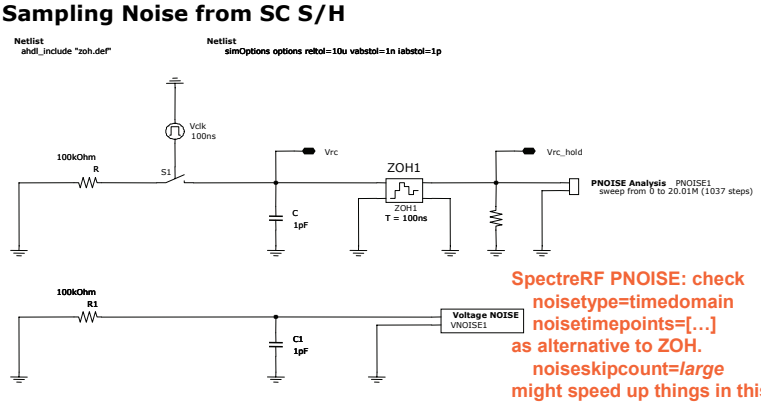
$$Since\ \ R_{EQ} = \frac{1}{f_sC} \quad then:$$

$$\boxed{\frac{\overline{i^2}}{\Delta f} = \frac{4k_BT}{R_{EQ}}}$$

→S.C. resistor noise = a physical resistor noise with same value!

Periodic Noise Analysis SpectreRF

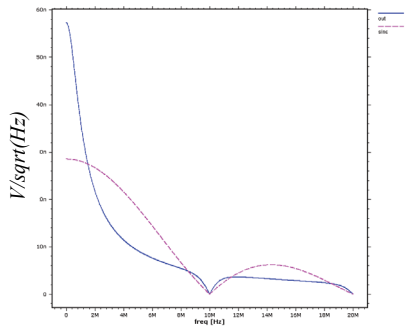
Sampling Noise from SC S/H



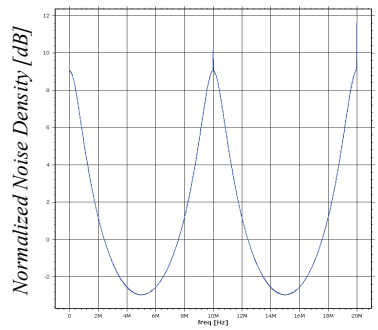
SpectreRF PNOISE: check
noisetype=timedomain
noisetimepoints=[…]
as alternative to ZOH.
noiseskipcount=*large*
might speed up things in this case.

```
PSS pss period=100n maxacfreq=1.5G errpreset=conservative
PNOISE ( Vrc_hold 0 ) pnoise start=0 stop=20M lin=500 maxsideband=10
```

Sampled Noise Spectrum

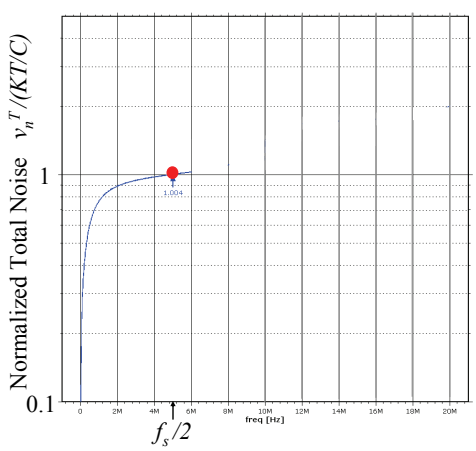


Spectral density of sampled noise including sinx/x effect



Noise spectral density with sinx/x effect taken out

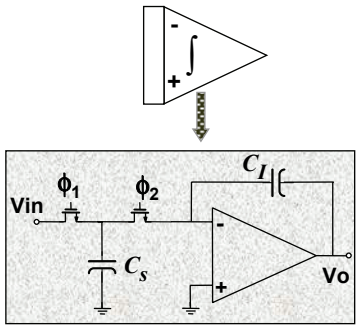
Total Noise

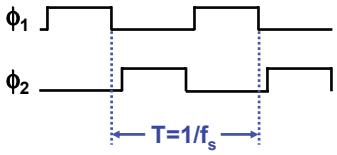


Sampled simulated noise in 0 … $f_s/2$: 62.2μV rms

(expect 64μV for 1pF)

Switched-Capacitor Integrator





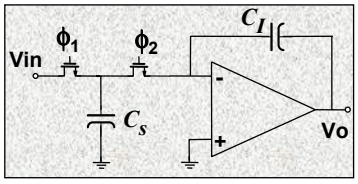
$$for \quad f_{signal} << f_{sampling}$$

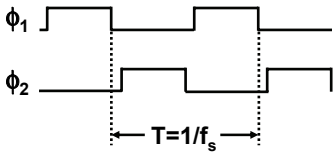
$$\rightarrow V_0 = \frac{f_s \times C_s}{C_I} \int V_{in}\, dt$$

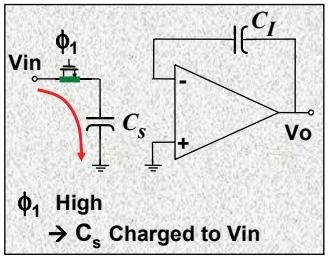
$$\omega_0 = f_s \times \frac{C_s}{C_I}$$

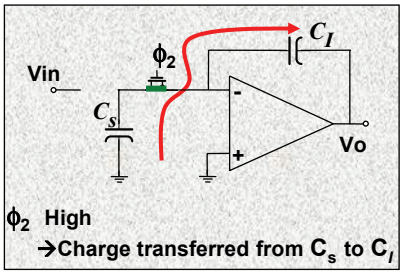
Main advantage: No tuning needed
→ Critical frequency function of ratio of capacitors & clock freq.

Switched-Capacitor Integrator









Continuous-Time versus Discrete-Time Analysis Approach

Continuous-Time

- Write differential equation
- Laplace transform ($F(s)$)
- Let $s=j\omega \rightarrow F(j\omega)$
- Plot $|F(j\omega)|$, $phase(F(j\omega))$

Discrete-Time

- Write difference equation → relates output sequence to input sequence
- Use delay operator z^{-1} to transform the recursive realization to algebraic equation in z domain
- Set $z = e^{j\omega T}$
- Plot mag./phase versus frequency

$$V_o(nT_s) = T_s \cdot V_i(nT_s) \cdots\cdots$$

$$V_o(z) = z^{-1} V_i(z) \ldots\ldots$$

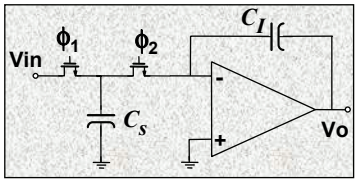
Discrete Time Design Flow

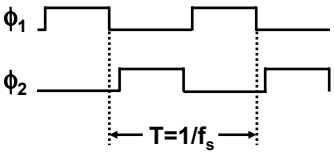
- Transforming the recursive realization to algebraic equation in z domain:
  - Use delay operator z :

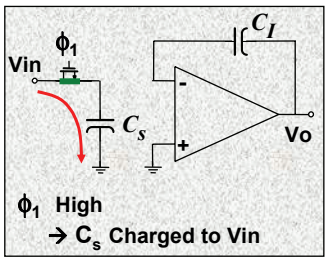
$$nT_S \ldots\ldots\ldots\ldots\ldots\ldots \rightarrow 1$$
$$\left[(n-1)T_S\right] \ldots\ldots\ldots\ldots \rightarrow z^{-1}$$
$$\left[(n-1/2)T_S\right] \ldots\ldots\ldots \rightarrow z^{-1/2}$$
$$\left[(n+1)T_S\right] \ldots\ldots\ldots\ldots \rightarrow z^{+1}$$
$$\left[(n+1/2)T_S\right] \ldots\ldots\ldots \rightarrow z^{+1/2}$$

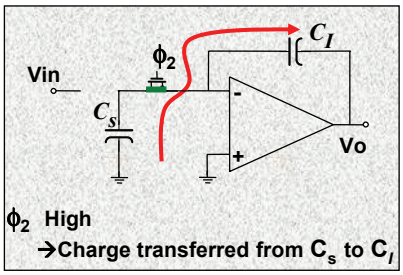
* Note: $z = e^{j\omega T_S} = cos(\omega T_s) + j\, sin(\omega T_s)$

Switched-Capacitor Integrator

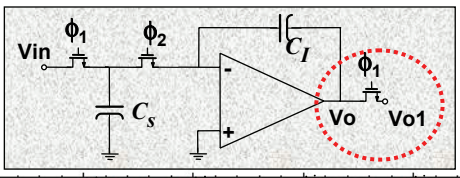


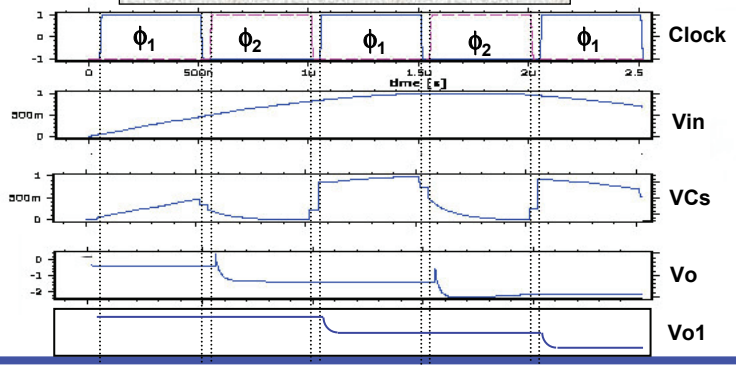




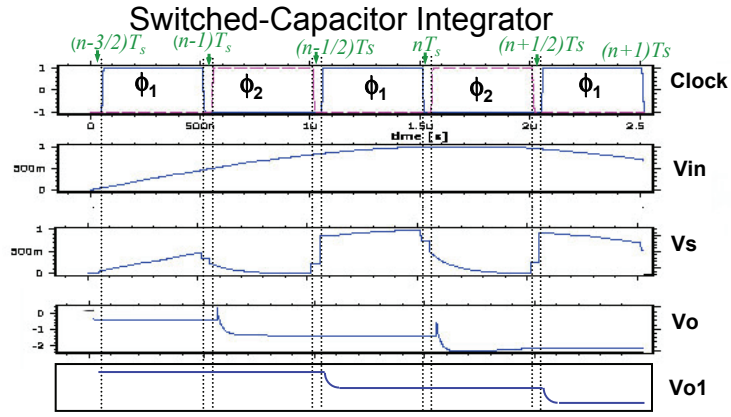


Switched-Capacitor Integrator
Output Sampled on ϕ1





Switched-Capacitor Integrator



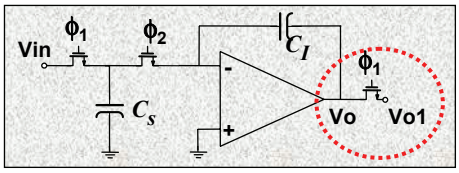
$\Phi_1 \rightarrow \quad Q_s[(n-1)T_s] = C_s V_i[(n-1)T_s]\,, \quad Q_I[(n-1)T_s] = Q_I[(n-3/2)T_s]$

$\Phi_2 \rightarrow \quad Q_s[(n-1/2)\,T_s] = 0\,, \quad Q_I[(n-1/2)\,T_s] = Q_I[(n-1)\,T_s] + Q_s[(n-1)\,T_s]$

$\Phi_1 \rightarrow \quad Q_s[nT_s] = C_s V_i[nT_s]\,, \quad \boxed{Q_I[nT_s] = Q_I[(n-1)\,T_s] + Q_s[(n-1)\,T_s]}$

Since $V_{o1} = -Q_I/C_I$ & $V_i = Q_s/C_s \rightarrow C_I V_{o1}(nT_s) = C_I V_{o1}[(n-1)\,T_s] - C_s V_i[(n-1)\,T_s]$

Switched-Capacitor Integrator Output Sampled on ϕ_1



$$C_I\ V_O(nT_S) = C_I\ V_O[(n-1)T_S] - C_S\ V_{in}[(n-1)T_S]$$

$$V_O(nT_S) = V_O[(n-1)T_S] - \frac{C_S}{C_I} V_{in}[(n-1)T_S]$$

$$V_O(Z) = Z^{-1} V_O(Z) - Z^{-1} \frac{C_S}{C_I} V_{in}(Z)$$

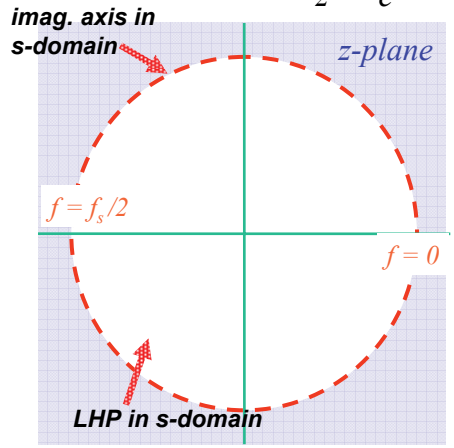
$$\frac{V_O}{V_{in}}(Z) = -\frac{C_S}{C_I} \times \boxed{\frac{Z^{-1}}{1-Z^{-1}}}$$

DDI (Direct-Transform Discrete Integrator)

z-Domain Frequency Response

- Sampled-data systems→ z plane singularities analyzed via z-plane
- The s-plane jω axis maps onto the unit-circle
- LHP singularities in s-plane map into inside of unit-circle in z-domain
- RHP singularities in s-plane map into outside of unit-circle in z-domain
- Particular values:
  - $f = 0 \rightarrow z = 1$
  - $f = f_s/2 \rightarrow z = -1$

$$z = e^{s.Ts}$$

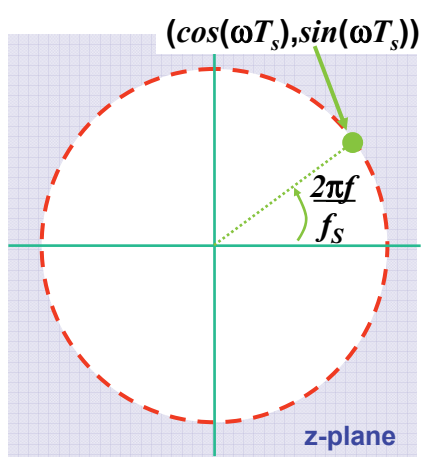


z-Domain Frequency Response

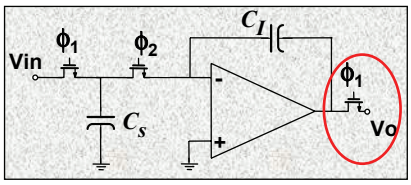
- The frequency response is obtained by evaluating H(z) on the unit circle at:

  $z = e^{j\omega T} = \cos(\omega T_s) + j \sin(\omega T_s)$

- Once $z=-1$ ($f_s/2$) is reached, the frequency response repeats, as expected
- The angle to the pole is equal to 360° (or 2π radians) times the ratio of the pole frequency to the sampling frequency



Switched-Capacitor Direct-Transform Discrete Integrator



$$\frac{V_o}{V_{in}}(z) = -\frac{C_s}{C_I} \times \frac{z^{-1}}{1-z^{-1}}$$

$$= -\frac{C_s}{C_I} \times \frac{1}{z-1}$$

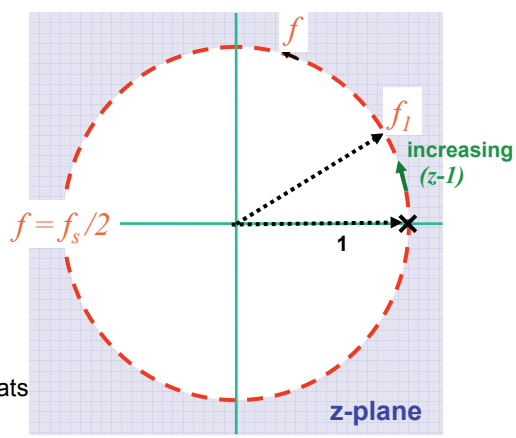
DDI Integrator Pole-Zero Map in z-Plane

$z - 1 = 0 \rightarrow z = 1$
on unit circle

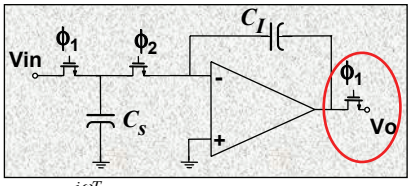
Pole from $f \rightarrow 0$
in s-plane mapped to $z = +1$

As frequency increases z domain point moves on unit circle (CCW)

Once frequency gets to:
$z = -1$ ($f = f_s/2$)
→ frequency response repeats



DDI Switched-Capacitor Integrator



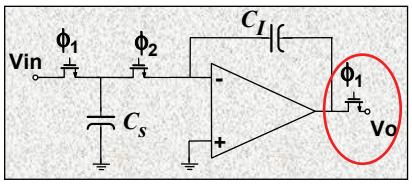
$$\frac{V_O}{V_{in}}(z) = -\frac{C_s}{C_I} \times \frac{z^{-1}}{1-z^{-1}} = \frac{C_s}{C_I} \times \frac{1}{1-z} \quad , \quad z = e^{j\omega T}$$

$$= \frac{C_s}{C_I} \times \frac{1}{1-e^{j\omega T}} = \frac{C_s}{C_I} \times \frac{e^{-j\omega T/2}}{e^{-j\omega T/2} - e^{j\omega T/2}} \qquad since: \quad sin\alpha = \frac{e^{j\alpha} - e^{-j\alpha}}{2j}$$

$$= -j\frac{C_s}{C_I} \times e^{-j\omega T/2} \times \frac{1}{2sin(\omega T/2)}$$

$$= \underbrace{-\frac{C_s}{C_I}\frac{1}{j\omega T}}_{\text{Ideal Integrator}} \times \underbrace{\frac{\omega T/2}{sin(\omega T/2)}}_{\text{Magnitude Error}} \times \underbrace{e^{-j\omega T/2}}_{\text{Phase Error}}$$

DDI Switched-Capacitor Integrator



$$\frac{V_O}{V_{in}}(z) = = -\frac{C_s}{C_I}\frac{1}{j\omega T} \times \underbrace{\frac{\omega T/2}{sin(\omega T/2)}}_{\text{Magnitude Error}} \times \underbrace{e^{-j\omega T/2}}_{\text{Phase Error}}$$

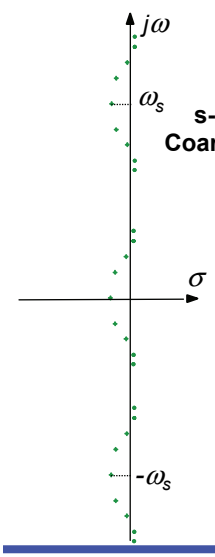
Example: Mag. & phase error for:

1- f/f_s=1/12 → Mag. error = 1% or 0.1dB
Phase error=15 degree
Q_{intg} = -3.8

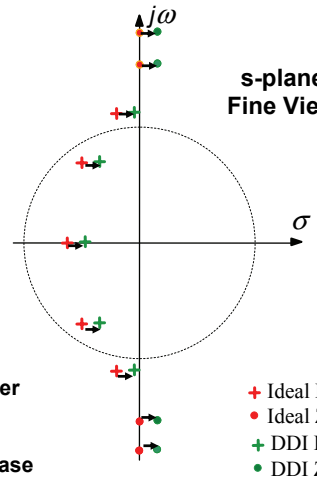
2- f/f_s=1/32 → Mag. error=0.16% or 0.014dB
Phase error=5.6 degree
Q_{intg} = -10.2

DDI Integrator:
→ magnitude error no problem
phase error major problem

5th Order Low-Pass Switched Capacitor Filter Built with DDI Integrators



s-plane Coarse View

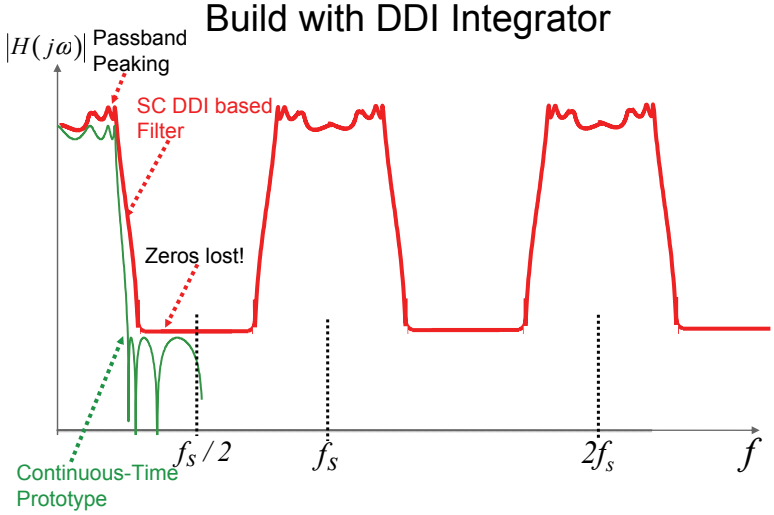


s-plane Fine View

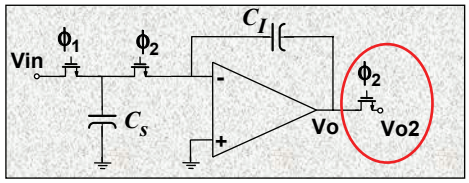
Example:
5th Order Elliptic Filter
Singularities pushed towards RHP due to integrator excess phase

+ Ideal Pole
• Ideal Zero
+ DDI Pole
• DDI Zero

Switched Capacitor Filter Build with DDI Integrator



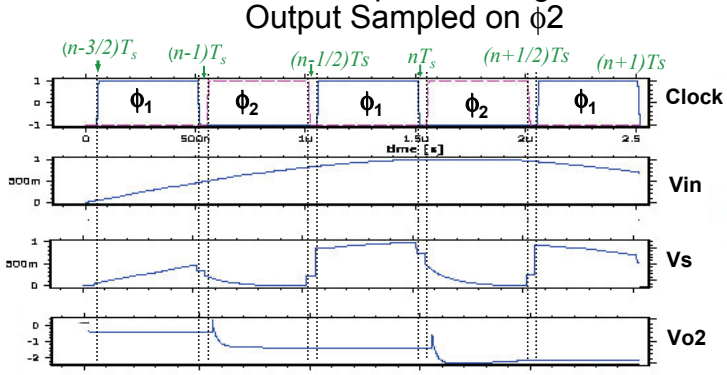
Switched-Capacitor Integrator Output Sampled on $\phi 2$



Sample output ½ clock cycle earlier

→ Sample output on ϕ_2

Switched-Capacitor Integrator Output Sampled on $\phi 2$



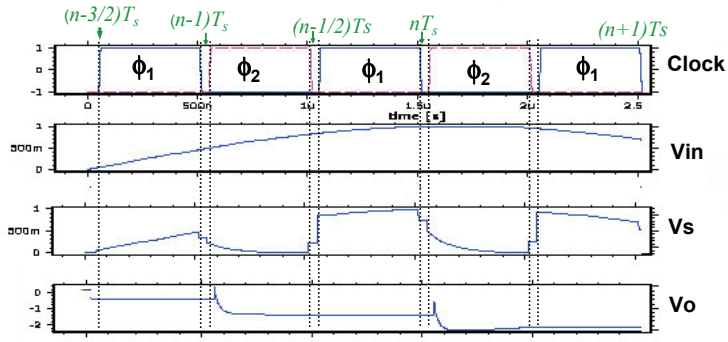
$\Phi_1 \rightarrow$ $Q_s[(n-1)T_s] = C_s V_i[(n-1)T_s]$, $Q_I[(n-1)T_s] = Q_I[(n-3/2)T_s]$

$\Phi_2 \rightarrow$ $Q_s[(n-1/2)T_s] = 0$, $Q_I[(n-1/2)T_s] = Q_I[(n-3/2)T_s] + Q_s[(n-1)T_s]$

$\Phi_1 \rightarrow$ $Q_s[nT_s] = C_s V_i[nT_s]$, $Q_I[nT_s] = Q_I[(n-1)T_s] + Q_s[(n-1)T_s]$

$\Phi_2 \rightarrow$ $Q_s[(n+1/2)T_s] = 0$, $Q_I[(n+1/2)T_s] = Q_I[(n-1/2)T_s] + Q_s[nT_s]$

Switched-Capacitor Integrator
Output Sampled on $\phi 2$



$Q_I\,[(n+1/2)\,T_s] = Q_I\,[(n-1/2)\,T_s] + Q_s\,[n\,T_s]$

$V_{o2} = -\,Q_I/C_I$ & $V_i = Q_s/C_s$ → $C_I\,V_{o2}\,[(n+1/2)\,T_s] = C_I\,V_{o2}\,[(n-1/2)\,T_s] - C_s\,V_i\,[n\,T_s]$

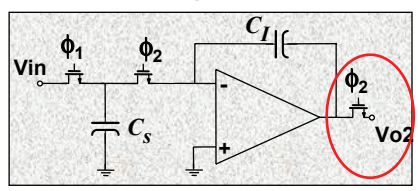
Using the z operator rules:

→ $C_I\,V_{o2}\,z^{1/2} = C_I\,V_{o2}\,z^{-1/2} - C_s\,V_i$

$$\boxed{\frac{V_{o2}}{V_{in}}(z) = -\frac{C_s}{C_I}\times\frac{z^{-1/2}}{1-z^{-1}}}$$

LDI Switched-Capacitor Integrator

LDI (Lossless Discrete Integrator) → same as DDI but output is sampled ½ clock cycle earlier



LDI

$$\frac{V_{o2}}{V_{in}}(z) = -\frac{C_s}{C_I}\times\boxed{\frac{z^{-1/2}}{1-z^{-1}}}\quad,\qquad z = e^{j\omega T}$$

$$= -\frac{C_s}{C_I}\times\frac{e^{-j\omega T/2}}{1-e^{-j\omega T}} = \frac{C_s}{C_I}\times\frac{1}{e^{-j\omega T/2}-e^{+j\omega T/2}}$$

$$= -j\frac{C_s}{C_I}\times\frac{1}{2\sin(\omega T/2)}$$

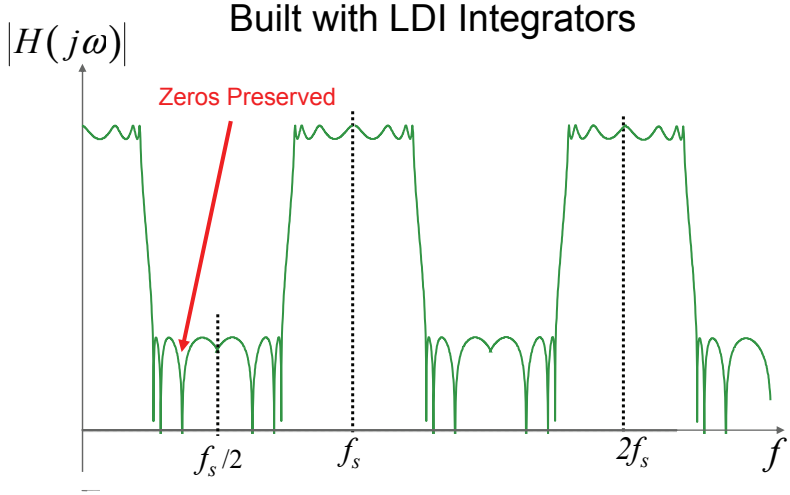
$$= -\frac{C_s}{C_I}\,\frac{1}{j\omega T}\times\frac{\omega T/2}{\sin(\omega T/2)}$$

Ideal Integrator

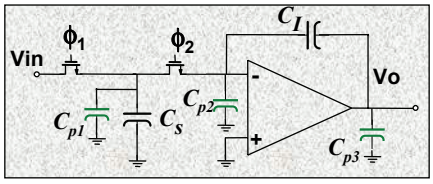
Magnitude Error

No Phase Error!
For signals at frequencies << sampling freq.
→ Magnitude error negligible

Switched-Capacitor Filter Built with LDI Integrators



Switched-Capacitor Integrator Parasitic Capacitor Sensitivity



Effect of parasitic capacitors:

1- C_{p3} – driven by opamp o.k.

2- C_{p2} – at opamp virtual gnd o.k.

3- C_{p1} – Charges to Vin & discharges into C_I,

– C_{p1} includes the MOS switch junction capacitors which are voltage dependent, not only affects C ratios but results in non-linearities

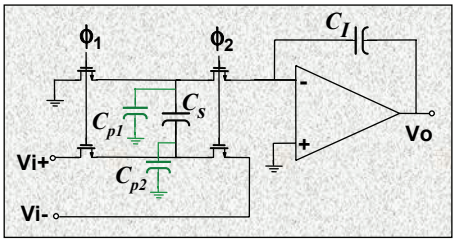
→ **Problem parasitic capacitor sensitivity**

Parasitic Insensitive Bottom-Plate Switched-Capacitor Integrator

Sensitive parasitic cap. → C_{p1} → rearrange circuit so that C_{p1} does not charge/discharge

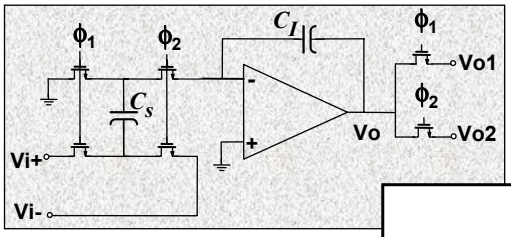
ϕ1=1 → C_{p1} grounded

ϕ2=1 → C_{p1} at virtual ground



Solution: Bottom plate capacitor integrator

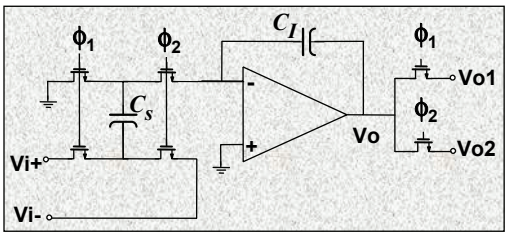
Bottom Plate Switched-Capacitor Integrator

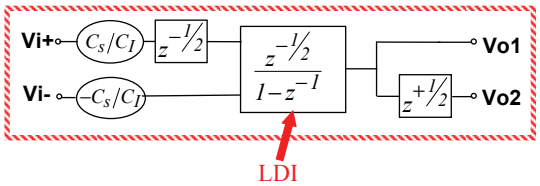


Note:
Different delay from Vi+ & Vi- to either output
→ Special attention needed for input/output connections to ensure LDI realization

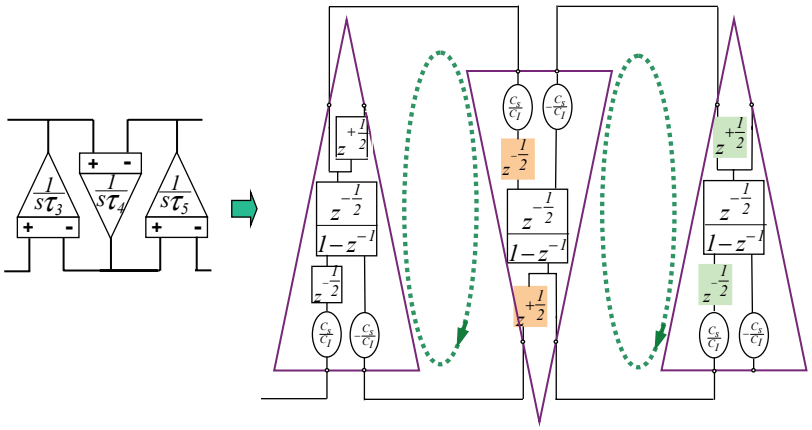
Output/Input z-Transform		
	Vo1 on **ϕ1**	Vo2 on **ϕ2**
Vi+ on **ϕ1**	$\frac{C_S}{C_I}\frac{z^{-1}}{1-z^{-1}}$	$\frac{C_S}{C_I}\frac{z^{-1/2}}{1-z^{-1}}$
Vi- on **ϕ2**	$-\frac{C_S}{C_I}\frac{z^{-1/2}}{1-z^{-1}}$	$-\frac{C_S}{C_I}\frac{1}{1-z^{-1}}$

Bottom Plate Switched-Capacitor Integrator z-Transform Model



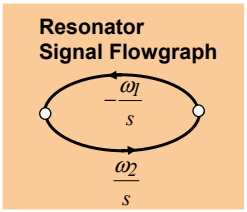


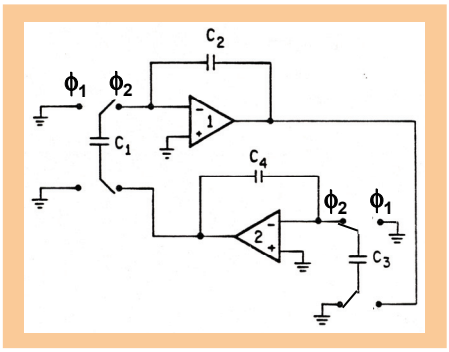
LDI Switched-Capacitor Ladder Filter



Delay around integrator loop is ($z^{-1/2} \cdot z^{+1/2} = 1$) ➔ LDI function

Switched-Capacitor LDI Resonator



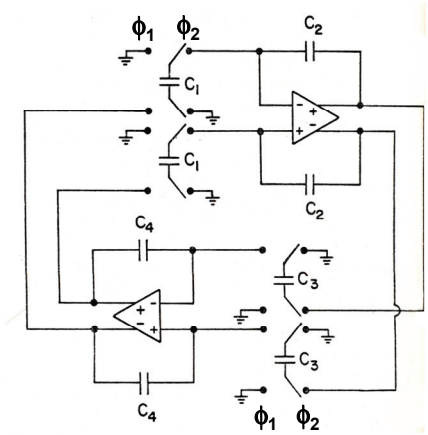


$$\omega_1 = \frac{1}{R_{eq1} C_2} = f_s \times \frac{C_1}{C_2}$$

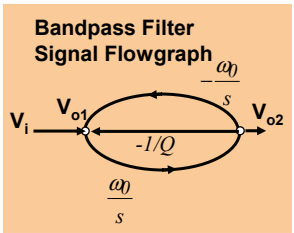
$$\omega_2 = \frac{1}{R_{eq3} C_4} = f_s \times \frac{C_3}{C_4}$$

Fully Differential Switched-Capacitor Resonator

- Note: Two sets of S.C. bottom plate networks for each differential integrator

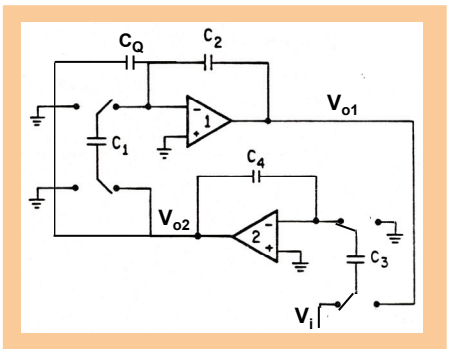


Switched-Capacitor LDI Bandpass Filter Utilizing Continuous-Time Termination

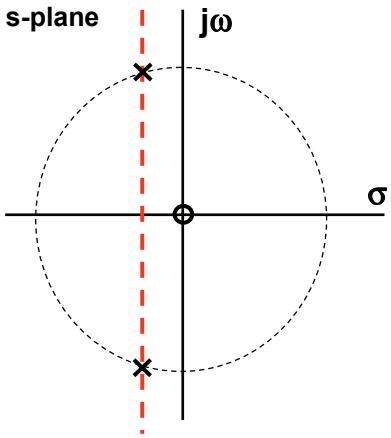


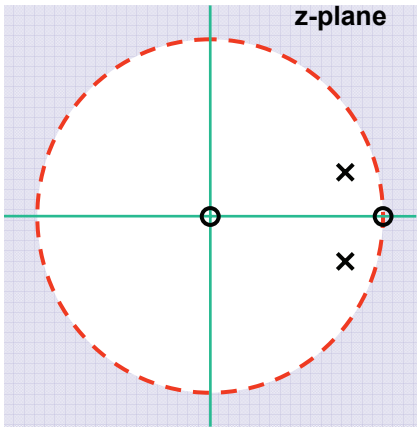
$$\omega_0 = f_s \times \frac{C_3}{C_4} = f_s \times \frac{C_1}{C_2}$$

$$Q = \frac{C_2}{C_Q}$$



Example: 2nd Order LDI Bandpass Filter s-Plane versus z-Plane





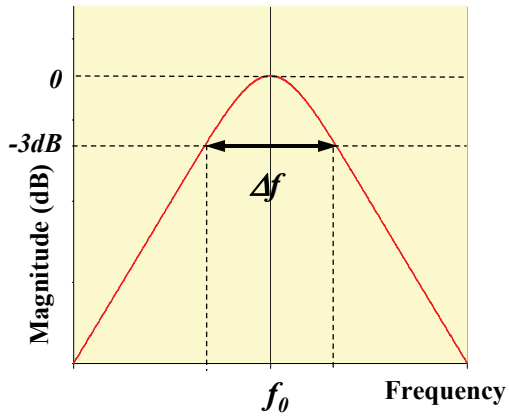
Switched-Capacitor LDI Bandpass Filter Continuous-Time Termination

$$f_0 = \frac{1}{2\pi} f_s \times \frac{C_1}{C_2}$$

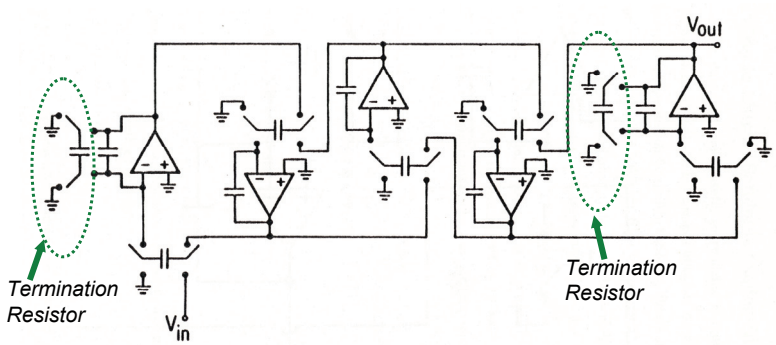
$$\Delta f = \frac{f_0}{Q}$$

$$= \frac{1}{2\pi} f_s \times \frac{C_1 C_Q}{C_2 C_4}$$

Both accurately determined by cap ratios & clock frequency



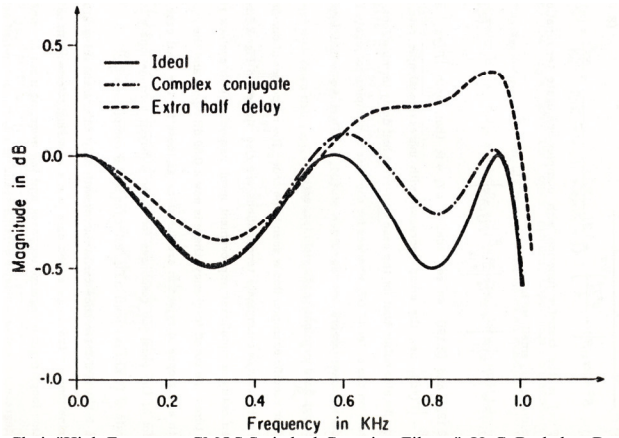
Fifth Order All-Pole LDI Low-Pass Ladder Filter Complex Conjugate Terminations



•Complex conjugate terminations (alternate phase switching)

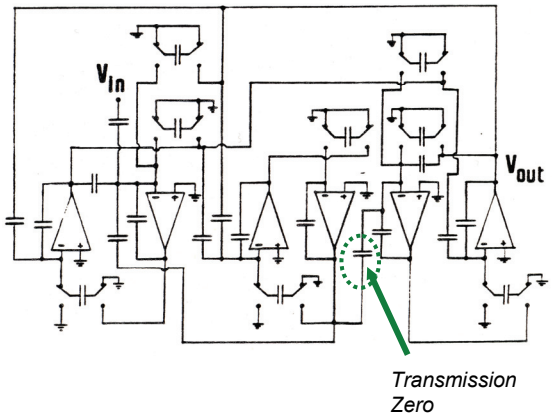
Ref: Tat C. Choi, "High-Frequency CMOS Switched-Capacitor Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, May 1983 (ERL Memorandum No. UCB/ERL M83/31).

Fifth-Order All-Pole Low-Pass Ladder Filter Termination Implementation



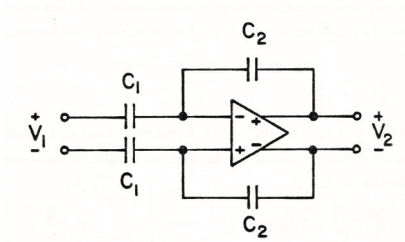
Ref: Tat C. Choi, "High-Frequency CMOS Switched-Capacitor Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, May 1983 (ERL Memorandum No. UCB/ERL M83/31).

Sixth-Order Elliptic LDI Bandpass Filter



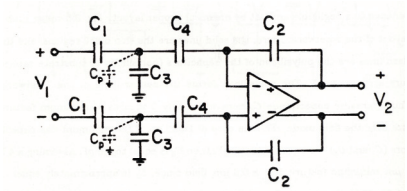
Ref: Tat C. Choi, "High-Frequency CMOS Switched-Capacitor Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, May 1983 (ERL Memorandum No. UCB/ERL M83/31).

Use of T-Network



$C_2:C_1 = 100:1$

$$\frac{V_2}{V_1} = -\frac{C_1}{C_2}$$



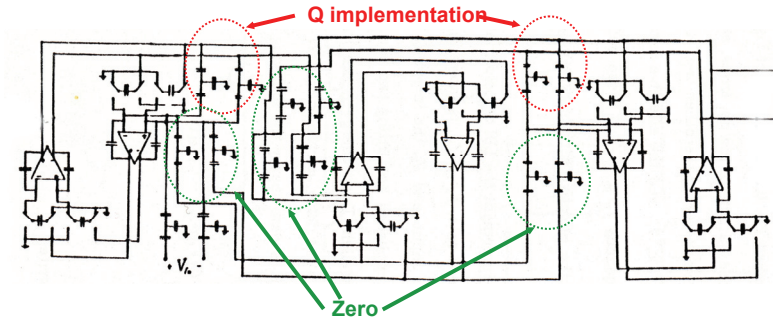
$C_4:C_3:C_2:C_1 = 1:8:10:1$

$$\frac{V_2}{V_1} = -\frac{C_1}{C_2} \times \frac{C_4}{C_1 + C_3 + C_4}$$

High Q filter → large cap. ratio for Q & transmission zero implementation
To reduce large ratios required → T-networks utilized

Ref: Tat C. Choi, "High-Frequency CMOS Switched-Capacitor Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, May 1983 (ERL Memorandum No. UCB/ERL M83/31).

Sixth Order Elliptic Bandpass Filter Utilizing T-Network



- **T-networks utilized** for:
  - **Q implemention**
  - **Transmission zero implementation**

Ref: Tat C. Choi, "High-Frequency CMOS Switched-Capacitor Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, May 1983 (ERL Memorandum No. UCB/ERL M83/31).

Effect of Opamp Nonidealities on Switched Capacitor Filter Behaviour

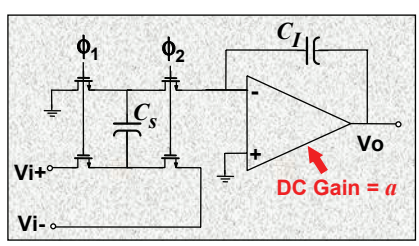
- Opamp finite gain
- Opamp finite bandwidth
- Finite slew rate of the opamp
- Non-linearity associated with opamp output/input characteristics

Effect of Opamp Non-Idealities Finite DC Gain

$$H(s) \approx -f_s \frac{C_s}{C_I} \frac{1}{s + f_s \frac{C_s}{C_I} \times \frac{1}{a}}$$

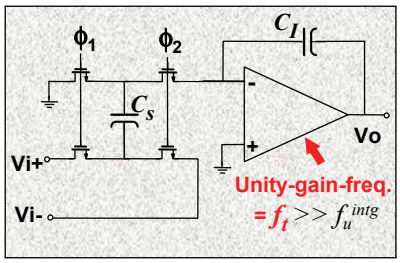
$$H(s) \approx \frac{-\omega_o}{s + \omega_o \times \frac{1}{a}}$$

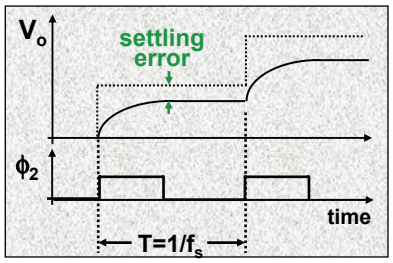
$$\Rightarrow \boxed{Q_{intg} \approx a}$$



- **Finite DC gain same effect in S.C. filters as for C.T. filters**
- **If DC gain not high enough → lowering of overall Q & droop in passband**

Effect of Opamp Non-Idealities
Finite Opamp Bandwidth





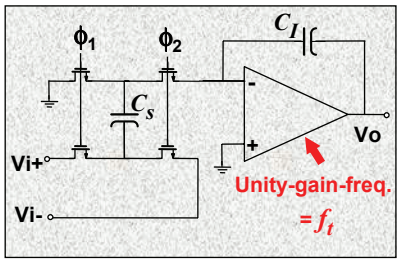
Assumption-

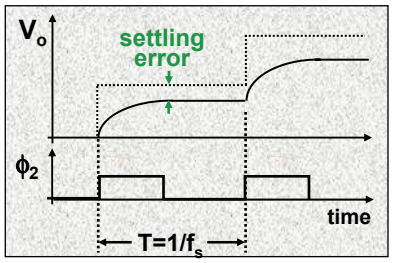
Opamp → does not slew (will be revisited)

Opamp has one pole only → exponential settling

Ref: K.Martin, A. Sedra, "Effect of the Opamp Finite Gain & Bandwidth on the Performance of Switched-Capacitor Filters," IEEE Trans. Circuits Syst., vol. CAS-28, no. 8, pp. 822-829, Aug 1981.

Effect of Opamp Non-Idealities
Finite Opamp Bandwidth





$$H_{actual}(Z) \approx H_{ideal}(Z)\left[1-e^{-k}+e^{-k}\times\frac{C_I}{C_I+C_s}Z^{-1}\right]$$

$$where \quad k=\pi\times\frac{C_I}{C_I+C_s}\times\frac{f_t}{f_s}$$

$$f_t \rightarrow \ Opamp\ unity-gain-frequency \quad , \quad f_s \rightarrow \ Clock\ frequency$$

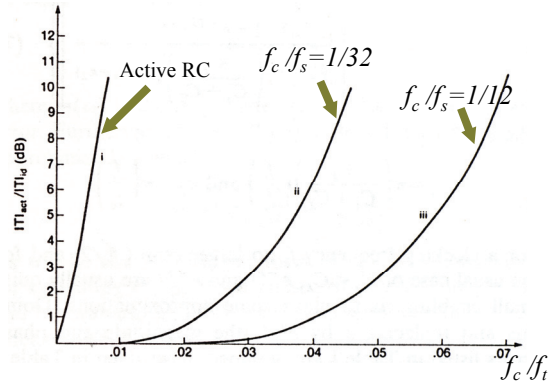
Ref: K.Martin, A. Sedra, "Effect of the Opamp Finite Gain & Bandwidth on the Performance of Switched-Capacitor Filters," IEEE Trans. Circuits Syst., vol. CAS-28, no. 8, pp. 822-829, Aug 1981.

Effect of Opamp Finite Bandwidth on Filter Magnitude Response

$|T|_{non\text{-}ideal} / |T|_{ideal}$ (dB)

Magnitude deviation due to finite opamp unity-gain-frequency

Example: 2nd order bandpass with ideal Q=25



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Effect of Opamp Finite Bandwidth on Filter Magnitude Response

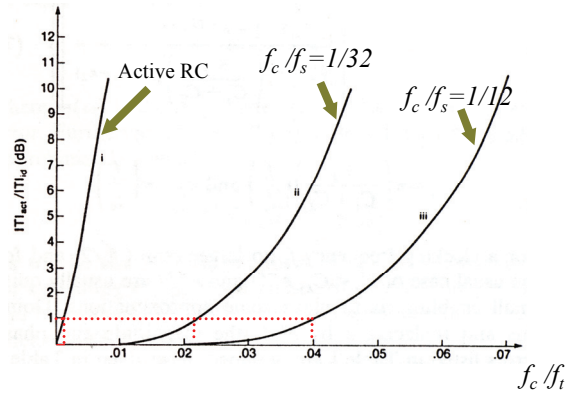
$|T|_{non\text{-}ideal} / |T|_{ideal}$ (dB)

Example:
For 1dB magnitude response deviation:

1- $f_c/f_s=1/12$
$f_c/f_t \sim 0.04$
→ $f_t > 25 f_c$

2- $f_c/f_s=1/32$
$f_c/f_t \sim 0.022$
→ $f_t > 45 f_c$

3- *Cont.-Time*
$f_c/f_t \sim 1/700$
→ $f_t > 700 f_c$



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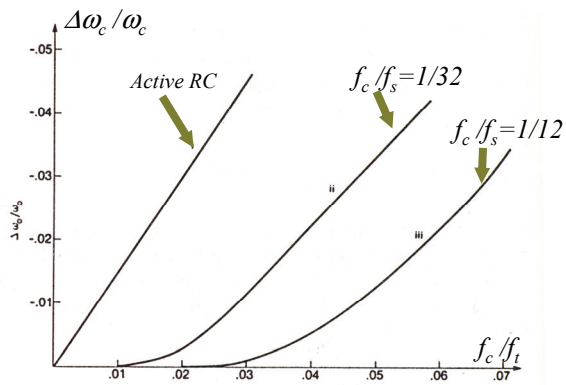
Effect of Opamp Finite Bandwidth on Filter Critical Frequency

Critical frequency deviation due to finite opamp unity-gain-frequency

Example: 2nd order filter



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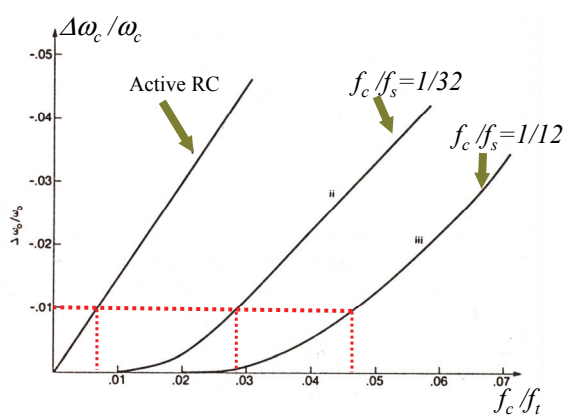
Effect of Opamp Finite Bandwidth on Filter Critical Frequency

Example:
For maximum critical frequency shift of <1%

1- $f_c/f_s=1/32$
$f_c/f_t \sim 0.028$
→ $f_t > 36 f_c$

2- $f_c/f_s=1/12$
$f_c/f_t \sim 0.046$
→ $f_t > 22 f_c$

3- *Active RC*
$f_c/f_t \sim 0.008$
→ $f_t > 125 f_c$



Ref: K.Martin, A. Sedra, "Effect of the Opamp Finite Gain & Bandwidth on the Performance of Switched-Capacitor Filters," IEEE Trans. Circuits Syst., vol. CAS-28, no. 8, pp. 822-829, Aug 1981.

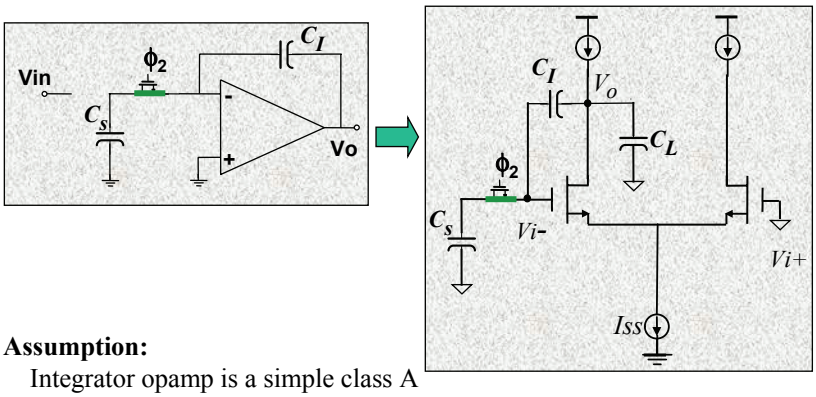
Opamp Bandwidth Requirements for Switched-Capacitor Filters Compared to Continuous-Time Filters

- Finite opamp bandwidth causes phase lag at the unity-gain frequency of the integrator for both type filters
  → Results in negative intg. Q & thus increases overall Q and gain & results in peaking in the passband in the frequency band of interest
- For given filter requirements, opamp bandwidth requirements are much less stringent for S.C. filters compared to cont. time filters
  → Lower power dissipation for S.C. filters (at low freq.s only due to other effects)
- Finite opamp bandwidth causes down shifting of critical frequencies in both type filters
  – Since cont. time filters are usually tuned→ tuning accounts for frequency deviation
  – S.C. filters are untuned and thus frequency shift could cause problems specially for narrow-band filters

Sources of Distortion in Switched-Capacitor Filters

- Opamp output/input transfer function non-linearity- similar to cont. time filters
- Capacitor non-linearity, similar to cont. time filters
- Distortion induced by finite slew rate of the opamp
- Distortion incurred by finite setting time of the opamp
- Distortion due to switch clock feed-through and charge injection

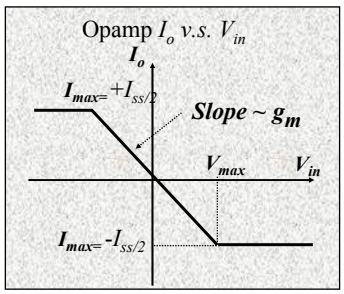
What is Slewing?

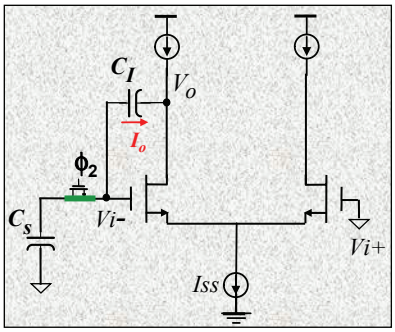


Assumption:

Integrator opamp is a simple class A transconductance type differential pair with fixed tail current, *Iss=const.*

What is Slewing?





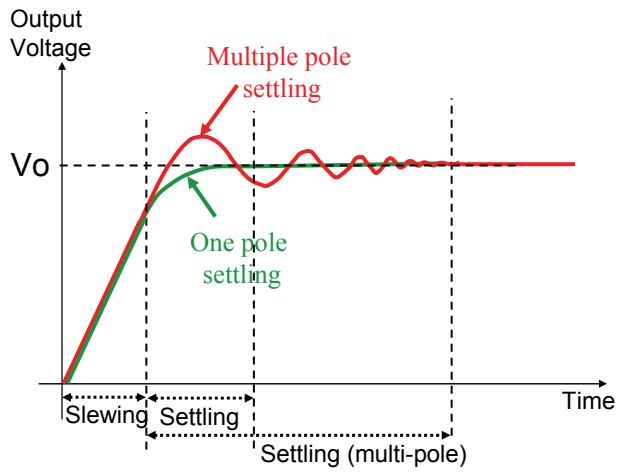
$|V_{Cs}| > V_{max}$ → Output current constant I_o=*Iss/2 or –Iss/2*

→ Constant current charging/discharging C_I: V_o ramps down/up → Slewing

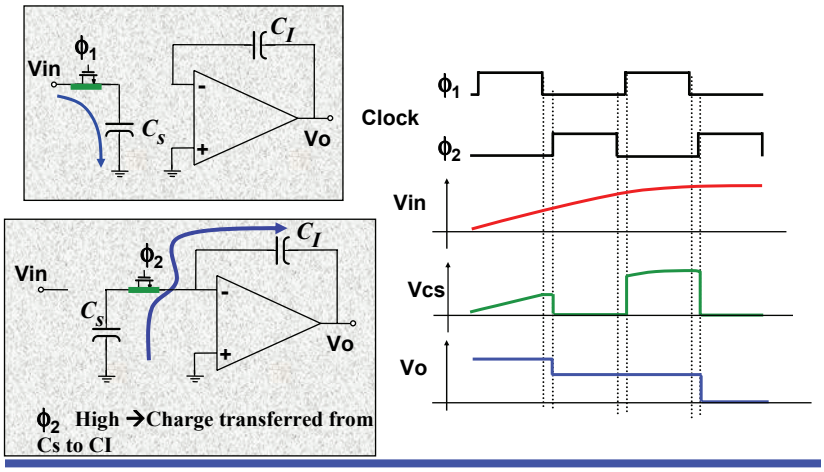
After V_{Cs} is discharged enough to have:

$|V_{Cs}|<V_{max}$ → I_o=*gm* V_{Cs} → Exponential or over-shoot settling

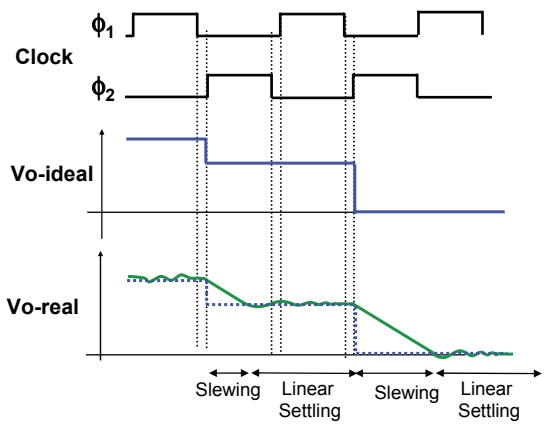
Distortion Induced by Opamp Finite Slew Rate



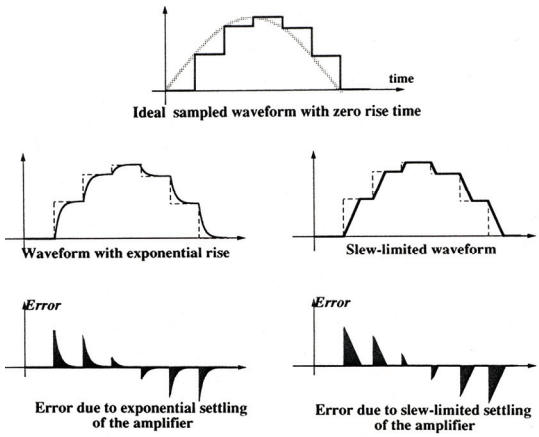
Ideal Switched-Capacitor Output Waveform



Slew Limited Switched-Capacitor Integrator Output Slewing & Settling



Distortion Induced by Finite Slew Rate of the Opamp



Ref: K.L. Lee, "Low Distortion Switched-Capacitor Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, Feb. 1986 (ERL Memorandum No. UCB/ERL M86/12).

Distortion Induced by Opamp Finite Slew Rate

- Error due to exponential settling changes linearly with signal amplitude
- Error due to slew-limited settling changes non-linearly with signal amplitude (doubling signal amplitude X4 error)
  - → For high-linearity need to have either high slew rate or non-slewing opamp

$$HD_k = \frac{V_o}{S_r T_s} \frac{8\left(\sin \omega_o T_s/2\right)^2}{\pi k\left(k^2-4\right)}$$

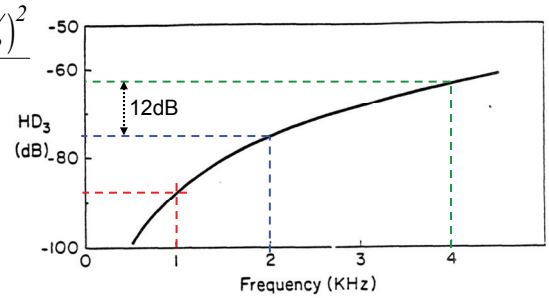
$$\rightarrow HD_3 = \frac{V_o}{S_r T_s} \frac{8\left(\sin \omega_o T_s/2\right)^2}{15\pi} \quad for \quad f_o << f_s \rightarrow \quad HD_3 \approx \frac{8\pi V_o}{15 S_r} \frac{f_o^2}{f_s}$$

Ref: K.L. Lee, "Low Distortion Switched-Capacitor Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, Feb. 1986 (ERL Memorandum No. UCB/ERL M86/12).

Example: Slew Related Harmonic Distortion

$$HD_3 = \frac{V_o}{S_r T_s} \frac{8\left(\sin \omega_o T_s/2\right)^2}{15\pi}$$

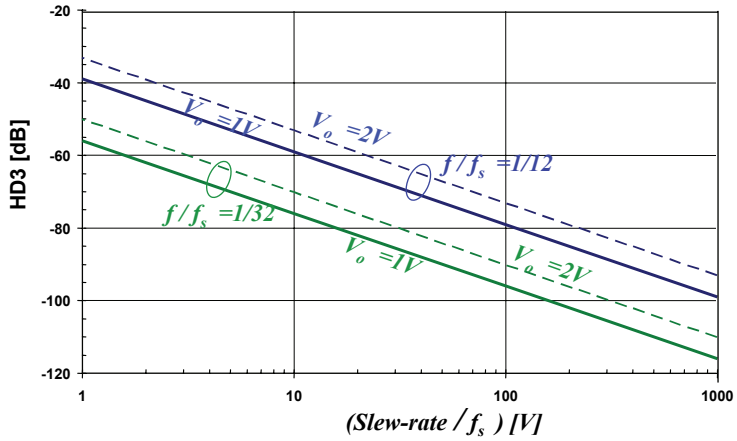
$$HD_3 \approx \frac{8\pi V_o}{15 S_r} \frac{f_o^2}{f_s}$$



Switched-capacitor filter with *4kHz* bandwidth, f_s=128kHz, S_r=1V/μsec, V_o=3V

Ref: K.L. Lee, "Low Distortion Switched-Capacitor Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, Feb. 1986 (ERL Memorandum No. UCB/ERL M86/12).

Distortion Induced by Opamp Finite Slew Rate Example



Distortion Induced by Finite Slew Rate of the Opamp

- Note that for a high order switched capacitor filter → only the last stage slewing will affect the output linearity (as long as the previous stages settle to the required accuracy)
  - → Can reduce slew limited non-linearity by using an amplifier with a higher slew rate *only* for the last stage
  - → Can reduce slew limited non-linearity by using class A/B amplifiers
    - Even though the output/input characteristics is non-linear as long as the DC open-loop gain is high, the significantly higher slew rate compared to class A amplifiers helps improve slew rate induced distortion
- In cases where the output is sampled by another sampled data circuit (e.g. an ADC or a S/H) → no issue with the slewing of the output as long as the output settles to the required accuracy & is sampled at the right time